

ABSTRACT

A memory device for improving the speed of a program operation and an operating method thereof is provided. The memory device includes a memory cell array including a plurality of memory cells, a voltage generator configured to generate voltages for one or more program operations and a verify operation performed on the plurality of memory cells, a control logic configured to perform a control operation on the plurality of memory cells so that a first program and a second program loop are performed, a second program operation being performed based on a compensation voltage level determined based on a result of the first verify operation, and a plurality of bit lines connected to the memory cell array, wherein the first verify operation includes first even sensing and second even sensing on even-numbered bit lines, and first odd sensing and second odd sensing on odd-numbered bit lines.

FIG. 1