

CLAIMS**WHAT IS CLAIMED IS:**

1. A method of performing a memory operation, the method comprising:
providing, by a processor, two or more source addresses of a memory;
copying two or more data elements from the two or more source addresses in the memory to a gather result buffer; and
loading the two or more data elements from the gather result buffer to a vector register in the processor using a single instruction multiple data (SIMD) load operation.
2. The method of claim 1, wherein the gather result buffer is located in the memory or in close proximity to the memory.
3. The method of claim 1, wherein the gather result buffer is a circular buffer.
4. The method of claim 1, wherein the two or more source addresses are orthogonal or independent and non-contiguous in the memory.
5. The method of claim 1, comprising copying the two or more data elements to the gather result buffer out-of-order.
6. The method of claim 5, wherein copying the two or more data elements to the gather result buffer out-of-order involves two or more different latencies.
7. The method of claim 5, comprising copying the two or more data elements to the gather result buffer out-of-order in a background mode without direction by the processor.
8. The method of claim 5, comprising tracking the gather result buffer and loading the two or more data elements from the gather result buffer after the gather result buffer is complete.
9. A method of performing a memory operation, the method comprising:

providing, by a processor, two or more source addresses and corresponding two or more destination addresses of a memory; and

executing two or more instructions for copying two or more data elements from the two or more source addresses to corresponding two or more destination addresses within the memory, without an intermediate copy to a register in a processor.

10. The method of claim 9, wherein the two or more source addresses are orthogonal or independent and non-contiguous.

11. The method of claim 9, wherein the two or more destination addresses are orthogonal or independent and non-contiguous in the memory.

12. The method of claim 9, wherein copying two or more data elements from the two or more source addresses to corresponding two or more destination addresses within the memory comprises executing a single instruction multiple data (SIMD) copy instruction.

13. The method of claim 12, comprising executing the SIMD copy instruction in a background mode without direction by the processor.

14. An apparatus comprising:
a processor configured to provide two or more source addresses of a memory;
a gather result buffer configured to receive two or more data elements copied from the two or more source addresses in the memory; and
logic configured to load the two or more data elements from the gather result buffer to a vector register in the processor based on a single instruction multiple data (SIMD) load operation executed by the processor.

15. The apparatus of claim 14, wherein the gather result buffer is located in the memory or in close proximity to the memory.

16. The apparatus of claim 14, wherein the gather result buffer is a circular buffer or storage structure configured to receive the two or more data elements out-of-order.

17. The apparatus of claim 14, wherein the two or more source addresses are orthogonal or independent and non-contiguous in the memory.

18. The apparatus of claim 14, wherein the two or more data elements are copied to the gather result buffer out-of-order in a background mode without direction by the processor.

19. The apparatus of claim 14, wherein the logic comprises a transaction sequencer configured to track the gather result buffer and generate a vector complete signal when the gather result buffer is complete.

20. An apparatus comprising:

a processor configured to provide two or more source addresses and corresponding two or more destination addresses of a memory; and

logic configured to copy two or more data elements from the two or more source addresses to corresponding two or more destination addresses within the memory, without an intermediate copy to a register in a processor.

21. The apparatus of claim 20, wherein the two or more source addresses are orthogonal or independent and non-contiguous.

22. The apparatus of claim 20, wherein the two or more destination addresses are orthogonal or independent and non-contiguous in the memory.

23. The apparatus of claim 20, comprising logic configured to copy the two or more data elements from the two or more source addresses to corresponding two or more destination addresses in a background mode without direction by the processor.