



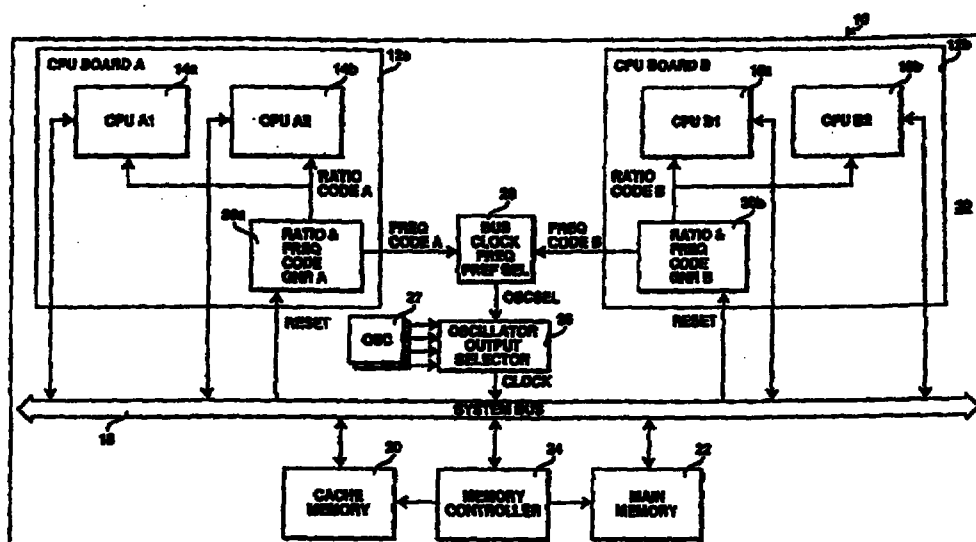
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(54) Title: METHOD AND APPARATUS FOR SELECTING AN OPTIMAL SYSTEM BUS CLOCK IN A HIGHLY SCALABLE COMPUTER SYSTEM

**(57) Abstract**

An oscillator output selector (26) and complementary control circuitry (28) are provided to a computer system. The oscillator output selector (26) is used to select a series of clock pulses for usage as a system bus clock. The control circuitry (28) controls the selection being made by the oscillator output selector, in accordance to control inputs received. In one embodiment, the control circuitry receives system bus clock frequency preferences from the CPU boards (12a-12b) as control inputs, and in response, the control circuitry causes the oscillator output selector to select the series of clock pulses having a frequency that is equal to or slower than the slowest preferred frequency. In an alternate embodiment, the control circuitry receives CPU types from the CPU boards as control inputs, and in response, the control circuitry causes the oscillator output selector to select a series of clock pulses having a frequency that will allow maximum total CPU clock frequency utilization.