Claims

What is claimed:

1. A semiconductor device, comprising:

a plurality of semiconductor die;

an electrostatic discharge (ESD) protection layer disposed ~~over~~on a first surface of the semiconductor die and ~~around~~ side surfaces of the semiconductor die, the ESD protection layer being discontinuous and electrically isolated between the semiconductor die;

an encapsulant deposited over the semiconductor die to completely enclose the ESD protection layer on the side surfaces of the semiconductor die; and

an interconnect structure formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die, the ESD protection layer being electrically connected to the interconnect structure to provide an ESD path.

2. The semiconductor device of claim 1, wherein the ESD protection layer includes:

an insulating layer formed over the first surface of the semiconductor die and around the side surfaces of the semiconductor die; and

a conductive layer formed over the insulating layer.

3. The semiconductor device of claim 1, wherein the ESD protection layer includes an encapsulant film, conductive polymer, or conductive ink formed over the first surface of the

semiconductor die and around the side surfaces of the semiconductor die.

4. The semiconductor device of claim 1, further including a conductive via formed through the encapsulant.

5. The semiconductor device of claim 1, further including a plurality of stacked semiconductor die covered by the ESD protective layer.

6. A semiconductor device, comprising:

a plurality of semiconductor die;

an electrostatic discharge (ESD) protection layer disposed over a first surface of the semiconductor die and ~~around~~on side surfaces of the semiconductor die, the ESD protection layer being discontinuous between the semiconductor die; and

an encapsulant deposited over the semiconductor die to enclose the ESD protection layer.

7. The semiconductor device of claim 6, further including an interconnect structure formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die.

~~8~~13. The semiconductor device of claim 7, wherein the ESD protection layer is electrically connected to the interconnect structure to provide an ESD path.

~~9~~8. The semiconductor device of claim 6, wherein the ESD protection layer includes:

an insulating layer; and

a conductive layer formed over the insulating layer.

~~10~~9. The semiconductor device of claim 6, wherein the ESD protection layer includes:

an insulating layer formed over the first surface of the semiconductor die and around the side surfaces of the semiconductor die; and

a conductive layer formed over the insulating layer.

1~~1~~0. The semiconductor device of claim 6, wherein the ESD protection layer includes an encapsulant film, conductive polymer, or conductive ink formed over the first surface of the semiconductor die and around the side surfaces of the semiconductor die.

1~~2~~1. The semiconductor device of claim 6, further including a conductive via formed through the encapsulant.

1~~3~~2. The semiconductor device of claim 6, further including a plurality of stacked semiconductor die covered by the ESD protective layer and electrically connected.

14. A semiconductor device, comprising:

a first semiconductor die;

an electrostatic discharge (ESD) protection layer disposed over a first surface of the first semiconductor die and around side surfaces of the first semiconductor die;

an encapsulant deposited over the first semiconductor die to enclose the ESD protection layer around the side surfaces of the first semiconductor die; and

a conductive via formed through the encapsulant.

15. The semiconductor device of claim 14, further including an interconnect structure formed over the encapsulant and a second

surface of the first semiconductor die opposite the first surface of the first semiconductor die.

16~~9~~. The semiconductor device of claim 15, wherein the ESD protection layer is electrically connected to the interconnect structure to provide an ESD path.

17~~6~~. The semiconductor device of claim 14, wherein the ESD protection layer includes:

an insulating layer formed over the first surface of the first semiconductor die and around the side surfaces of the first semiconductor die; and

a conductive layer formed over the insulating layer.

18~~7~~. The semiconductor device of claim 14, wherein the ESD protection layer includes an encapsulant film, conductive polymer, or conductive ink formed over the first surface of the first semiconductor die and around the side surfaces of the first semiconductor die.

19~~8~~. The semiconductor device of claim 14, further including a second semiconductor die without the ESD protection layer disposed adjacent to or disposed over the first semiconductor die.

20. A semiconductor device, comprising:

a first semiconductor die;

an electrostatic discharge (ESD) protection layer disposed over a first surface of the first semiconductor die and around side surfaces of the first semiconductor die, the ESD protection layer terminating at the side surfaces of the first semiconductor die; and

an encapsulant deposited over the ~~first semiconductor die~~ ESD protection layer.

21. The semiconductor device of claim 20, further including an interconnect structure formed over the encapsulant and a second surface of the first semiconductor die opposite the first surface of the first semiconductor die.

2~~2~~5. The semiconductor device of claim 21, wherein the ESD protection layer is electrically connected to the interconnect structure to provide an ESD path.

2~~3~~2. The semiconductor device of claim 20, further including a conductive via formed through the encapsulant.

2~~4~~3. The semiconductor device of claim 20, wherein the ESD protection layer includes:

an insulating layer formed over the first surface of the first semiconductor die and around the side surfaces of the first semiconductor die; and

a conductive layer formed over the insulating layer.

2~~5~~4. The semiconductor device of claim 20, further including a second semiconductor die without the ESD protection layer disposed adjacent to or disposed over the first semiconductor die.