

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
05 June 2025 (05.06.2025)



(10) International Publication Number
WO 2025/117398 A1

(51) International Patent Classification:
H10D 30/67 (2025.01) *H10D 86/60* (2025.01)
H10D 30/01 (2025.01)

(74) Agent: WYNNEGAR, James D., Jr.; c/o EMD Millipore Corporation, 400 Summit Drive, Burlington, Massachusetts 01803 (US).

(21) International Application Number:
PCT/US2024/057213

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(22) International Filing Date:
25 November 2024 (25.11.2024)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/603,807 29 November 2023 (29.11.2023) US

(71) Applicant: VERSUM MATERIALS US, LLC [US/US];
8555 South River Parkway, Tempe, Arizona 85284 (US).

(72) Inventor: KOUSHAN, Foroozan Sarah; c/o EMD Millipore Corporation, 400 Summit Drive, Burlington, Massachusetts 01803 (US).

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT,

(54) Title: METHOD AND RELATED CIRCUIT FOR PROVIDING SUPPLEMENTAL DIELECTRIC MATERIAL

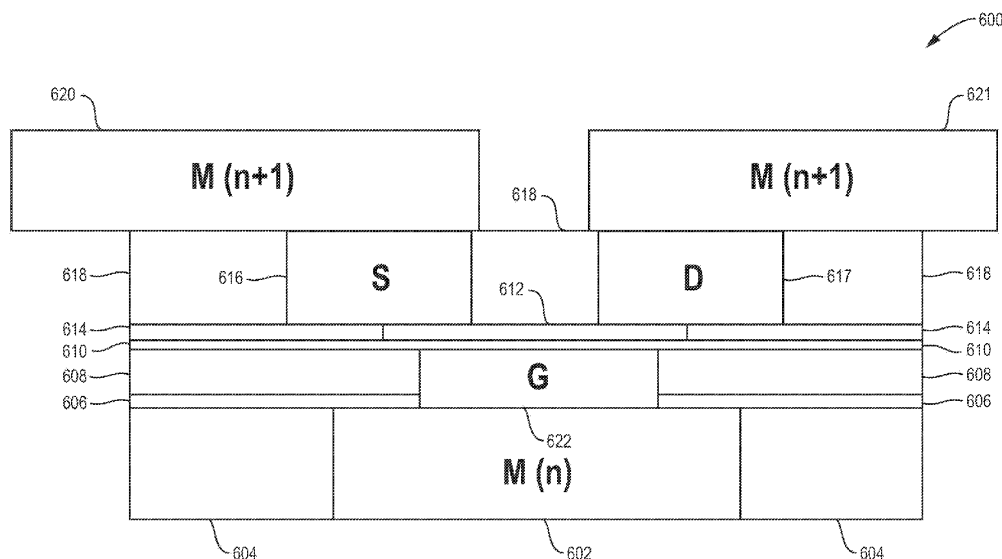


FIG. 6D

(57) Abstract: An integrated circuit, and related method, are provided herein. The integrated circuit may be formed on a die and consists of several components. These components include a first electrode, a dielectric layer placed on the first electrode, an active layer positioned on top of the dielectric layer, and finally, a supplemental layer located next to the active layer. The method may include forming a dielectric layer, forming an active layer on the dielectric layer, and/or forming a supplemental dielectric layer on the dielectric layer.

[Continued on next page]

WO 2025/117398 A1

LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE,
SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN,
GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*