REPLACEMENT SHEETS

CLEAN CLAIMS

1. A host controller, comprising:
an interface to access one or more registers within the host controller;
a processing circuit, within the host controller, coupled to the interface and adapted to
set an error register upon detection, by host controller hardware, of an error condition in the processing of tasks;
halt task execution or processing of tasks by the host controller hardware;
resume execution or processing of tasks, by the host controller hardware, upon detection that the error condition has been cleared by a host software.

2. The host controller of claim 1, wherein the processing circuit is further adapted to
process one or more tasks from a task queue, and
monitor for error conditions while processing the tasks.

3. The host controller of claim 1, wherein the processing circuit is further adapted to
poll the error register to ascertain whether the error condition has been cleared by the host controller hardware.

4. The host controller of claim 1, wherein the host controller halts execution or processing tasks upon finishing one of a current task, a current command, and a current instruction.

5. The host controller of claim 1, wherein the error register is located in a shared register space accessible to error handling software external to the host controller.

6. The host controller of claim 1, wherein the error condition is cleared by an external error handling software.

7. The host controller of claim 1, wherein halting task execution or processing of tasks includes stopping hardware operations in known location or state upon finishing one of a current task, a current command, and a current instruction.

8. A method operational at a host controller, comprising:

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setting an error register upon detection, by host controller hardware, of an error condition in the processing of tasks by a processing circuit;

halting, by the host controller hardware, task execution or processing of tasks by the processing circuit; and

resuming execution or processing of tasks, by the host controller hardware, upon detection that the error condition has been cleared by a host software operating at the processing circuit.

9. The method of claim 8, further comprising:
processing one or more tasks from a task queue; and
monitoring for error conditions while processing the tasks.

10. The method of claim 8, further comprising:
polling the error register to ascertain whether the error condition has been cleared.

11. The method of claim 8, wherein the host controller halts execution or processing tasks upon finishing one of a current task, a current command, and a current instruction.

12. The method of claim 8, wherein the error register is located in a shared register space accessible to error handling software external to the host controller.

13. The method of claim 8, further comprising:
instructing an external target device with which the host controller communicates to clear some or all task in the external target device.

14. A non-transitory processor-readable storage medium having one or more instructions which, when executed by at least one host controller, cause the at least one host controller to:

set an error register upon detection, by host controller hardware, of an error condition in the processing of tasks by a processing circuit;

halt, by host controller hardware, task execution or processing of tasks by the processing circuit; and

resume execution or processing of tasks, by host controller hardware, upon detection that the error condition has been cleared by a host software operating at the processing circuit.

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15. The storage medium of claim 14, wherein the one or more instructions further cause the at least one processing circuit to:

process one or more tasks from a task queue; and

monitor for error conditions while processing the tasks.

16. The storage medium of claim 14, wherein the one or more instructions further cause the at least one processing circuit to:

poll the error register to ascertain whether the error condition has been cleared.

17. A host device, comprising:

one or more registers including an error register;

a host controller including hardware configured to detect an error in task execution or processing of tasks and set the error register when such error is detected;

a processing circuit coupled to the host controller and the one or more registers and executing a host software, wherein the host software is adapted to perform error handling on the host controller by

polling, by the host software, the error register to ascertain whether an error has been set by the host controller;

performing error handling, by the host software, upon detection that the error register has been set; and

clearing, by a host software, the error register upon completion of error handling.

18. The host device of claim 17, wherein the processing circuit and host controller are integrated into a single semiconductor device.

19. The host device of claim 17, wherein at least one of the host software and host controller further performs at least one of:

clearing all task pending on a task queue of the host device;

clearing specific tasks pending on the task queue of the host device; and

instructing an external target device with which the host controller communicates to clear some or all task in the target device.

20. A method performed by a host software on a host device, comprising:

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polling, by the host software, an error register to ascertain whether an error has been set, at a hardware level, by a processing circuit of a host controller;

performing error handling, by the host software, upon detection that the error register has been set by the processing circuit; and

clearing, by the host software, the error register upon completion of error handling by the processing circuit.

21. The method of claim 20, further comprising:

clearing all task pending on a task queue of the host device;

clearing specific tasks pending on the task queue of the host device; and

instructing an external target device with which the host controller communicates to clear some or all task in the target device.

22. A host device, comprising:

a processing circuit executing a host software;

a host controller coupled to the processing circuit, wherein the host controller and host software are adapted to:

detecting, at a hardware level, an error condition at the host controller;

setting an error interrupt or register, at the hardware level, by the host controller;

halting task execution or processing by the host controller;

detecting an error condition at the host software as a result of the host controller having set the error interrupt or register;

performing error handling by at least one of the host software and host controller;

clearing the error condition by the host software; and

resuming execution or processing of tasks at the host controller upon detecting that error condition has been cleared by the host software.

23. The host device of claim 22, wherein the host controller and host software have access to a shared register space including the error interrupt or register.

24. The host device of claim 22, further comprising:

checking registers, by the host software, to ascertain details of the error condition.

25. A method operational on a host device, comprising:

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detecting, at a hardware level, an error condition at a host controller by a processing circuit;

setting an error interrupt or register, at the hardware level, at the host controller by the processing circuit;

halting task execution or processing at the host controller by the processing circuit;

detecting an error condition at a host software as a result of the host controller having set the error interrupt or register;

performing error handling by at least one of the host software and host controller;

clearing the error condition by the host software; and

resuming execution or processing of tasks at the host controller upon detecting that error condition has been cleared by the host software.

26. The method of claim 25, wherein at least one of the host software and host controller further performs at least one of:

clearing all task pending on a task queue of the host device;

clearing specific tasks pending on the task queue of the host device; and

instructing a target device with which the host controller communicates to clear some or all task in the target device.

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CLAIMS

1. A host controller, comprising:

an interface to access one or more registers;

a processing circuit coupled to the interface and adapted to

set an error register upon detection, by host controller hardware, of an error condition in the processing of tasks;

halt task execution or processing of tasks by host controller hardware;

resume execution or processing of tasks, by host controller hardware, upon detection that the error condition has been cleared by a host software operating at the processing circuit.

2. The host controller of claim 1, wherein the processing circuit is further adapted to

process one or more tasks from a task queue; and

monitor for error conditions while processing the tasks.

3. The host controller of claim 1, wherein the processing circuit is further adapted to

poll the error register to ascertain whether the error condition has been cleared by the host controller software.

4. The host controller of claim 1, wherein the host controller halts execution or processing tasks upon finishing one of a current task, a current command, and a current instruction.

5. The host controller of claim 1, wherein the error register is located in a shared register space accessible to error handling software external to the host controller.

6. The host controller of claim 1, wherein the error condition is cleared by an external error handling software.

7. The host controller of claim 1, wherein halting task execution or processing of tasks includes stopping hardware operations in known location or state upon finishing one of a current task, a current command, and a current instruction.

8. A method operational at a host controller, comprising:

setting an error register upon detection, by host controller hardware, of an error condition in the processing of tasks by a processing circuit;

halting, by the host controller hardware, task execution or processing of tasks by the processing circuit; and

resuming execution or processing of tasks, by the host controller hardware, upon detection that the error condition has been cleared by a host software operating at the processing circuit.

9. The method of claim 8, further comprising:

processing one or more tasks from a task queue; and

monitoring for error conditions while processing the tasks.

10. The method of claim 8, further comprising:

polling the error register to ascertain whether the error condition has been cleared by the host controller software.

11. The method of claim 8, wherein the host controller halts execution or processing tasks upon finishing one of a current task, a current command, and a current instruction.

12. The method of claim 8, wherein the error register is located in a shared register space accessible to error handling software external to the host controller.

13. The method of claim 8, further comprising:

instructing an external target device with which the host controller communicates to clear some or all task in the external target device.

14. A non-transitory processor-readable storage medium having one or more instructions which, when executed by at least one processing circuit, cause the at least one processing circuit to:

set an error register upon detection, by host controller hardware, of an error condition in the processing of tasks by a processing circuit;

halt, by the host controller hardware, task execution or processing of tasks by the processing circuit; and

resume execution or processing of tasks, by the host controller hardware, upon detection that the error condition has been cleared by a host software operating at the processing circuit.

15. The storage medium of claim 14, wherein the one or more instructions further cause the at least one processing circuit to:

process one or more tasks from a task queue; and

monitor for error conditions while processing the tasks.

16. The storage medium of claim 14, wherein the one or more instructions further cause the at least one processing circuit to:

poll the error register to ascertain whether the error condition has been cleared.

17. A host device, comprising:

one or more registers including an error register;

a host controller including hardware configured to detect an error in task execution or processing of tasks and set the error register when such error is detected;

a processing circuit coupled to the host controller and the one or more registers and executing a host software, wherein the host software is adapted to perform error handling on the host controller by

polling, by the host software, the error register to ascertain whether an error has been set by the host controller;

performing error handling, by the host software, upon detection that the error register has been set; and

clearing, by a host software, the error register upon completion of error handling.

18. The host device of claim 17, wherein the processing circuit and host controller are integrated into a single semiconductor device.

19. The host device of claim 17, wherein at least one of the host software and host controller further performs at least one of:

clearing all task pending on a task queue of the host device;

clearing specific tasks pending on the task queue of the host device; and

instructing an external target device with which the host controller communicates to clear some or all task in the target device.

20. A method performed by a host software on a host device, comprising:

polling, by the host software, an error register to ascertain whether an error has been set, at a hardware level, by a processing circuit of a host controller;

performing error handling, by the host software, upon detection that the error register has been set by the processing circuit; and

clearing, by the host software, the error register upon completion of error handling by the processing circuit.

21. The method of claim 20, further comprising:

clearing all task pending on a task queue of the host device;

clearing specific tasks pending on the task queue of the host device; and

instructing an external target device with which the host controller communicates to clear some or all task in the target device.

22. A host device, comprising:

a processing circuit executing a host software;

a host controller coupled to the processing circuit, wherein the host controller and host software are adapted to:

detect, at a hardware level, an error condition at the host controller;

set an error interrupt or register, at the hardware level, by the host controller;

halt task execution or processing by the host controller;

detect an error condition at the host software as a result of the host controller having set the error interrupt or register;

perform error handling by at least one of the host software and host controller;

clear the error condition by the host software; and

resume execution or processing of tasks at the host controller upon detecting that error condition has been cleared by the host software.

23. The host device of claim 22, wherein the host controller and host software have access to a shared register space including the error interrupt or register.

24. The host device of claim 22, further comprising:

checking registers, by the host software, to ascertain details of the error condition.

25. A method operational on a host device, comprising:

detecting, at a hardware level, an error condition at a host controller by a processing circuit;

setting an error interrupt or register, at the hardware level, at the host controller by the processing circuit;

halting task execution or processing at the host controller by the host controller;

detecting an error condition at a host software as a result of the host controller having set the error interrupt or register;

performing error handling by at least one of the host software and host controller;

clearing the error condition by the host software; and

resuming execution or processing of tasks at the host controller upon detecting that error condition has been cleared by the host software.

26. The method of claim 25, wherein at least one of the host software and host controller further performs at least one of:

clearing all task pending on a task queue of the host device;

clearing specific tasks pending on the task queue of the host device; and

instructing a target device with which the host controller communicates to clear some or all task in the target device.