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(54) Title: TEST CIRCUIT FOR AN UNPROGRAMMED OTP MEMORY ARRAY

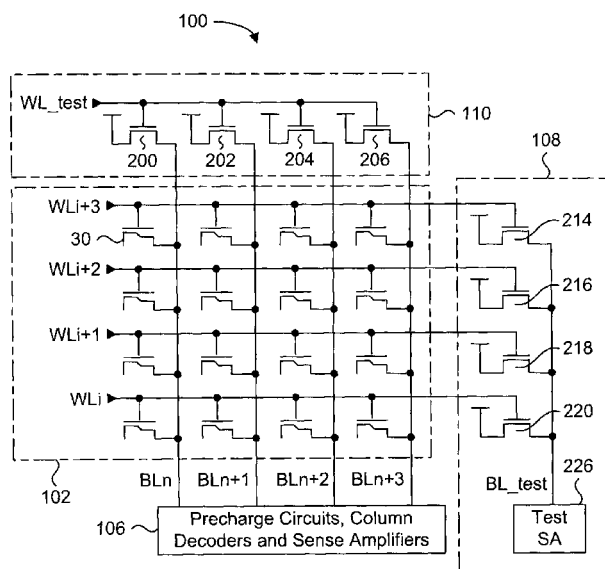


FIG. 8

(57) Abstract: Circuits for testing unprogrammed OTP memories to ensure that wordline and bitline connections, column decoders, wordline drivers, correctness of decoding, sensing and multiplexing operate properly. The OTP testing system includes one or both of column test circuitry and row test circuitry. The column test circuitry charges all the bitlines to a voltage level similar to that provided by a programmed OTP memory cell during a read operation, in response to activation of a test wordline. The bitline voltages can be sensed, thereby allowing for testing of the column decoding and sense amplifier circuits. The row test circuitry charges a test bitline to a voltage level similar to that provided by a programmed OTP memory cell during a read operation, in response to activation of a wordline of the OTP memory array. This test bitline voltage can be sensed, thereby allowing for testing of the row decoding and driver circuits.



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