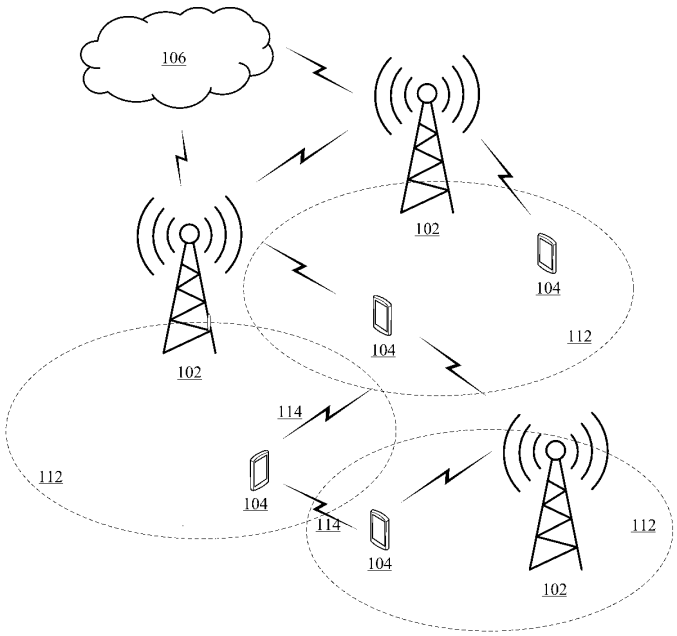

Figure 1

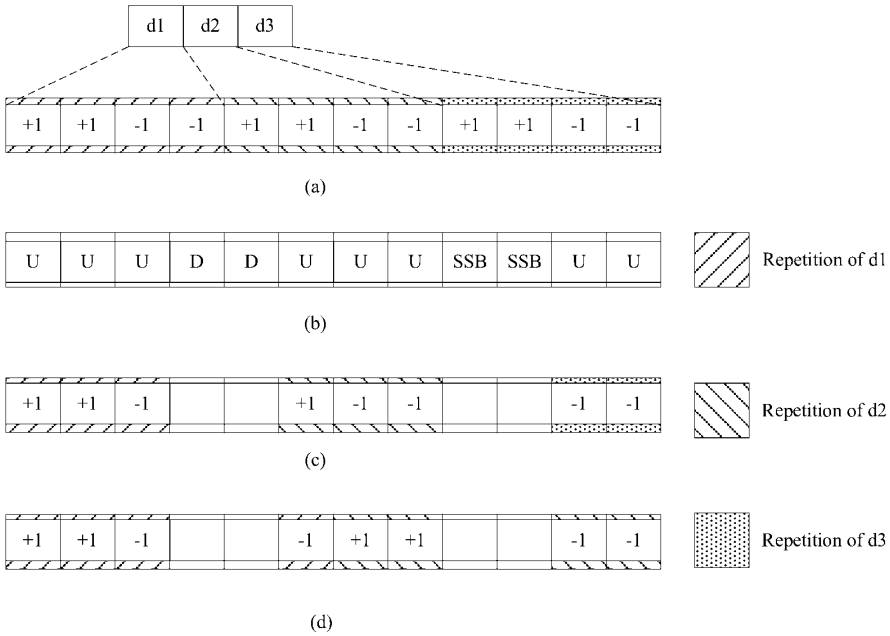

Figure 2

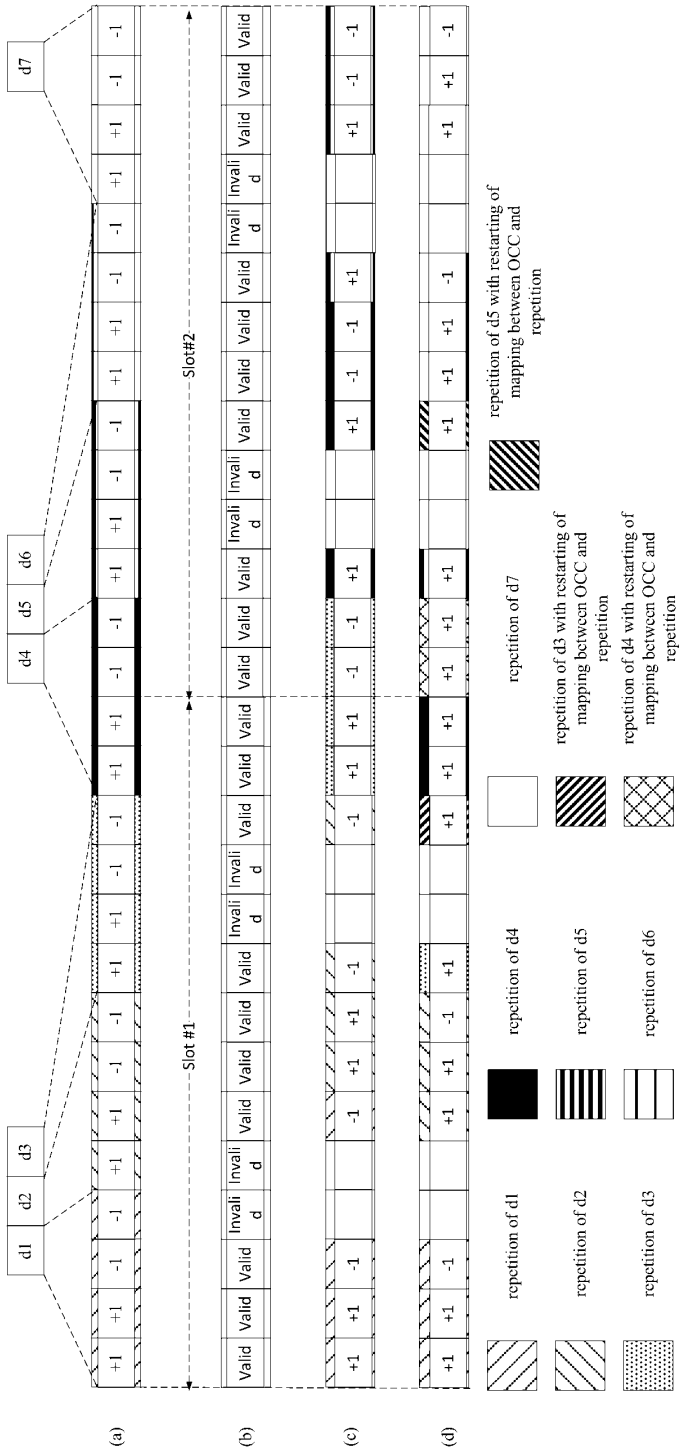
d1
d2
d3
d4
d5
d6
d7
Slot #1
Slot#2
(a)
(b)
(c)
(d)
repetition of d1
repetition of d2
repetition of d3
repetition of d4
repetition of d5
repetition of d6
repetition of d7
repetition of d3 with restarting of mapping between OCC and repetition
repetition of d4 with restarting of mapping between OCC and repetition
repetition of d5 with restarting of mapping between OCC and repetition

Figure 3

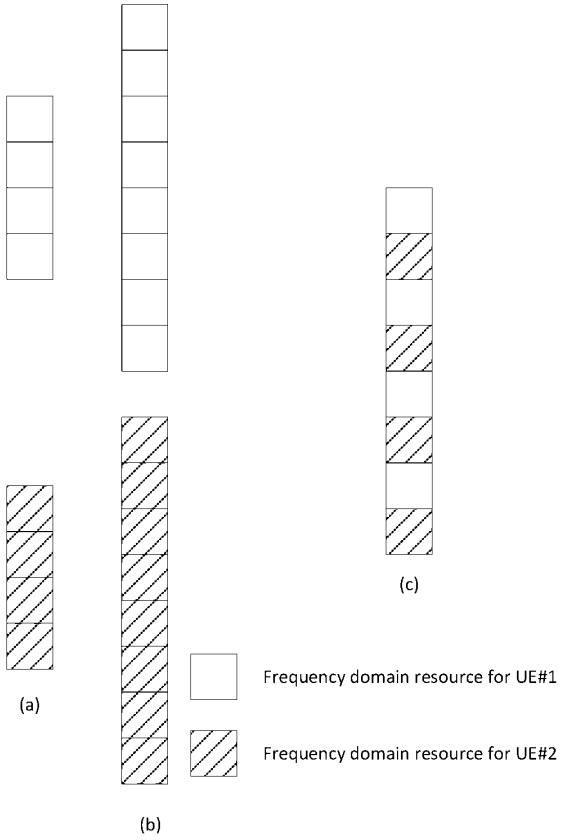
(a)
(b)
(c)
Frequency domain resource for UE#1
Frequency domain resource for UE#2

Figure 4

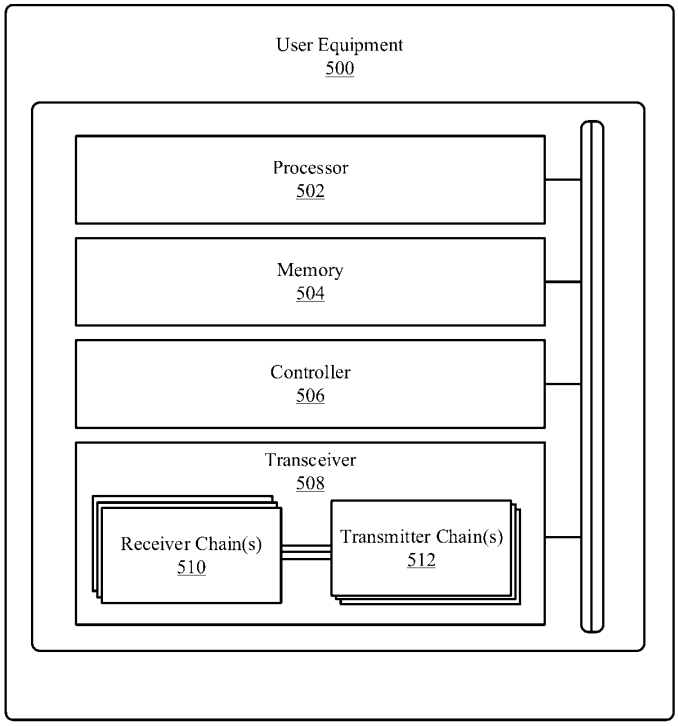

Figure 5

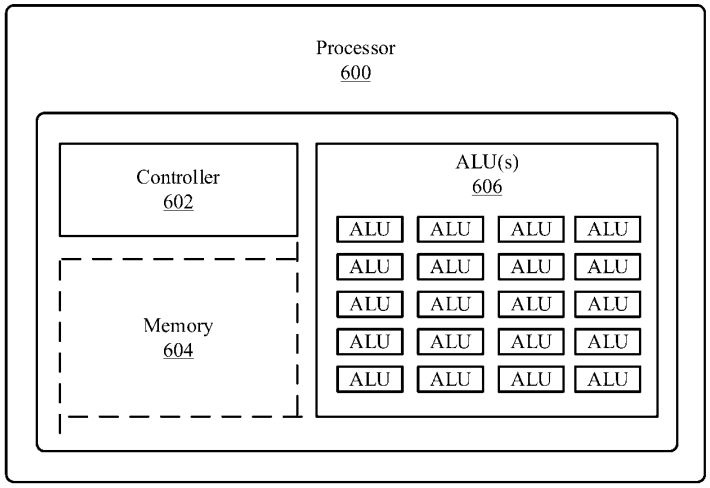

Figure 6

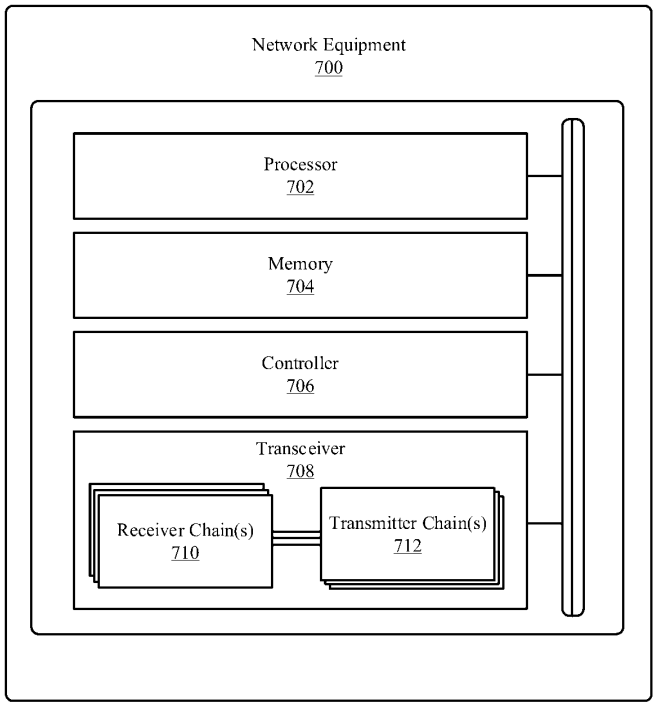
Network Equipment
700
Processor
702
Memory
704
Controller
706
Transceiver
708
Receiver Chain(s)
710
Transmitter Chain(s)
712

Figure 7

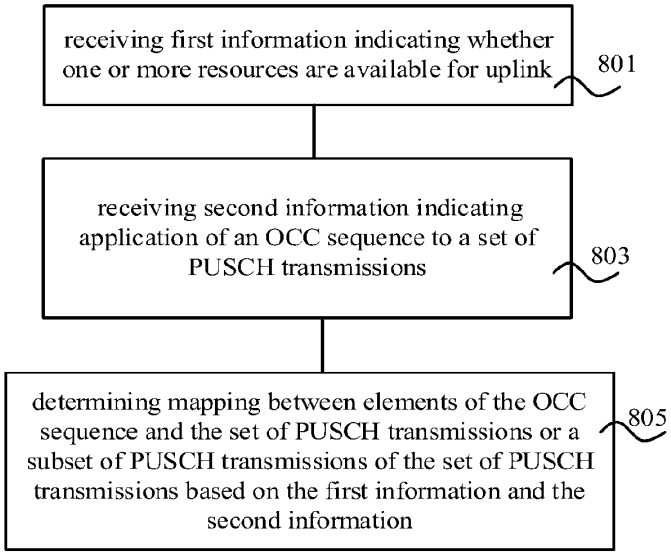

Figure 8

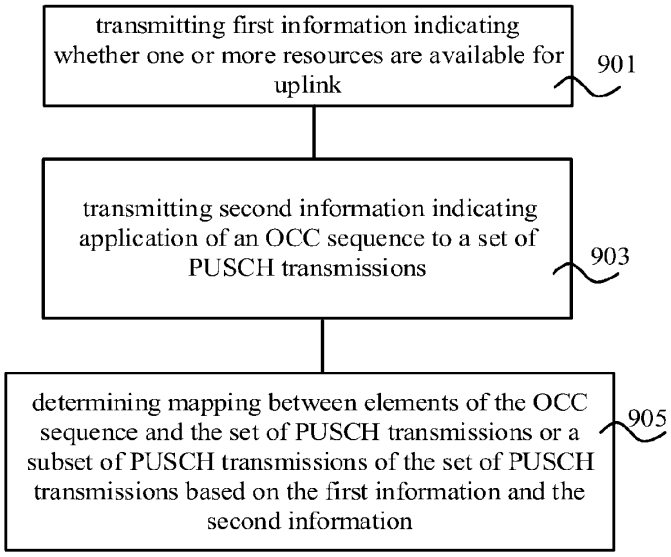

Figure 9