In1255DE

Abstract

Integrated circuit arrangement having capacitors and having preferably planar transistors and fabrication method

An explanation is given, inter alia, of an integrated circuit arrangement (140), which contains a preferably planar transistor (142) and a capacitor (144). The bottom electrode of the capacitor (144) is arranged together with a channel region of the transistor (142) in an SOI substrate. The circuit arrangement (140) is simple to fabricate and has outstanding electronic properties.

(Figure 13)



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