

IMAGE SENSOR, CONTROL METHOD, AND ELECTRONIC DEVICE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priorities of Chinese Patent Applications No.
5 201510964086.4, 201510963291.9, 201510963293.8, and 201510960708.6, filed
December 18, 2015. The entire disclosures of the above applications are incorporated
herein by reference.

BACKGROUND

Field

10 [0002] The present disclosure relates to imaging technique, and more particularly
to an image sensor, a control method, and an electronic device.

Background

[0003] As mobile phones are becoming more and more popular, more and more
people are interested in taking photos using the mobile phones. However, people are
15 placing more demands in taking the photos. Good quality low-light photos have
become an urgent demand of consumers, and thus sensors require a higher sensitivity
and a better signal-to-noise ratio. However, the sensitivity and the signal-to-noise ratio
of current image sensors need to be improved further.

SUMMARY OF THE DISCLOSURE

20 [0004] The present disclosure is intended to solve at least one of the technical
problems in the related art to a certain extent. To this end, the present disclosure
requires providing an image sensor, a control method, and an electronic device.

[0005] An image sensor in accordance with an embodiment of the present
disclosure includes a light sensing array; a light filtering array disposed on the light
25 sensing array, wherein each of light filtering units correspondingly covers one of light
sensing units, and each of the light sensing units comprises a plurality of light sensing
pixels; and a plurality of conversion units, wherein each of the conversion units

includes at least two source followers, and at least one of the at least two source followers is connected to a plurality of the light sensing pixels.

[0006] In some embodiments, the light filtering array includes a Bayer array.

5 **[0007]** In some embodiments, each of the light sensing units includes 2x2 light sensing pixels.

[0008] In some embodiments, each of the conversion units includes two source followers, one of the source followers is connected to two of the light sensing pixels in a first row, and the other one of the source followers is connected to two of the light sensing pixels in a second row.

10 **[0009]** In some embodiments, the image sensor further includes a plurality of analog-to-digital conversion units, and one of the analog-to-digital conversion units is connected to the two source followers.

[0010] In some embodiments, the image sensor further includes:

15 **[0011]** A plurality of clock switches, wherein each of the clock switches is connected to one of the light sensing pixels;

[0012] A plurality of reset switches, wherein the two of the light sensing pixels in the first row is connected to one of the reset switches, and the two of the light sensing pixels in the second row is connected to the other one of the reset switches; and

20 **[0013]** A plurality of readout switches, wherein each of the readout switches is connected to one of the source followers.

[0014] In some embodiments, each of the conversion units includes two source followers, one of the source followers is connected to three of the light sensing pixels, and the other one of the source followers is connected to a remaining one of the light sensing pixels.

25 **[0015]** In some embodiments, the image sensor further includes a plurality of analog-to-digital conversion units, and each of the analog-to-digital conversion units is connected to one of the source followers.

[0016] In some embodiments, the image sensor further includes:

[0017] A plurality of clock switches, wherein each of the clock switches is connected to one of the light sensing pixels;

[0018] A plurality of reset switches, wherein the three of the light sensing pixels to which the one of the source followers is connected are connected to one of the reset switches, and the remaining one of the light sensing pixels to which the other one of the source followers is connected is connected to the other one of the reset switches; and

[0019] A plurality of readout switches, wherein the one of the source followers connected to the three of the light sensing pixels is connected to one of the readout switches, and the other one of the source followers connected to the remaining one of the light sensing pixels is connected to the other one of the readout switches.

[0020] In some embodiments, each of the conversion units includes three source followers, one of the source followers is connected to two of the light sensing pixels in one column, and the other two of the source followers are respectively connected to remaining two of the light sensing pixels.

[0021] In some embodiments, the image sensor of further includes a plurality of analog-to-digital conversion units, the source follower connected to the two of the light sensing unit in the one column is connected to one of the analog-to-digital conversion units, and the two source follower respectively connected to the remaining two of the light sensing units are connected to the other one of the analog-to-digital conversion units.

[0022] In some embodiments, the image sensor further includes:

[0023] A plurality of clock switches, wherein each of the clock switches is connected to one of the light sensing pixels;

[0024] A plurality of reset switches, wherein the two of the light sensing pixels in the one column to which the one of the source followers is connected are connected to one of the reset switches, and the remaining two of the light sensing pixels are connected to respective ones of the reset switches; and

[0025] A plurality of readout switches, wherein the one of the source followers connected to the two of the light sensing pixels in the one column is connected to one of the readout switches, and the other two of the source followers respectively connected to the remaining two of the light sensing pixels is connected to the other
5 one of the readout switches.

[0026] In some embodiments, each of the conversion units includes three source followers, one of the source followers is connected to two of the light sensing pixels in one row, and the other two of the source followers are respectively connected to remaining two of the light sensing pixels.

10 **[0027]** In some embodiments, the image sensor further includes a plurality of analog-to-digital conversion units, and one of the analog-to-digital conversion units is connected to the three source followers.

[0028] In some embodiments, the image sensor further includes:

[0029] A plurality of clock switches, wherein each of the clock switches is
15 connected to one of the light sensing pixels;

[0030] A plurality of reset switches, wherein the two of the light sensing pixels in the one row to which the one of the source followers is connected are connected to one of the reset switches, and the other two of the light sensing pixels are connected to respective ones of the reset switches; and

20 **[0031]** A plurality of readout switches, wherein the one of the source followers connected to the two of the light sensing pixels in the one row is connected to one of the readout switches, and the other two of the source followers connected to the other two of the light sensing pixels is connected to the other one of the readout switches.

[0032] A control method in accordance with an embodiment of the present
25 disclosure is configured to control an image sensor. The image sensor includes a light sensing array, a light filtering array, and a plurality of conversion units. The light sensing array is disposed on the light sensing array. Each of light filtering units correspondingly covers one of light sensing units. Each of the light sensing units includes a plurality of light sensing pixels. Each of the conversion units includes at

least two source followers. At least one of the at least two source followers is connected to a plurality of the light sensing pixels. The image sensor further includes a plurality of clock switches configured to control the light sensing pixels to be exposed, a plurality of reset switches configured to reset the light sensing pixels, and a plurality of readout switches configured to control readouts of the light sensing pixels.
5 The control method includes:

[0033] Controlling the clock switches, the reset switches, and the readout switches to read two image frames; and

[0034] Synthesizing the two image frames to acquire a high dynamic range image.
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[0035] In some embodiments, controlling the clock switches, the reset switches, and the readout switches to read the two image frames includes:

[0036] Controlling the reset switches to reset the light sensing pixels;

[0037] Controlling the clock switches, so that two adjacent rows of the light sensing pixels are exposed synchronously; and
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[0038] Controlling timing sequences of the readout switches to read an output of each of the source followers to read the two image frames.

[0039] In some embodiments, controlling the clock switches, the reset switches, and the readout switches to read the two image frames includes:

[0040] Converting analog signals outputted by the source followers into digital signals.
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[0041] In some embodiments, an electronic device includes any one of the above-mentioned image sensors.

[0042] In some embodiments, the electronic device includes a mobile phone or a tablet computer.
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[0043] In some embodiments, the electronic device further includes a central processing unit connected to the image sensor and a display device. The central

processing unit is configured to control the display device to display an image outputted by the image sensor.

[0044] An electronic device in accordance with an embodiment of the present disclosure includes a case, a processor, a storage device, a circuit board, and a power
5 circuit. The circuit board is disposed in a space surrounded by the case. The processor and the storage device are disposed on the circuit board. The power circuit is configured to providing power for each circuit and each device of the electronic device. The storage device is configured to store executable program codes. The processor executes programs corresponding to the executable program codes to
10 perform the control method of any one of claims 16-18.

[0045] In the image sensor, the control method, and the electronic device in accordance with the embodiments of the present disclosure, since each of the filtering units correspond to a plurality of the light sensing pixels and at least one of the source followers is connected to multiple light sensing pixels, the multiple light sensing
15 pixels can obtain more photoinduced charges when compared to an output of one light sensing pixel. Accordingly, by improving hardware, sensitivity and a signal-to-noise ratio can be increased, and outputs and readouts by controlling exposure of the light sensing pixels can synthesize a high dynamic range image.

[0046] Additional aspects and advantages of the present disclosure will be given
20 in the following description, and some will become apparent from the following description or learned by practice of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0047] FIG. 1 illustrates an image sensor in accordance with an embodiment of the present disclosure.

25 [0048] FIG. 2 illustrates a light filtering array in accordance with an embodiment of the present disclosure.

[0049] FIG. 3 illustrates a circuit diagram of the image sensor in accordance with some embodiments of the present disclosure.

[0050] FIG. 4 illustrates a circuit diagram of the image sensor in accordance with some embodiments of the present disclosure.

[0051] FIG. 5 illustrates a circuit diagram of the image sensor in accordance with some embodiments of the present disclosure.

5 [0052] FIG. 6 illustrates a circuit diagram of the image sensor in accordance with some embodiments of the present disclosure.

[0053] FIG. 7 illustrates a structural diagram of the image sensor in accordance with some embodiments of the present disclosure.

[0054] FIG. 8 illustrates a flowchart of a control method in accordance with an
10 embodiment of the present disclosure.

[0055] FIG. 9 illustrates a flowchart of the control method in accordance with some embodiments of the present disclosure.

[0056] FIG. 10 illustrates a functional block diagram of an electronic device in accordance with some embodiments of the present disclosure.

15 [0057] FIG. 11 illustrates a functional block diagram of an electronic device in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0058] Hereinafter, exemplary embodiments of the present disclosure will be described with reference to the accompanying drawings. The same or similar elements
20 or the elements with the same or similar functions will be designated by the same or similar reference numerals all through the following description and drawings. The following embodiments described with the accompanying drawings are merely exemplary to explain the present disclosure and not to be construed as limiting the present disclosure.

25 [0059] Please refer to FIG. 1. An image sensor 100 in accordance with an embodiment of the present disclosure includes a light filtering array 10, a light sensing array 20, and a plurality of conversion units 30.

[0060] The light filtering array 10 includes a plurality of light filtering units 11. The light filtering array 10 is disposed on the light sensing array 20. The light sensing array 20 includes a plurality of light sensing units 21. Each of the light sensing units 21 includes a plurality of light sensing pixels 22. Each of the light filtering units 11 correspondingly covers one of the light sensing units 21. That is, each of the light filtering units 11 correspondingly covers multiple light sensing pixels 22. Each of the conversion units 30 includes at least two source followers 31. At least one of the source followers 31 is connected to multiple light sensing pixels 22. The source followers 31 are configured to convert light generated by the light sensing pixels 22 into analog signals.

[0061] It may be understood that since at least one of the source followers 31 is connected to multiple light sensing pixels 22, photoinduced charges generated by the multiple light sensing pixels 22 corresponding to the same light filtering unit 11 output a plurality sets of analog signals according to a number of the source followers 31 and different connections. Compared to an output of one light sensing pixel 22, the multiple light sensing pixels 22 can obtain more photoinduced charges. Accordingly, by improving hardware, sensitivity and a signal-to-noise ratio can be increased, and outputs and readouts by controlling exposure of multiple light sensing pixels 22 can synthesize a high dynamic range image.

[0062] In some embodiments, the image sensor 100 includes a complementary metal oxide semiconductor (CMOS) image sensor.

[0063] Please refer to FIG. 2. The light filtering array 10 includes a Bayer array. The light filtering units 11 having the same color are represented by the same character, for example, Gr, Gb, R, or B. A numeral after the character represents a sequential number corresponding to a light sensing pixel 22 of the light filtering units 11 having the same color. The light filtering units 11 having different colors allow light, having corresponding wavelengths, to pass.

[0064] In some embodiments, the light sensing pixel 22 corresponding to each of the light filtering units 11 are positioned in different rows.

[0065] For example, in some embodiments, each of the light sensing units 21 includes 2x2 light sensing pixels 22. That is, each of the light filtering units 11 correspondingly covers four light sensing pixels 22 in two rows and two columns.

[0066] Please refer to FIG. 3. In some embodiments, each of the conversion units 30 includes two source followers 31. One of the source followers 31 is connected to two light sensing pixels 22 in a first row. The other one of the source followers 31 is connected to two light sensing pixels 22 in a second row.

[0067] As such, the photoinduced charges generated by the two light sensing pixels 22 in the first row are accumulated and converted into a first analog signal A1 by one of the source followers 31. The photoinduced charges generated by the two light sensing pixels 22 in the second row are accumulated and converted into a second analog signal A2 by the other one of the source followers 31.

[0068] Further, the image sensor 100 further includes a plurality of analog-to-digital conversion units 40. Each of the analog-to-digital conversion units 40 is connected to two source followers 31. Each of the analog-to-digital conversion units 40 is configured to convert the analog signals outputted by the source followers 31 into digital signals. In detail, in the present embodiment, the first analog signal A1 and the second analog signal A2 are respectively converted into a first digital signal D1 and a second digital signal D2 by one of the analog-to-digital conversion units 40.

[0069] Further, the image sensor 100 further includes a plurality of clock switches 50, a plurality of reset switches 60, and a plurality of readout switches 70. The clock switches 50 are configured to control the light sensing pixels 22 to be exposed. The reset switches 60 are configured to reset the light sensing pixels 22. The readout switches 70 are configured to control readouts of the light sensing pixels 22.

[0070] An equivalent circuit of one of the light sensing units 21 of the image sensor 100 is described as follows. The one of the light sensing units 21 includes light sensing pixels PD1-PD4, clock switches TG1-TG4, source followers SF1 and SF2, reset switches RST1 and RST2, and readout switches SEL1 and SEL2.

[0071] In detail, the light sensing pixels PD1-PD4 are arranged in a 2x2 array. The first light sensing pixel PD1, the second light sensing pixel PD2, the third light

sensing pixel PD3, and the fourth light sensing pixel PD4 are adjacent light sensing pixels and correspond to the same light filtering unit 11. That is, the four adjacent light sensing pixels receive the same color of light. In brief, the four light sensing pixels constitute a large pixel. The first light sensing pixel PD1 and the second light sensing pixel PD2 are positioned in the same row, and the third light sensing pixel PD3 and the fourth light sensing pixel PD4 are positioned in the same row. Each of the light sensing pixels is connected to one of the clock switches. That is, the first light sensing pixel PD1 is connected to the first clock switch TG1. The second light sensing pixel PD2 is connected to the second clock switch TG2. The third light sensing pixel PD3 is connected to the third clock switch TG3. The fourth light sensing pixel PD4 is connected to the fourth clock switch TG4.

[0072] Further, in the first row, the first light sensing pixel PD1 is connected to a first terminal of the source follower SF1 via the first clock switch TG1, and the second light sensing pixel PD2 is connected to the first terminal of the source follower SF1 via the second clock switch TG2. The first light sensing pixel PD1 is connected to a first terminal of the reset switch RST1 via the first clock switch TG1, and the second light sensing pixel PD2 is connected to the first terminal of the reset switch RST1 via the second clock switch TG2. A second terminal of the reset switch RST1 and a second terminal of the source follower SF1 are connected to a predetermined power source, e.g., Vdd. A third terminal of the source follower SF1 is connected to a first terminal of the readout switch SEL1.

[0073] Further, in the second row, connections of the third light sensing pixel PD3, the fourth light sensing pixel PD4, the corresponding clock switches TG3 and TG4, the reset switch RST2, the source follower SF2, and the readout switch SEL2 are similar to the connections of the first light sensing pixel PD1, the second light sensing pixel PD2, the corresponding clock switches TG1 and TG2, the reset switch RST1, the source follower SF1, and the readout switch SEL1 in the first row, and not repeated herein.

[0074] Further, second terminals of the readout switches SEL1 and SEL2 are connected to one of the analog-to-digital conversion units 40.

[0075] In order to implement control of an exposure, the image sensor 100 further includes a control module. Control terminals of the first clock switch TG1, the second clock switch TG2, the third clock switch TG3, and the fourth clock switch TG4 are connected to the control module. The control module controls turned-on and
5 turned-off of the four clock switches. When each of the four clock switches is turned on, the corresponding light sensing pixel starts to be exposed.

[0076] It is noted that before being exposed, the light sensing pixels have to be reset. That is, control terminals of the reset switches RST1 and RST2 are also connected to the control module and configured to reset the corresponding light
10 sensing pixels before the corresponding light sensing pixels are exposed or after exposing data is read.

[0077] During an exposure process, the first to fourth light sensing pixels PD1-PD4, for example, photodiodes, receive the light passing through the corresponding one of the light filtering units and generate charge. The clock switches
15 TG1-TG4 are turned on, and the charges generated by the corresponding light sensing pixels are outputted. The charges are converted into analog signals by the source followers SF1 and SF2, and the analog signals are converted into digital signals by the corresponding one of the analog-to-digital conversion units. The digital signals are outputted for providing a data basis of image processing.

20 **[0078]** The control module controls the light sensing pixels 22 corresponding to the same one of the light filtering units 11 to be exposed synchronously row by row, and controls exposing time, so as to implement the control of the exposure.

[0079] As an example, two light sensing pixels corresponding to each of the light filtering units 11 in the $(2i+1)$ th row ($i=0, 1, 2, 3, 4, \dots$) of the light sensing array 20
25 (e.g., the light sensing pixels corresponding to the light filtering units Gr1 and Gr2), that is, the first light sensing pixel PD1 and the second light sensing pixel PD2 share the source follower SF1. The charges generated by the first light sensing pixel PD1 and the second light sensing pixel PD2 are collected, and the collected charges are converted into the analog signals by the source follower SF1. The analog signals are
30 converted into the digital signals by the analog-to-digital conversion unit 40 and outputted. It is assumed that an output value of the analog-to-digital conversion unit

40 is ADC1. Further, two light sensing pixels corresponding to each of the light filtering units 11 in the $(2i+2)$ th row ($i=0, 1, 2, 3, 4, \dots$) of the light sensing array 20 adjacent to the $(2i+1)$ th row (e.g., the light sensing pixels corresponding to the light filtering units Gr3 and Gr4), that is, the third light sensing pixel PD3 and the fourth light sensing pixel PD4 share the source follower SF2. The charges generated by the third light sensing pixel PD3 and the fourth light sensing pixel PD4 are collected, and the collected charged are converted into the analog signals by the source follower SF2. The analog signals are converted into the digital signals by the analog-to-digital conversion unit 40 and outputted. It is assumed that an output value of the analog-to-digital conversion unit 40 is ADC2.

[0080] When a photo is taken, the control module controls two adjacent rows of the light sensing units to be exposed synchronously. For example, the $(2i+1)$ th and the $(2i+2)$ th rows ($i=0, 1, 2, 3, 4, \dots$) of the light sensing units are exposed synchronously. The exposing time is controlled to avoid that the two light sensing units 22 sharing the same source follower have saturation outputs. In the embodiment of the present disclosure, each source follower 31 can collect the charges by the two light sensing units 22 that are connected to the source follower 31. It can be understood that the charge amount collected by or the analog signals converted by the source follower SF1 or the source follower SF2 is a sum of the charges generated by the two corresponding light sensing units 22 and approximately double of the charges generated by one of the two light sensing units 22. After the readout switches SEL1 and SEL2 are controlled to be turned on simultaneously, an output value of the analog-to-digital conversion unit 40 is an average value of the values outputted by the source followers SF1 and SF2. That is, compared to one light sensing unit 22, the charges generated by the four light sensing units 22 corresponding to the same one of the light filtering units 11 are increasing, thereby improving the sensitivity of the image sensor 100 (approximately double).

[0081] Please refer to FIG. 4. In some embodiments, each of the conversion units 30 includes two source followers 31. One of the source followers 31 is connected to three light sensing pixels 22 of one of the light sensing units 21. The other one of the source followers 31 is connected to a remaining one light sensing pixel 22 of the one of the light sensing units 21.

[0082] For example, photoinduced charges generated by the three light sensing pixels 22 including two light sensing pixels 22 in a first row and a light sensing pixel 22 in a second row are accumulated and converted into a first analog signal A1 by one of the source followers 31. Photoinduced charges generated by the other one of the light sensing pixels 22 in the second row are accumulated and converted into a second analog signal A2 by the other one of the source followers 31.

[0083] Further, the image sensor 100 further includes a plurality of analog-to-digital conversion units 40. Each of the analog-to-digital conversion units 40 is connected to one of the source followers 31. That is, each of the light sensing units 21 is connected to two analog-to-digital conversion units 40. Each of the analog-to-digital conversion units 40 is configured to convert the analog signals outputted by the source followers 31 into digital signals. In detail, in the present embodiment, the first analog signal A1 is converted into a first digital signal D1 by one of the analog-to-digital conversion units 40, and the second analog signal A2 is converted into a second digital signal D2 by the other one of the analog-to-digital conversion units 40.

[0084] Further, the image sensor 100 further includes a plurality of clock switches 50, a plurality of reset switches 60, and a plurality of readout switches 70. The clock switches 50 are configured to control the light sensing pixels 22 to be exposed. The reset switches 60 are configured to reset the light sensing pixels 22. The readout switches 70 are configured to control readouts of the light sensing pixels 22.

[0085] An equivalent circuit of one of the light sensing units 21 of the image sensor 100 is described as follows. The one of the light sensing units 21 includes light sensing pixels PD1-PD4, clock switches TG1-TG4, source followers SF1 and SF2, reset switches RST1 and RST2, and readout switches SEL1 and SEL2.

[0086] In detail, the light sensing pixels PD1-PD4 are arranged in a 2x2 array. The first light sensing pixel PD1, the second light sensing pixel PD2, the third light sensing pixel PD3, and the fourth light sensing pixel PD4 are adjacent light sensing pixels and correspond to the same light filtering unit 11. That is, the four adjacent light sensing pixels receive the same color of light. In brief, the four light sensing pixels constitute a large pixel. The first light sensing pixel PD1 and the second light

sensing pixel PD2 are in the same row, and the third light sensing pixel PD3 and the fourth light sensing pixel PD4 are in the same row. Each of the light sensing pixels is connected to one of the clock switches. That is, the first light sensing pixel PD1 is connected to the first clock switch TG1. The second light sensing pixel PD2 is connected to the second clock switch TG2. The third light sensing pixel PD3 is connected to the third clock switch TG3. The fourth light sensing pixel PD4 is connected to the fourth clock switch TG4.

[0087] Further, the first light sensing pixel PD1 is connected to a first terminal of the source follower SF1 via the first clock switch TG1, the second light sensing pixel PD2 is connected to the first terminal of the source follower SF1 via the second clock switch TG2, and the third light sensing pixel PD3 is connected to the first terminal of the source follower SF1 via the third clock switch TG3. The first light sensing pixel PD1 is connected to a first terminal of the reset switch RST1 via the first clock switch TG1, the second light sensing pixel PD2 is connected to the first terminal of the reset switch RST1 via the second clock switch TG2, and the third light sensing pixel PD3 is connected to the first terminal of the reset switch RST1 via the third clock switch TG3. A second terminal of the reset switch RST1 and a second terminal of the source follower SF1 are connected to a predetermined power source, e.g., Vdd. A third terminal of the source follower SF1 is connected to a first terminal of the readout switch SEL1.

[0088] Further, the fourth light sensing pixel PD4 is connected to first terminals of the source follower SF2 and the reset switch RST2 via the fourth clock switch TG4. Second terminals of the source follower SF2 and the reset switch RST2 are connected to the predetermined power source. A third terminal of the source follower SF2 is connected to a first terminal of the readout switch SEL2.

[0089] Further, second terminals of the readout switches SEL1 and SEL2 are respectively connected to one of the analog-to-digital conversion units 40.

[0090] In order to implement control of an exposure, the image sensor 100 further includes a control module. Control terminals of the first clock switch TG1, the second clock switch TG2, the third clock switch TG3, and the fourth clock switch TG4 are connected to the control module. The control module controls turned-on and

turned-off of the four clock switches. When each of the four clock switches is turned on, the corresponding light sensing pixel starts to be exposed.

[0091] It is noted that before being exposed, the light sensing pixels have to be reset. That is, control terminals of the reset switches RST1 and RST2 are also
5 connected to the control module and configured to reset the corresponding light sensing pixels before the corresponding light sensing pixels are exposed or after exposing data is read.

[0092] During an exposure process, the first to fourth light sensing pixels PD1-PD4, for example, photodiodes, receive the light passing through the
10 corresponding one of the light filtering units and generate charge. The clock switches TG1-TG4 are turned on, and the charges generated by the corresponding light sensing pixels are outputted. The charges are converted into analog signals by the source followers SF1 and SF2, and the analog signals are converted into digital signals by the corresponding analog-to-digital conversion units. The digital signals are outputted for
15 providing a data basis of image processing.

[0093] The control module controls the light sensing pixels 22 corresponding to the same one of the light filtering units 11 to be exposed synchronously row by row, and controls exposing time, so as to implement the control of the exposure. Further, the control module further controls outputs of the light sensing pixels to be read out in
20 a time-sharing manner, thereby acquiring source material for synthesizing a high dynamic range image.

[0094] As an example, three light sensing pixels corresponding to each of the light filtering units 11 in the $(2i+1)$ th row ($i=0, 1, 2, 3, 4, \dots$) of the light sensing array
20 and the $(2i+2)$ th row adjacent to the $(2i+1)$ th row (e.g., the light sensing pixels corresponding to the light filtering units Gr1, Gr2, and Gr4), that is, the first light sensing pixel PD1, the second light sensing pixel PD2, and the third light sensing pixel PD3 share the source follower SF1. The charges generated by the first light sensing pixel PD1, the second light sensing pixel PD2, and the third light sensing pixel PD3 are collected, and the collected charges are converted into the analog
25 signals by the source follower SF1. The analog signals are converted into the digital signals by one of the analog-to-digital conversion units 40 and outputted. It is
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assumed that an output value of the one of the analog-to-digital conversion units 40 is ADC1. Further, an output of the light sensing pixel corresponding to each of the light filtering units 11 adjacent to the $(2i+2)$ th row of the light sensing array 20 (e.g., the light sensing pixel corresponding to the light filtering unit Gr3), that is, the output of the fourth light sensing pixel PD4, is converted into analog signals by the source follower SF2. The analog signals are converted into digital signals by the other one of the analog-to-digital conversion units 40 and outputted. It is assumed that an output value of the other one of the analog-to-digital conversion units 40 is ADC2.

[0095] When a photo is taken, the control module controls two adjacent rows of the light sensing units to be exposed synchronously. For example, the $(2i+1)$ th and the $(2i+2)$ th rows ($i=0, 1, 2, 3, 4, \dots$) of the light sensing units are exposed synchronously. The exposing time is controlled to avoid that the light sensing units 22 sharing the same source follower have saturation outputs. In the embodiment of the present disclosure, an output of the source follower SF1 is three times of an output of the source follower SF2. That is, the four light sensing units 22 corresponding to the same light filtering unit 11 can output a high ADC value and a low ADC value synchronously. After the readout switches SEL1 and SEL2 are controlled to be turned on in a timesharing manner, output values of the two analog-to-digital conversion units 40 are SF1 ($SF1=3*SF2$) and SF2, thereby performing a synthetic processing using an image processor to acquire a high dynamic range image. That is, based on hardware structure of the image sensor 100, the high output and the low output of the two analog-to-digital conversion units provide conditions for the synthesis of the high dynamic range image.

[0096] Please refer to FIG. 5. In some embodiments, each of the conversion units 30 includes three source followers 31. One of the source followers 31 is connected to two light sensing pixels 22 in one column of one of the light sensing units 21. The other two of the source followers 31 are respectively connected to remaining two light sensing pixels 22 of the one of the light sensing units 21.

[0097] For example, photoinduced charges generated by the two light sensing pixels 22 in a first column are outputted by the other two of the source followers 31 and merged as a first analog signal A1. Photoinduced charges generated by the two

light sensing pixels 22 in a second column are accumulated and converted into a second analog signal A2 by the one of the source followers 31.

[0098] Further, the image sensor 100 further includes a plurality of analog-to-digital conversion units 40. The one of the source followers 31 connected to the two light sensing units 21 in the same column is connected to one of the analog-to-digital conversion units 40. The other two of the source followers 31 respectively connected to the remaining two light sensing units 21 are connected to the other one of the analog-to-digital conversion units 40. That is, each light sensing unit 21 is connected to two analog-to-digital conversion units 40. Each of the analog-to-digital conversion units 40 is configured to convert analog signals outputted by the source followers 31 into digital signals. In detail, in the present embodiment, the first analog signal A1 is converted into a first digital signal D1 by one of the analog-to-digital conversion units 40, and the second analog signal A2 is converted into a second digital signal D2 by the other one of the analog-to-digital conversion units 40.

[0099] Further, the image sensor 100 further includes a plurality of clock switches 50, a plurality of reset switches 60, and a plurality of readout switches 70. The clock switches 50 are configured to control the light sensing pixels 22 to be exposed. The reset switches 60 are configured to reset the light sensing pixels 22. The readout switches 70 are configured to control readouts of the light sensing pixels 22.

[0100] An equivalent circuit of one of the light sensing units 21 of the image sensor 100 is described as follows. The one of the light sensing units 21 includes light sensing pixels PD1-PD4, clock switches TG1-TG4, source followers SF1-SF3, reset switches RST1-RST3, and readout switches SEL1 and SEL2.

[0101] In detail, the light sensing pixels PD1-PD4 are arranged in a 2x2 array. The first light sensing pixel PD1, the second light sensing pixel PD2, the third light sensing pixel PD3, and the fourth light sensing pixel PD4 are adjacent light sensing pixels and correspond to the same light filtering unit 11. That is, the four adjacent light sensing pixels receive the same color of light. In brief, the four light sensing pixels constitute a large pixel. The first light sensing pixel PD1 and the second light sensing pixel PD2 are positioned in the same row, and the third light sensing pixel

PD3 and the fourth light sensing pixel PD4 are positioned in the same row. Each of the light sensing pixels is connected to one of the clock switches. That is, the first light sensing pixel PD1 is connected to the first clock switch TG1. The second light sensing pixel PD2 is connected to the second clock switch TG2. The third light sensing pixel PD3 is connected to the third clock switch TG3. The fourth light sensing pixel PD4 is connected to the fourth clock switch TG4.

[0102] Further, the second light sensing pixel PD2 is connected to a first terminal of the source follower SF2 via the second clock switch TG2, and the fourth light sensing pixel PD4 is connected to the first terminal of the source follower SF2 via the fourth clock switch TG4. The second light sensing pixel PD2 is connected to a first terminal of the reset switch RST2 via the second clock switch TG2, and the fourth light sensing pixel PD4 is connected to the first terminal of the reset switch RST2 via the fourth clock switch TG4. A second terminal of the reset switch RST2 and a second terminal of the source follower SF2 are connected to a predetermined power source, e.g., Vdd. A third terminal of the source follower SF2 is connected to a first terminal of the readout switch SEL2.

[0103] Further, the first light sensing pixel PD1 is connected to a first terminal of the source follower SF1 via the first clock switch TG1, and the third light sensing pixel PD3 is connected to a first terminal of the source follower SF3 via the third clock switch TG3. The first light sensing pixel PD1 is connected to a first terminal of the reset switch RST1 via the first clock switch TG1, and the third light sensing pixel PD3 is connected to a first terminal of the reset switch RST3 via the third clock switch TG3. Second terminals of the source follower SF1, the source follower SF3, the reset switch RST1, and the reset switch RST3 are connected to the predetermined power source. Third terminals of the source follower SF1 and the source follower SF3 are connected to a first terminal of the readout switch SEL1.

[0104] Further, each of second terminals of the readout switches SEL1 and SEL2 is connected to one of the analog-to-digital conversion units 40.

[0105] In order to implement control of an exposure, the image sensor 100 further includes a control module. Control terminals of the first clock switch TG1, the second clock switch TG2, the third clock switch TG3, and the fourth clock switch TG4 are

connected to the control module. The control module controls turned-on and turned-off of the four clock switches. When each of the four clock switches is turned on, the corresponding light sensing pixel starts to be exposed.

5 [0106] It is noted that before being exposed, the light sensing pixels have to be reset. That is, control terminals of the reset switches RST1, RST2, and RST3 are also connected to the control module and configured to reset the corresponding light sensing pixels before the corresponding light sensing pixels are exposed or after exposing data is read.

10 [0107] During an exposure process, the first to fourth light sensing pixels PD1-PD4, for example, photodiodes, receive the light passing through the corresponding one of the light filtering units and generate charge. The clock switches TG1-TG4 are turned on, and the charges generated by the corresponding light sensing pixels are outputted. The charges are converted into analog signals by the source followers SF1-SF3, and the analog signals are converted into digital signals by the
15 corresponding analog-to-digital conversion units. The digital signals are outputted for providing a data basis of image processing.

[0108] The control module controls the light sensing pixels 22 corresponding to the same one of the light filtering units 11 to be exposed synchronously row by row, and controls exposing time, so as to implement the control of the exposure. Further,
20 the control module further controls outputs of the light sensing pixels to be read out in a time-sharing manner, thereby acquiring source material for synthesizing a high dynamic range image.

[0109] As an example, charges of one light sensing pixel (i.e., the first light sensing pixel PD1 corresponding to the light filtering unit Gr1) in the $(2i+1)$ th row
25 ($i=0, 1, 2, 3, 4, \dots$) of the light sensing array 20 and charges of one light sensing pixel (i.e., the third light sensing pixel PD3 corresponding to the light filtering unit Gr3) in the $(2i+2)$ th row adjacent to the $(2i+1)$ th row in each of the light filtering units 11 are respectively converted by the source followers SF1 and SF3. Outputs of the source followers SF1 and SF3 are converted into digital signals by one of the
30 analog-to-digital conversion units 40 and outputted. It is assumed that an output value of the one of the analog-to-digital conversion units 40 is ADC1. Further, charges

generated by one light sensing pixel (i.e., the second light sensing pixel PD2 corresponding to the light filtering unit Gr2) in the $(2i+1)$ th row of the light sensing array 20 and charges generated by one light sensing pixel (i.e., the fourth light sensing pixel PD4 corresponding to the light filtering unit Gr4) in the $(2i+2)$ th row in the same column of each of the light filtering units 11 are collected and converted by the source follower SF2. An output of the source follower SF2 is converted into digital signals by the other one of the analog-to-digital conversion units 40 and outputted. It is assumed that an output value of the other one of the analog-to-digital conversion units 40 is ADC2.

[0110] When a photo is taken, the control module controls two adjacent rows of the light sensing units to be exposed synchronously. For example, the $(2i+1)$ th and the $(2i+2)$ th rows ($i=0, 1, 2, 3, 4, \dots$) of the light sensing units are exposed synchronously. The exposing time is controlled to avoid that the light sensing units 22 sharing the same source follower have saturation outputs. In the embodiment of the present disclosure, an output of the source follower SF2 is approximately two times of an output of the source follower SF1 and two times of an output of the source follower SF3 (that is, $SF2=2*SF1=2*SF3$). The output value ADC1 is an average value of the outputs of the source followers SF1 and SF3, and the output value ADC2 is the output of the source follower SF2. That is, the four light sensing units 22 corresponding to the same light filtering unit 11 can output a high ADC value and a low ADC value synchronously. After the readout switches SEL1 and SEL2 are controlled to be turned on in a timesharing manner, the output values of the two analog-to-digital conversion units 40 are ADC1 ($AVG_{SF1+SF3}$) and ADC2 ($SF2=2*SF1=2*SF3$), thereby performing a synthetic processing using an image processor to acquire a high dynamic range image. That is, based on hardware structure of the image sensor 100, the high output and the low output of the two analog-to-digital conversion units provide conditions for the synthesis of the high dynamic range image.

[0111] Please refer to FIG. 6. In some embodiments, each of the conversion units 30 includes three source followers 31. One of the source followers 31 is connected to two light sensing pixels 22 in one row of one of the light sensing units 21. The other two of the source followers 31 are respectively connected to remaining two light sensing pixels 22 of the one of the light sensing units 21.

[0112] For example, photoinduced charges generated by the two light sensing pixels 22 in a first row are accumulated and converted into a first analog signal A1 by the one of the source followers 31. Photoinduced charges generated by the two light sensing pixels 22 in a second row are outputted by the other two of the source followers 31 and merged as a second analog signal A2.

[0113] Further, the image sensor 100 further includes a plurality of analog-to-digital conversion units 40. The three source followers 31 corresponding to each of the light sensing units are connected to one of the analog-to-digital conversion units 40. That is, each of the light sensing units 21 is connected to one of the analog-to-digital conversion units 40. The one of the analog-to-digital conversion units 40 is configured to convert the analog signals outputted by the source followers 31 into digital signals. In detail, in the present embodiment, the first analog signal A1 and the second analog signal A2 are respectively converted into a first digital signal D1 and a second digital signal D2 by the one of the analog-to-digital conversion units 40.

[0114] Further, the image sensor 100 further includes a plurality of clock switches 50, a plurality of reset switches 60, and a plurality of readout switches 70. The clock switches 50 are configured to control the light sensing pixels 22 to be exposed. The reset switches 60 are configured to reset the light sensing pixels 22. The readout switches 70 are configured to control readouts of the light sensing pixels 22.

[0115] An equivalent circuit of one of the light sensing units 21 of the image sensor 100 is described as follows. The one of the light sensing units 21 includes light sensing pixels PD1-PD4, clock switches TG1-TG4, source followers SF1-SF3, reset switches RST1-RST3, and readout switches SEL1 and SEL2.

[0116] In detail, the light sensing pixels PD1-PD4 are arranged in a 2x2 array. The first light sensing pixel PD1, the second light sensing pixel PD2, the third light sensing pixel PD3, and the fourth light sensing pixel PD4 are adjacent light sensing pixels and correspond to the same light filtering unit 11. That is, the four adjacent light sensing pixels receive the same color of light. In brief, the four light sensing pixels constitute a large pixel. The first light sensing pixel PD1 and the second light sensing pixel PD2 are positioned in the same row, and the third light sensing pixel

PD3 and the fourth light sensing pixel PD4 are positioned in the same row. Each of the light sensing pixels is connected to one of the clock switches. That is, the first light sensing pixel PD1 is connected to the first clock switch TG1. The second light sensing pixel PD2 is connected to the second clock switch TG2. The third light sensing pixel PD3 is connected to the third clock switch TG3. The fourth light sensing pixel PD4 is connected to the fourth clock switch TG4.

[0117] Further, the first light sensing pixel PD1 is connected to a first terminal of the source follower SF1 via the first clock switch TG1, and the second light sensing pixel PD2 is connected to the first terminal of the source follower SF1 via the second clock switch TG2. The first light sensing pixel PD1 is connected to a first terminal of the reset switch RST1 via the first clock switch TG1, and the second light sensing pixel PD2 is connected to the first terminal of the reset switch RST1 via the second clock switch TG2. A second terminal of the reset switch RST1 and a second terminal of the source follower SF1 are connected to a predetermined power source, e.g., Vdd. A third terminal of the source follower SF1 is connected to a first terminal of the readout switch SEL1.

[0118] Further, the third light sensing pixel PD3 is connected to a first terminal of the source follower SF2 via the third clock switch TG3, and the fourth light sensing pixel PD4 is connected to a first terminal of the source follower SF3 via the fourth clock switch TG4. The third light sensing pixel PD3 is connected to a first terminal of the reset switch RST2 via the third clock switch TG3, and the fourth light sensing pixel PD4 is connected to a first terminal of the reset switch RST3 via the fourth clock switch TG4. Second terminals of the source follower SF2, the source follower SF3, the reset switch RST2, and the reset switch RST3 are connected to the predetermined power source. Third terminals of the source follower SF2 and the source follower SF3 are connected to a first terminal of the readout switch SEL2.

[0119] Further, second terminals of the readout switches SEL1 and SEL2 are connected to one of the analog-to-digital conversion units 40.

[0120] In order to implement control of an exposure, the image sensor 100 further includes a control module. Control terminals of the first clock switch TG1, the second clock switch TG2, the third clock switch TG3, and the fourth clock switch TG4 are

connected to the control module. The control module controls turned-on and turned-off of the four clock switches. When each of the four clock switches is turned on, the corresponding light sensing pixel starts to be exposed.

5 [0121] It is noted that before being exposed, the light sensing pixels have to be reset. That is, control terminals of the reset switches RST1-RST3 are also connected to the control module and configured to reset the corresponding light sensing pixels before the corresponding light sensing pixels are exposed or after exposing data is read.

10 [0122] During an exposure process, the first to fourth light sensing pixels PD1-PD4, for example, photodiodes, receive the light passing through the corresponding one of the light filtering units and generate charge. The clock switches TG1-TG4 are turned on, and the charges generated by the corresponding light sensing pixels are outputted. The charges are converted into analog signals by the source followers SF1-SF3, and the analog signals are converted into digital signals by the
15 one of the analog-to-digital conversion unit. The digital signals are outputted for providing a data basis of image processing.

[0123] The control module controls the light sensing pixels 22 corresponding to the same one of the light filtering units 11 to be exposed synchronously row by row, and controls exposing time, so as to implement the control of the exposure. Further,
20 the control module further controls outputs of the light sensing pixels to be read out in a time-sharing manner, thereby acquiring source material for synthesizing a high dynamic range image.

[0124] As an example, charges of two light sensing pixels (i.e., the first light sensing pixel PD1 and the second light sensing pixel PD2 corresponding to the light
25 filtering units Gr1 and Gr2) corresponding to each of the light filtering units 11 in the $(2i+1)$ th row ($i=0, 1, 2, 3, 4, \dots$) of the light sensing array 20 are collected and converted by the source follower SF1. An output of the source follower SF1 is converted into digital signals by the one of the analog-to-digital conversion units 40 and outputted. It is assumed that an output value of the one of the analog-to-digital
30 conversion units 40 is ADC1. Further, charges of two light sensing pixels (i.e., the third light sensing pixel PD3 and the fourth light sensing pixel PD4 corresponding to

the light filtering units Gr3 and Gr4) corresponding to each of the light filtering units 11 in the $(2i+1)$ th row ($i=0, 1, 2, 3, 4, \dots$) of the light sensing array 20 adjacent to the $(2i+1)$ th row are respectively collected and converted by the source followers SF2 and SF3. Outputs of the source followers SF2 and SF3 are converted into digital signals by the one of the analog-to-digital conversion units 40 and outputted. It is assumed that an output value of the one of the analog-to-digital conversion units 40 is ADC2.

[0125] When a photo is taken, the control module controls two adjacent rows of the light sensing units to be exposed synchronously. For example, the $(2i+1)$ th and the $(2i+2)$ th rows ($i=0, 1, 2, 3, 4, \dots$) of the light sensing units are exposed synchronously. The exposing time is controlled to avoid that the light sensing units 22 sharing the same source follower have saturation outputs. In the embodiment of the present disclosure, an output of the source follower SF1 is approximately two times of an output of the source follower SF2 and two times of an output of the source follower SF3 (that is, $SF1=2*SF2=2*SF3$). The output value ADC1 is the output of the source follower SF1, and the output value ADC2 is an average value of the outputs of the source followers SF2 and SF3. That is, the four light sensing units 22 corresponding to the same light filtering unit 11 can output a high ADC value and a low ADC value synchronously. After the readout switches SEL1 and SEL2 are controlled to be turned on in a timesharing manner, the output values of the one of the analog-to-digital conversion units 40 are ADC1 ($SF1=2*SF2=2*SF3$) and ADC2 ($AVG_{SF2+SF3}$), thereby performing a synthetic processing using an image processor to acquire a high dynamic range image. That is, based on hardware structure of the image sensor 100, the high output and the low output of the one of the analog-to-digital conversion units provide conditions for the synthesis of the high dynamic range image.

[0126] Please refer to FIG. 7. The image sensor 100 further includes a micromirror array 80 disposed on the light filtering array 10. Each of micromirrors 81 in the micromirror array 80 corresponds to one of the light sensing pixels 22. The correspondence includes formation, size, and position. The micromirrors 81 can guide light to light sensing parts of the light sensing pixels 22 to enhance light receiving intensity of the light sensing pixels 22, thereby improving imaging quality.

[0127] Based on the image sensors in the above-mentioned embodiments, a control method in accordance with an embodiment of the present disclosure is described in conjunction with the appended drawings.

[0128] Please refer to FIG. 8. The control method includes the following operations.

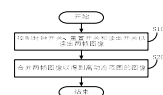
[0129] At block S10, clock switches, reset switches, and readout switches are controlled to read two image frames.

[0130] At block S20, the two image frames are synthesized to acquire a high dynamic range image.

[0131] As the above-mentioned description of the image sensors in the embodiments, the high dynamic range image can be synthesized based on hardware structure of one of the image sensors.

[0132] In an imaging method in accordance with an embodiment of the present disclosure, it is assumed that an output of each of the light sensing pixels is S , noise is N , and a merged pixel includes M light sensing pixels. Accordingly, a pixel value of

the merged pixel is $n*m*S$, and noise of the merged pixel is $\sqrt{n*m*N}$. When $n=2$ and $m=2$, the noise of the merged pixel is approximate $n*m*N/2$. As such, brightness of the merged pixel is increased in a low brightness environment, and a signal-to-noise ratio is increased.



[0133] Please refer to FIG. 9. In some embodiments, block S10 includes the following operations.

[0134] At block S12, the reset switches are controlled to reset the light sensing pixels.

[0135] At block S14, the clock switches are controlled, so that two adjacent rows of the light sensing pixels are exposed synchronously.

[0136] At block S16, timing sequences of the readout switches are controlled to read an output of each of the source followers to read the two image frames.

[0137] As such, source material for synthesizing the high dynamic range image can acquire by controlling the exposure and the time sequences.

[0138] In some embodiments, block S10 further includes converting analog signals outputted by the source followers into digital signals.

5 [0139] As such, an image processing module served as a chip for processing digital signals can directly process the output of the image sensor.

[0140] Based on the image sensors in the above-mentioned embodiments, an electronic device in accordance with an embodiment of the present disclosure is described in conjunction with the appended drawings.

10 [0141] Please refer to FIG. 10. The electronic device 1000 includes one of the above-mentioned image sensors 100. In detail, the electronic device 1000 may include a mobile phone or a tablet computer.

[0142] In some embodiments, the electronic device 1000 further includes a central processing unit 200 connected to the image sensor 100 and a display device
15 300. The central processing unit 200 is configured to control the display device 300 to display an image outputted by the image sensor 100. Accordingly, an image captured by the electronic device 1000 can be displayed in the display device 300 for a user to see. The display device 300 includes an LED display.

[0143] In some embodiments, the electronic device 1000 further includes a
20 central processing unit 200 connected to the image sensor 100 and an external storage device 400. The central processing unit 200 is configured to control the external storage device 400 to store an image outputted by the image sensor 100.

[0144] As such, generated images can be stored, so that they can be seen, used, or transferred conveniently. For example, the external storage device 400 includes a
25 secure digital (SD) card or a compact flash (CF) card.

[0145] The electronic device 1000 which uses the image sensor 100 not only can increase the sensitivity and decrease the signal-to-noise ratio based on the hardware structure of the image sensor 100 when a photo is taken, but also can implement a

function of synthesizing a high dynamic range image to improve photographing experience.

[0146] Please refer to FIG. 11, an embodiment of the present disclosure further provides an electronic device. The electronic device includes a case, a processor, a storage device, a circuit board, and a power circuit. The circuit board is disposed in a space surrounded by the case. The processor and the storage device are disposed on the circuit board. The power circuit is configured to providing power for each circuit and each device of the electronic device. The storage device is configured to store executable program codes. The processor executes programs corresponding to the executable program codes to perform the above-mentioned control methods.

[0147] An embodiment of the present disclosure further provides a computer readable storage medium stored with instructions. When a processor of an electronic device executes the instructions, the electronic device performs the control methods in accordance with the embodiments of the present disclosure as shown in the drawings.

[0148] It should be explained that, relation and relative terms used herein, such as the first and the second, are only used for distinguishing one entity or operation from another entity or operation, and it is not required or suggested to necessarily have any of the practical relations or sequence between the entities or operations. Furthermore, the terms “comprise”, “include” or any other variants aim to be non-exclusive, so that not only a series of elements such as the process, method, article or device included, but also other elements unlisted are included. Furthermore, the inherent elements of the process, method, article or device are included. Under the condition without more limitation, the elements limited by the sentence “comprises a ...” are non-exclusive to additional same elements besides the process, method, article or device of the elements.

[0149] The logic and/or step described in other manners herein or shown in the flowchart, for example, a particular sequence table of executable instructions for realizing the logical function, may be specifically achieved in any computer readable medium to be used by the instruction execution system, device or equipment (such as the system based on computers, the system comprising processors or other systems capable of obtaining the instruction from the instruction execution system, device and

equipment and executing the instruction), or to be used in combination with the instruction execution system, device and equipment. As to the specification, “the computer readable medium” may be any device adaptive for including, storing, communicating, propagating or transferring programs to be used by or in combination
5 with the instruction execution system, device or equipment. More specific examples of the computer readable medium comprise but are not limited to: an electronic connection (an electronic device) with one or more wires, a portable computer enclosure (a magnetic device), a random access memory (RAM), a read only memory (ROM), an erasable programmable read-only memory (EPROM or a flash memory),
10 an optical fiber device and a portable compact disk read-only memory (CDROM). In addition, the computer readable medium may even be a paper or other appropriate medium capable of printing programs thereon, this is because, for example, the paper or other appropriate medium may be optically scanned and then edited, decrypted or processed with other appropriate methods when necessary to obtain the programs in
15 an electric manner, and then the programs may be stored in the computer memories.

[0150] It should be understood that each part of the present disclosure may be realized by the hardware, software, firmware or their combination. In the above embodiments, a plurality of steps or methods may be realized by the software or firmware stored in the memory and executed by the appropriate instruction execution
20 system. For example, if it is realized by the hardware, likewise in another embodiment, the steps or methods may be realized by one or a combination of the following techniques known in the art: a discrete logic circuit having a logic gate circuit for realizing a logic function of a data signal, an application-specific integrated circuit having an appropriate combination logic gate circuit, a programmable gate array (PGA), a field programmable gate array (FPGA), etc.
25

[0151] It is noted that in the description of the specification, reference terminologies “an embodiment”, “some embodiments”, “an illustrate embodiment”, “an example”, “a specific example”, or “some examples”, “some embodiments”, “some embodiments”, “some embodiments”, or “some embodiments” mean that
30 specific features, structures, materials, or characteristics in conjunction with the description of the embodiments or examples are included in at least one of the embodiments or examples. In the specification, the illustrated description of the

above-mentioned terminologies is not limited to the same embodiment or example. Moreover, the described specific features, structures, materials, or characteristics may be combined in a proper way in any one or more of the embodiments or examples.

5 [0152] In the description of the specification, reference terminologies “an embodiment”, “some embodiments”, “an illustrate embodiment”, “an example”, “a specific example”, or “some examples”, “some embodiments”, “some embodiments”, “some embodiments”, or “some embodiments” mean that specific features, structures, materials, or characteristics in conjunction with the description of the embodiments or examples are included in at least one of the embodiments or examples. In the
10 specification, the illustrated description of the above-mentioned terminologies is not limited to the same embodiment or example. Moreover, the described specific features, structures, materials, or characteristics may be combined in a proper way in any one or more of the embodiments or examples.

15 [0153] While the embodiments of the present disclosure have been shown and described, it will be understood that the above-mentioned embodiments are merely exemplary and not to be construed as limiting the present disclosure. Those skilled in the art can make various changes, modifications, equivalents, and variants without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. An image sensor, characterized in comprising:
 - a light sensing array;
 - a light filtering array disposed on the light sensing array, wherein each of light
 - 5 filtering units correspondingly covers one of light sensing units, and each of the light sensing units comprises a plurality of light sensing pixels; and
 - a plurality of conversion units, wherein each of the conversion units comprises at least two source followers, and at least one of the at least two source followers is connected to a plurality of the light sensing pixels.
- 10 2. The image sensor of claim 1, characterized in that the light filtering array comprises a Bayer array.
3. The image sensor of claim 1, characterized in that each of the light sensing units comprises 2x2 light sensing pixels.
4. The image sensor of claim 3, characterized in that each of the conversion
- 15 units comprises two source followers, one of the source followers is connected to two of the light sensing pixels in a first row, and the other one of the source followers is connected to two of the light sensing pixels in a second row.
5. The image sensor of claim 4, characterized in that the image sensor further comprises a plurality of analog-to-digital conversion units, and one of the
- 20 analog-to-digital conversion units is connected to the two source followers.
6. The image sensor of claim 4, characterized in that the image sensor further comprises:
 - a plurality of clock switches, wherein each of the clock switches is connected to one of the light sensing pixels;
 - 25 a plurality of reset switches, wherein the two of the light sensing pixels in the first row is connected to one of the reset switches, and the two of the light sensing pixels in the second row is connected to the other one of the reset switches; and
 - a plurality of readout switches, wherein each of the readout switches is connected to one of the source followers.
- 30 7. The image sensor of claim 3, characterized in that each of the conversion units comprises two source followers, one of the source followers is connected to three of the light sensing pixels, and the other one of the source followers is connected to a remaining one of the light sensing pixels.

8. The image sensor of claim 7, characterized in that the image sensor further comprises a plurality of analog-to-digital conversion units, and each of the analog-to-digital conversion units is connected to one of the source followers.

9. The image sensor of claim 7, characterized in that the image sensor further
5 comprises:

a plurality of clock switches, wherein each of the clock switches is connected to one of the light sensing pixels;

a plurality of reset switches, wherein the three of the light sensing pixels to which the one of the source followers is connected are connected to one of the reset
10 switches, and the remaining one of the light sensing pixels to which the other one of the source followers is connected is connected to the other one of the reset switches; and

a plurality of readout switches, wherein the one of the source followers connected to the three of the light sensing pixels is connected to one of the readout
15 switches, and the other one of the source followers connected to the remaining one of the light sensing pixels is connected to the other one of the readout switches.

10. The image sensor of claim 3, characterized in that each of the conversion units comprises three source followers, one of the source followers is connected to two of the light sensing pixels in one column, and the other two of the source
20 followers are respectively connected to remaining two of the light sensing pixels.

11. The image sensor of claim 10, characterized in that the image sensor further comprises a plurality of analog-to-digital conversion units, the source follower connected to the two of the light sensing unit in the one column is connected to one of the analog-to-digital conversion units, and the two source follower respectively
25 connected to the remaining two of the light sensing units are connected to the other one of the analog-to-digital conversion units.

12. The image sensor of claim 10, characterized in that the image sensor further comprises:

a plurality of clock switches, wherein each of the clock switches is connected to
30 one of the light sensing pixels;

a plurality of reset switches, wherein the two of the light sensing pixels in the one column to which the one of the source followers is connected are connected to one of the reset switches, and the remaining two of the light sensing pixels are connected to respective ones of the reset switches; and

a plurality of readout switches, wherein the one of the source followers connected to the two of the light sensing pixels in the one column is connected to one of the readout switches, and the other two of the source followers respectively connected to the remaining two of the light sensing pixels are connected to the other
5 one of the readout switches.

13. The image sensor of claim 3, characterized in that each of the conversion units comprises three source followers, one of the source followers is connected to two of the light sensing pixels in one row, and the other two of the source followers are respectively connected to remaining two of the light sensing pixels.

10 14. The image sensor of claim 13, characterized in that the image sensor further comprises a plurality of analog-to-digital conversion units, and one of the analog-to-digital conversion units is connected to the three source followers.

15. The image sensor of claim 13, characterized in that the image sensor further comprises:

15 a plurality of clock switches, wherein each of the clock switches is connected to one of the light sensing pixels;

a plurality of reset switches, wherein the two of the light sensing pixels in the one row to which the one of the source followers is connected are connected to one of the reset switches, and the other two of the light sensing pixels are connected to
20 respective ones of the reset switches; and

a plurality of readout switches, wherein the one of the source followers connected to the two of the light sensing pixels in the one row is connected to one of the readout switches, and the other two of the source followers connected to the other two of the light sensing pixels is connected to the other one of the readout switches.

25 16. A control method configured to control an image sensor, characterized in that the image sensor comprises a light sensing array, a light filtering array, and a plurality of conversion units, the light sensing array is disposed on the light sensing array, each of light filtering units correspondingly covers one of light sensing units, each of the light sensing units comprises a plurality of light sensing pixels, each of the
30 conversion units comprises at least two source followers, at least one of the at least two source followers is connected to a plurality of the light sensing pixels, the image sensor further comprises a plurality of clock switches configured to control the light sensing pixels to be exposed, a plurality of reset switches configured to reset the light sensing pixels, and a plurality of readout switches configured to control readouts of

the light sensing pixels, and the control method comprises:

controlling the clock switches, the reset switches, and the readout switches to read two image frames; and

synthesizing the two image frames to acquire a high dynamic range image.

5 17. The control method of claim 16, characterized in that controlling the clock switches, the reset switches, and the readout switches to read the two image frames comprises:

controlling the reset switches to reset the light sensing pixels;

controlling the clock switches, so that two adjacent rows of the light sensing
10 pixels are exposed synchronously; and

controlling timing sequences of the readout switches to read an output of each of the source followers to read the two image frames.

18. The control method of claim 17, characterized in that controlling the clock switches, the reset switches, and the readout switches to read the two image frames
15 comprises:

converting analog signals outputted by the source followers into digital signals.

19. An electronic device, characterized in comprising the image sensor of any one of claims 1-15.

20. The electronic device of claim 19, characterized in that the electronic device
20 comprises a mobile phone or a tablet computer.

21. The electronic device of claim 19, characterized in that the electronic device further comprises a central processing unit connected to the image sensor and a display device, and the central processing unit is configured to control the display device to display an image outputted by the image sensor.

25 22. An electronic device, comprising a case, a processor, a storage device, a circuit board, and a power circuit, characterized in that the circuit board is disposed in a space surrounded by the case, the processor and the storage device are disposed on the circuit board, the power circuit is configured to providing power for each circuit and each device of the electronic device, the storage device is configured to store
30 executable program codes, and the processor executes programs corresponding to the executable program codes to perform the control method of any one of claims 16-18.