

Description

A. BACKGROUND OF THE INVENTION.

A(1) Field of the invention.

The invention relates in broad outline to an arrangement for changing the sampling frequency f_i of a discrete-time signal into a sampling frequency f_u . An arrangement of this type will hereinafter be referred to as sample rate converter and the ratio f_u/f_i will be referred to as the conversion factor. The invention particularly relates to a sample rate converter in which the conversion factor is non-rational (for example, $\sqrt{2}$ or $1/\sqrt{2}$).

A(2) Description of the prior art.

Sample rate converters have been generally known for many years. They are used to increase or decrease the sampling frequency of a discrete-time signal. In the former case, the converter is sometimes referred to as an interpolator, in the latter case as a decimator. For a general background about interpolators and decimators, reference is made to the references 1-6 in section C.

A sample rate converter generally comprises a signal processing circuit. The discrete-time signal is applied thereto as an input signal whose sampling frequency must be changed and furthermore it receives so-called filter coefficients. It supplies the desired discrete-time signal as an output signal. Each sample of this discrete-time output signal is equal to the sum of a number of, for example, M samples of the discrete-time input signal in which each of these input samples is weighted with a filter coefficient.

To calculate an output sample, a group of M filter coefficients must be principally available. These filter coefficients are supplied by a filter coefficient generator and, as is known, they represent samples of the finite pulse response $h(v)$ of a predetermined filter (v is a continuously variable in the interval $-\infty < v < \infty$).

If the sample rate converter is a decimator and if the conversion factor is $1/R$, with R being an integer, it does not supply an output sample until after it has received R input samples. For the calculation of each output sample the same group of M filter coefficients is used. A memory in which the M filter coefficients are stored may be used as a filter coefficient generator.

If the sample rate converter is an interpolator and if the conversion factor is equal to R , it supplies R output samples whenever a new input sample has been received. For each of these R output samples the filter coefficient generator must supply an appropriate group of filter coefficients. Also in this case a memory in which the required (for example, RM) filter coefficients are stored may be used as a filter coefficient generator.

When, as in the above described cases, the quantity R is an integer, the required filter coefficients are invariable. The situation is entirely different

when R is non-rational. In that case the required filter coefficients for each output sample must be calculated separately. Filter coefficient generators that can fulfil this task have been described extensively in references 7 and 8. More particularly, reference 7 describes a decimator, whereas reference 8 describes an interpolator. Each filter coefficient generator used therein comprises a deviation circuit to which on the one hand clock pulses occurring at a "low" rate f_l (hereinafter referred to as low-rate clock pulses) and on the other hand clock pulses occurring at a "high" rate f_h (hereinafter referred to as high-rate clock pulses) are applied. Each time after a low-rate clock pulse has occurred, this deviation circuit supplies a deviation d whose magnitude is proportional to the ratio between the time interval T_d between this low-rate clock pulse and the immediately subsequent or immediately preceding high-rate clock pulse and the time interval $1/f_h$ between two consecutive high-rate clock pulses. In a mathematical form this is:

$$d = T_d \cdot f_h \quad (1)$$

The deviation d thus obtained is applied to a calculation circuit which, starting from the predetermined pulse response $h(v)$, calculates the required filter coefficients. When the m^{th} filter coefficient to be calculated is symbolically represented by $a(m)$, there applies that:

$$a(m) = h(d+m)/f_h \quad (2)$$

If the sample rate converter is a decimator, as in reference 7, f_h is equal to the sampling frequency f_i of the input signal and f_l is equal to the sampling frequency f_u of the output signal. If the sample rate converter is an interpolator, these equalities are reversed.

B. OBJECT AND SUMMARY OF THE INVENTION.

The deviation circuits as extensively described in the said references 7 and 8 are found to require a considerable amount of hardware in practice.

It is therefore an object of the invention according to Claim 1 to provide a simpler embodiment of a deviation circuit of this type.

According to the invention the deviation circuit comprises

- a phase detector to which the low-rate clock pulses are applied on the one hand and to which synthetic low-rate clock pulses are applied on the other hand and which supplies a discrete-time phase difference signal;
- a counter circuit adapted to receive a reference value, which circuit receives the high-rate clock pulses as counting pulses and supplies a synthetic low-rate clock pulse for the phase detector each time after receiving a number of high-rate clock pulses which is equal to the reference value; and
- a processor circuit which receives the discrete-time phase difference signal and in response there-

to supplies deviations d at the low rate f_l as well as reference values for the counter circuit.

Functionally, this deviation circuit constitutes a phase-locked loop in which a generator is used as a voltage-controlled oscillator supplying a sawtooth signal, the height of the sawtooth being determined by the phase difference signal and the slope being constant.

The implemented phase-locked loop as defined above does not, however, actually supply this sawtooth signal in a complete form. On the other hand the processor circuit supplies a reference value which indicates how many high-rate clock pulses fit into one period of the sawtooth signal and this period must be equal to the period with which the low-rate clock pulses are applied to the phase detector. The processor circuit which is used in combination with the counter circuit for generating the synthetic clock pulses is also used for calculating the deviation d so that no extra hardware is required for this purpose.

C. REFERENCES.

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D. BRIEF DESCRIPTION OF THE FIGURES.

Fig. 1 diagrammatically shows the general structure of a sample rate converter;

Fig. 2 shows the theoretical model of the phase-locked loop shown in Fig. 1;

Figs. 3, 4 and 5 show some diagrams to explain the operation of the filter coefficient generator shown in Fig. 1;

Fig. 6 shows the flow chart for programming the processor shown in Fig. 1;

Fig. 7 shows an embodiment of a loop filter; and

Fig. 8 shows an embodiment of a digital phase detector.

E. DESCRIPTION OF THE EMBODIMENTS.

E(1) General structure of a sample rate converter.

Fig. 1 diagrammatically shows the general structure of a sample rate converter having a non-rational conversion factor. It is provided with an input buffer 1 through which the input samples $x(q)$ which occur at a rate f_i are applied to a signal processing device 2 supplying output samples $y(n)$ at the desired rate f_u . For calculating each output samples $y(n)$ the signal processing device 2 also receives M filter coefficients $a(0), a(1), \dots, a(M-1)$ from a filter coefficient generator 3.

The buffer 1 has a write input W and a read input RE . The write input WR receives a clock signal cl_i consisting of clock pulses $cl_i(.)$ occurring at the input sampling frequency f_i . The input sample $x(q)$ is stored in this buffer in response to a clock pulse $cl_i(.)$. The read input RE receives a clock signal cl_h consisting of clock pulses $cl_h(.)$ which occur at a frequency f_h and will be referred to as high-rate clock pulses. Whenever such a high-rate clock pulse $cl_h(.)$ occurs, the contents of the buffer are transferred to the signal processing device 2 and the buffer is also reset. Thus it is achieved that if no input sample is stored in the buffer between two consecutive high-rate clock pulses, a sample having the value zero is applied to the signal processing device 2. This situation occurs when the sample rate converter is an interpolator.

The signal processing device 2 may be implemented in known manner. For example, in the manner as described in reference 7 when the sample rate converter is a decimator and in the manner as described in reference 8 when it is an interpolator.

The clock pulses $cl_i(.)$ occurring at the input sampling frequency f_i are supplied by a clock pulse generator 4. It will be assumed that there is also a clock pulse generator 5 supplying a clock signal consisting of the clock pulses $cl_u(.)$ occurring at the output sampling frequency f_u . Since a sample rate converter is concerned in this case, the output sampling frequency will be either higher or lower than the in-

put sampling frequency. The previously mentioned clock signal cl_h consisting of the high-rate clock pulses $cl_h(.)$ is now formed by one of the two clock signals cl_l and cl_u , more specifically by the clock signal whose clock pulses occur at the highest rate. For the purpose of simplification of the following, the other clock signal will be indicated by cl_l and its clock pulses with $cl_l(.)$. The rate at which these clock pulses occur will be indicated by f_l and they will be referred to as low-rate clock pulses.

The clock pulses $cl_h(.)$ and $cl_l(.)$ are applied to the filter coefficient generator 3 and utilized therein for calculating the deviation d on the one hand and the required coefficients $a(m)$ on the other hand. To this end this filter coefficient generator 3 is provided with a phase-locked loop 30 and a calculation device 31. In response to each low-rate clock pulse $cl_l(.)$ the phase-locked loop 30 supplies a deviation $d(.)$ which is applied to the calculation device 31 (for example, a microcomputer). The latter is adapted to calculate the required filter coefficients at the given value of $d(.)$ in accordance with expression (2).

The phase-locked loop 30 comprises more particularly a phase detector 301, a processor circuit 302 and a counter circuit 304. In the embodiment shown the processor circuit 302 is constituted by the cascade arrangement of a loop filter 3021 and a processor 3022. The phase detector 301 receives the low-rate clock pulses $cl_l(.)$ at one of its inputs and synthetic low-rate clock pulses $cl'_l(.)$ at the other input, which latter pulses are supplied by the counter circuit 304. This phase detector supplies a discrete-time phase difference signal u in which each phase difference sample $u(.)$ is a measure of the time interval between a clock pulse $cl_l(.)$ and the immediately subsequent or immediately preceding synthetic clock pulse $cl'_l(.)$. The discrete-time phase difference signal thus obtained is subjected in the loop filter 3021 to a discrete-time filter processing operation. As a result of and in response to each low-rate clock pulse $cl_l(.)$ this loop filter supplies a control signal sample $H(.)$ which is processed in the processor 3022. This processor is programmed in a manner to be described hereinafter so that on the one hand it supplies the deviation $d(.)$ and on the other hand a number $N(.)$ which indicates how many high-rate clock pulses fit into one period of a hypothetical sawtooth signal having the same slope in each period but whose sawtooth height and thus also the actual period is proportional to the actual control signal sample $H(.)$ supplied by the loop filter. This number $N(.)$ is applied to the counter circuit 304. This circuit 304 also receives the high-rate clock pulses via a clock pulse input and supplies a synthetic clock pulse $cl'_l(.)$ when $N(.)$ high-rate clock pulses have been received. Therefore this counter circuit 304 may advantageously be designed as a presettable down counter.

It is to be noted that the phase detector 301 supplies a control pulse SP simultaneously with a phase difference sample $u(.)$, which pulse is applied to the processor circuit for its initialisation.

E(2) Theoretical background of the invention.

The embodiment of the phase-locked loop shown in Fig. 1 is a practical embodiment of the theoretical model shown in Fig. 2. In addition to the phase detector 301 and the loop filter 302, this model comprises a sawtooth oscillator 305 and a differentiating network 306. The phase detector 301 again receives the low-rate clock pulses $cl_l(.)$ and $cl'_l(.)$ and supplies in response to each low-rate clock pulse a difference signal sample $u(.)$ which is a measure of the phase difference between the last received low-rate clock pulse $cl_l(.)$ and the immediately subsequent or immediately preceding low-rate clock pulse $cl'_l(.)$. After filtering of the phase difference samples by the loop filter 3021, a control signal sample $H(.)$ is obtained which controls the sawtooth oscillator 305. All sawteeth supplied by this oscillator have the same slope. Their tooth height is, however, equal or proportional to the actual control signal sample $H(.)$. Whenever the sawtooth has reached this tooth height, a new sawtooth starts and the differentiating network 306 supplies a low-rate synthetic clock pulse $cl'_l(.)$.

When the loop is not locked, there is a phase difference between two low-rate clock pulses. This situation is shown for completeness' sake in Fig. 3. More particularly Fig. 3 shows at A a number of low-rate clock pulses $cl_l(.)$, at B a number of synthetic low-rate clock pulses $cl'_l(.)$ and at C the output signal $z(t)$ of oscillator 305.

When the loop is locked, there is a minimum phase difference between the two low-rate clock pulse signals cl_l and cl'_l . This situation is shown for completeness' sake in Fig. 4. More particularly this Fig. 4 shows at A again a number of low-rate clock pulses $cl_l(.)$, at B a number of low-rate clock pulses $cl'_l(.)$ and at C the output signal $z(t)$ of oscillator 305.

As is shown in Fig. 2, the output signal $z(t)$ of the sawtooth oscillator 305 is first sampled in the sampler 307 for calculating the consecutive deviations $d(.)$, the high-rate clock pulses $cl_h(.)$ being used as sampling pulses. A number of these high-rate clock pulses is shown at D in Fig. 4. In response to these clock pulses the sampler supplies the sawtooth samples $z(.)$ shown at E in Fig. 4 of the sawtooth signal $z(t)$ shown at C in Fig. 4. In the diagram shown at E the original sawtooth signal is shown in broken lines for completeness' sake. These sawtooth samples $z(.)$ are furthermore applied to a calculator circuit 308 calculating a new deviation $d(.)$ whenever a control pulse SP has occurred and applying this deviation to its output. To indicate how this deviation $d(.)$, which is mathematically formulated in expression (2), is calculated by using the sawtooth samples $z(.)$, the part of the diagram shown at E in Fig. 4 between the points P and Q is enlarged in Fig. 5. In this Figure a number of points have been indicated by a, b, c, e, g, k, m. In accordance with expression (2) there applies that:

$$d(q) = T_d(q) \cdot f_h.$$

In this expression $T_d(q)$ represents the distance between the low-rate clock pulse $cl_l(q)$ the immediately subsequent high-rate clock pulse $cl_h(n+1)$, or the immediately preceding high-rate clock pulse $cl_h(n)$. The starting point hereinafter will be that $T_d(q+1)$ is the distance between $cl_l(q)$ and $cl_h(n+1)$ so that this distance corresponds to the line section gc. The reciprocal value T_h of f_h represents the distance between two consecutive sawtooth samples and thus corresponds to the length of the line section ab. Furthermore the line sections gk and em correspond to $H(q-1)$ and the length of the line section ec corresponds to $z(n+1)$. Since each sawtooth has the same slope, the difference between two consecutive sawtooth samples within one and the same period is constant. This constant has the magnitude $incr$. Since the line section eb represents such a difference, the length of this line section corresponds to $incr$. In accordance with the known rules of planimetry it then follows that

$$d(q) = z(n+1)/incr. \quad (3)$$

It follows that for calculating the deviation $d(.)$ it is sufficient to know the value of the first sawtooth sample taken from a sawtooth.

The present invention is based on the recognition that this sawtooth sample can be calculated and that the consequence thereof is that the sawtooth oscillator 305 shown in Fig. 2 is no longer physically present in the sample rate converter according to the invention. More particularly $z(n+1)$ can be derived from $z(n-4)$. In fact, as is apparent from Fig. 5:

$$z(n+1) = z(n-4) + 5 \text{ incr} - H(q-1) \quad (4)$$

In this expression the number 5 indicates that $z(n+1)$ is the fifth sawtooth sample after $z(n-4)$. To generalise expression (4) it is to be noted that a new sawtooth does not start until after a difference signal sample $u(.)$ has occurred, whilst the q^{th} sawtooth commences after the q^{th} difference signal sample $u(q)$ has occurred. When the first sawtooth sample taken from the q^{th} sawtooth is represented by $s(q)$ and when furthermore the number of high-rate clock pulses occurring within the period of this q^{th} sawtooth (or, identically, the number of sawtooth samples from this q^{th} sawtooth) is equal to N , there generally applies that

$$s(q) = s(q-1) + N \text{ incr} - H(q-1) \quad (5)$$

so that

$$d(q) = s(q)/incr = N + \{s(q-1) - H(q-1)\}/incr \quad (6)$$

In this expression the quantities $s(q)$ and N are unknown. The quantity $incr$ is fixed and known by choice. The quantity $H(q-1)$ is supplied by the loop filter, the quantity $s(q-1)$ is known because this is the result either of a preceding calculation or because it is a known initial value. In spite of all these known quantities expression (6) comprises $s(q)$ as

the desired quantity but also N as an unknown quantity. In order to be able to calculate the desired sawtooth sample $s(q)$ it should be considered that

$$0 \leq s(q) < incr \quad (7)$$

and hence

$$0 \leq s(q)/incr < 2^0 \quad (8)$$

$$\text{while } N \geq 2^0(9)$$

In other words, if a number P can be found which is equal to, for example, the difference

$$p = -N + s(q)/incr$$

and which consists of the sum of two numbers P_1 and P_2 in which, for example, $P_1 < 1$ and $P_2 \geq 1$, then it holds that

$$\begin{aligned} d(q) &= s(q)/incr = P_1 \\ N &= P_2 \end{aligned} \quad (10)$$

Such a number P exists indeed and can be calculated.

In accordance with expression (6)

$$-N + s(q)/incr = \{s(q-1) - H(q-1)\}/incr = P \quad (11)$$

E(3) The processor 3022.

The quantity P indicated in expression (11) is calculated by the processor 3022 which may be a microcomputer. It may be, for example, a microcomputer of the MAB 8000 family in which the steps shown in Fig. 6 are carried out. A calculation cycle starts some time after the phase detector 301 has supplied a control pulse SP. After the last supplied phase difference sample has given a contribution to the new control sample $H(q-1)$ which is supplied by the loop filter, this sample $H(q-1)$ is read by the processor and stored in a work register intended for this purpose (step 302(0)). Subsequently the last calculated sawtooth sample $s(q-1)$ stored in a storage location intended for this purpose and referred to as S store is transferred to a further work register (step 302(1)). These two data are subsequently subtracted from each other in a step 302(2) and divided by the number $incr$. As a result the desired number P is obtained which is stored in a P-register (step 302(3)). In a step 302(4) the bits of P having a significance which is larger than or equal to 2^0 and thus represent the number N are subsequently applied to the counter circuit. In a further step 302(5) the bits of P having a significance of less than 2^0 and thus representing the deviation $d(q)$ are applied to the calculation device 31. Subsequently the deviation $d(q)$ is multiplied by the number $incr$ in a step 302(6) so that the number $s(q)$ is obtained. Finally the sawtooth sample $s(q-1)$ is replaced by $s(q)$ in the S store in a step 302(7).

E(4) The loop filter.

Fig. 7 shows an embodiment of a loop filter 3021. It is of the discrete-time type and comprises counter circuits 30211 and 30212, three delay circuits 30213, 30214 and 30215 each having a delay period T_1 and three multipliers 30216, 30217 and 30218 with the respective multiplication coefficients C_0 , C_1 and C_2 supplied by a coefficient generator 30219. These elements are interconnected in the manner shown in the Figure such that a transfer function is realised which is equal to:

$$C_2(1+C_0Z^{-1})/(1-Z^{-1})(1-C_1Z^{-1}) \quad (12)$$

In a practical embodiment the multiplication coefficients were chosen as follows:

$$\begin{aligned} C_0 &= b-1 \\ C_1 &= 1-32b \\ C_2 &= -1/2 W^2 \\ b &= 2^{-7}W. \end{aligned} \quad (13)$$

W is a number to be chosen in the range of 10^{-2} to 10^{-7} inclusive. This number W need not be a fixed number. In the embodiment shown the coefficient generator 30219 receives the phase difference signal and based thereon it calculates a value for W so as to calculate subsequently the coefficients with this value for W in accordance with expression (13). The loop filter thus obtained is referred to as an adaptive filter.

As is known, the embodiment of the loop filter shown in Fig. 7 may also be considered as a flow diagram for a software implementation. This means that such a loop filter can also be implemented in known manner in software in the processor 3022.

E(5) The phase detector.

Fig. 8 shows an embodiment of a digital phase detector 301. It is provided with a device 3011 to which the low-rate clock pulses $cl_l(.)$ are applied. After having received a clock pulse $cl_l(.)$ this device supplies a pulse in phase with a high-rate clock pulse $cl_h(.)$. The output-signal of this device 3011 as well as the synthetic low-rate clock pulses $cl_l(.)$ are applied to a control circuit 3012 supplying an up command UP or a down command DWN for an up-down counter 3013. The latter counter also receives the high-rate clock pulses $cl_h(.)$ as counting pulses. The contents of this counter are transferred to the processor circuit at the instant when the control pulse SP occurs.

In the embodiment shown the control circuit 3012 consists of 2 JK flip-flops 30121 and 30122 and an AND gate 30123 which are connected together in the manner shown. The JK flip-flops are of the type having a clock pulse input. The high-rate clock pulses are applied thereto.

The pulse supplied by AND-gate 30123 resets the two JK flip-flops and also sets a further flip-flop 3014 which in response thereto supplies the previ-

ously mentioned control pulse SP starting, inter alia, the program shown in Fig. 6.

5 Claims

1. An arrangement for changing the sampling frequency of a discrete-time signal having a value f_i in to a value f_u , one of said two sampling frequencies being equal to f_i and the other being equal to a higher frequency f_h , said arrangement comprising:

a) first means for supplying low-rate clock pulses occurring at the said rate f_i ;

b) second means for supplying high-rate clock pulses occurring at the said rate f_h ;

c) a filter coefficient generator (3) comprising:

c1) a deviation circuit (30) to which the low and high-rate clock pulses are applied and which supplies a deviation d which is equal to the product of f_h and a time interval T_d between a low-rate clock pulse and the immediately subsequent or the immediately preceding high-rate clock pulse;

c2) means (31) to generate a predetermined number of (M) filter coefficients in response to the supplied deviation d , the filter coefficient having ordinal number m being equal to $a(m)$ and being defined by the relation

$$a(m) = h[(d+m)/f_h]$$

wherein the function $h[.]$ represents the pulse response of a FIR filter and $m = 0, 1, 2, \dots, M-1$;

d) a signal processing circuit (2) for generating at a rate f_u the samples of the discrete-time signal having the changed sampling frequency by multiplication of samples of the original discrete-time signal by selected filter coefficients and by adding the products thus obtained;

characterized in that the deviation circuit (30) comprises:

c11) a phase detector (301) to which the low-rate clock pulses are applied on the one hand and to which synthetic low-rate clock pulses are applied on the other hand and which supplies a discrete-time phase difference signal;

c12) a counter circuit (304) adapted to receive a reference value, which circuit receives the high-rate clock pulses as counting pulses and supplies a synthetic low-rate clock pulse each time after receiving a number of high-rate clock pulses which is equal to the reference value; and

c13) a processor circuit (302) receiving the discrete-time phase difference signal and in response thereto supplying the deviation d to the means (31) generating the filter coefficients as well as reference values for the counter circuit (304) at the rate f_i .

2. An arrangement as claimed in Claim 1, characterized in that the processor circuit (302) is adapted to perform a discrete-time filtering on the discrete-time phase difference signal for generating control signal samples ($H(.)$).

E(4) The loop filter.

Fig. 7 shows an embodiment of a loop filter 3021. It is of the discrete-time type and comprises counter circuits 30211 and 30212, three delay circuits 30213, 30214 and 30215 each having a delay period T_1 and three multipliers 30216, 30217 and 30218 with the respective multiplication coefficients C_0 , C_1 and C_2 supplied by a coefficient generator 30219. These elements are interconnected in the manner shown in the Figure such that a transfer function is realised which is equal to:

$$C_2(1+C_0Z^{-1})/(1-Z^{-1})(1-C_1Z^{-1}) \quad (12)$$

In a practical embodiment the multiplication coefficients were chosen as follows:

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As is known, the embodiment of the loop filter shown in Fig. 7 may also be considered as a flow diagram for a software implementation. This means that such a loop filter can also be implemented in known manner in software in the processor 3022.

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ously mentioned control pulse SP starting, inter alia, the program shown in Fig. 6.

5 Claims

1. An arrangement for changing the sampling frequency of a discrete-time signal having a value f_l into a value f_u , one of said two sampling frequencies being equal to f_l and the other being equal to a higher frequency f_h , said arrangement comprising:

a) first means for supplying low-rate clock pulses occurring at the said rate f_l ;

b) second means for supplying high-rate clock pulses occurring at the said rate f_h ;

c) a filter coefficient generator (3) comprising:

c1) a deviation circuit (30) to which the low and high-rate clock pulses are applied and which supplies a deviation d which is equal to the product of f_h and a time interval T_d between a low-rate clock pulse and the immediately subsequent or the immediately preceding high-rate clock pulse;

c2) means (31) to generate a predetermined number of (M) filter coefficients in response to the supplied deviation d , the filter coefficient having ordinal number m being equal to $a(m)$ and being defined by the relation

$$a(m) = h[(d+m)/f_h]$$

wherein the function $h[.]$ represents the pulse response of a FIR filter and $m = 0, 1, 2, \dots, M-1$;

d) a signal processing circuit (2) for generating at a rate f_u the samples of the discrete-time signal having the changed sampling frequency by multiplication of samples of the original discrete-time signal by selected filter coefficients and by adding the products thus obtained;

characterized in that the deviation circuit (30) comprises:

c11) a phase detector (301) to which the low-rate clock pulses are applied on the one hand and to which synthetic low-rate clock pulses are applied on the other hand and which supplies a discrete-time phase difference signal;

c12) a counter circuit (304) adapted to receive a reference value, which circuit receives the high-rate clock pulses as counting pulses and supplies a synthetic low-rate clock pulse each time after receiving a number of high-rate clock pulses which is equal to the reference value; and

c13) a processor circuit (302) receiving the discrete-time phase difference signal and in response thereto supplying the deviation d to the means (31) generating the filter coefficients as well as reference values for the counter circuit (304) at the rate f_l .

2. An arrangement as claimed in Claim 1, characterized in that the processor circuit (302) is adapted to perform a discrete-time filtering on the discrete-time phase difference signal for generating control signal samples $H(.)$.



3. An arrangement as claimed in Claim 2, characterized in that the discrete-time filtering is described by the transfer function

$$C_2(1+C_0Z^{-1})/(1-Z^{-1})(1-C_1Z^{-1})$$

wherein C_0 , C_1 and C_2 are multiplication coefficients.

4. An arrangement as claimed in Claim 2, characterized in that the processor circuit (302) is further adapted to carry out the following steps:

- a) calculating a difference quantity (P) which is equal to the difference between the actual control sample $H(.)$ and an auxiliary sample $s(.)$ divided by a fixed weighting factor (incr);
- b) applying those bits of the difference quantity P that have a significance which is less than 2^o as a deviation (d) to the means generating the filter coefficients and applying the other bits of this difference quantity as a reference value to the counter circuit (304);
- c) calculating a new auxiliary sample $s(.)$ by multiplication of the deviation d obtained in step b by the weighting factor (incr).

Patentansprüche

1. Anordnung zum Ändern der Abtastfrequenz eines zeitdiskreten Signals von einem Wert f_i zu einem Wert f_u , wobei eine dieser beiden Abtastfrequenzen dem Wert f_i und die andere einer höheren Frequenz f_h entspricht, wobei diese Anordnung die folgenden Elemente aufweist:

- a) erste Mittel zum Liefern von Taktimpulsen niedriger Geschwindigkeit, die mit der genannten Geschwindigkeit f_i auftreten,
- b) zweite Mittel zum Liefern von Taktimpulsen hoher Geschwindigkeit, die mit der genannten Geschwindigkeit f_h auftreten,
- c) einen Filterkoeffizientengenerator (3), der mit den folgenden Mitteln versehen ist:

c1) einer Abweichungsschaltung (30), der die Taktimpulse niedriger und hoher Geschwindigkeit zugeführt werden und die eine Abweichung d liefert, die dem Produkt aus f_h und einem Zeitintervall T_d zwischen einem Taktimpuls niedriger Geschwindigkeit und dem unmittelbar folgenden oder dem unmittelbar vorhergehenden Taktimpuls hoher Geschwindigkeit entspricht;

c2) Mitteln (31) zum in Antwort auf die gelieferte Abweichung d Liefern einer vorbestimmten Anzahl (M) Filterkoeffizienten, wobei der Filterkoeffizient mit der Rangnummer m dem Wert $a(m)$ entspricht und durch die folgende Beziehung definiert wird:

$$a(m) = h [(d+m) / f_h]$$

wobei die Funktion $h [.]$ die Impulsstoßantwort eines FIR-Filters darstellt und $m = 1, 2, \dots, M-1$ ist;

d) eine Signalbearbeitungsschaltung (2) zum mit einer Geschwindigkeit f_u Erzeugen der Abtast-

werte des zeitdiskreten Signals mit der geänderten Abtastfrequenz durch Multiplikation von Abtastwerten des ursprünglichen zeitdiskreten Signals mit selektierten Filterkoeffizienten und durch Addition der auf diese Weise erhaltenen Produkte;

dadurch gekennzeichnet, daß die Abweichungsschaltung (30) die folgenden Elemente aufweist:

c11) einen Phasendetektor (301), dem einerseits die Taktimpulse niedriger Geschwindigkeit und andererseits synthetische Taktimpulse niedriger Geschwindigkeit zugeführt werden, und der ein zeitdiskretes Phasendifferenzsignal liefert;

c12) eine Zählerschaltung (304) zum Empfangen eines Bezugswertes, die als Zählerimpulse die Taktimpulse hoher Geschwindigkeit empfängt und die jeweils nach Empfang einer dem Bezugswert entsprechenden Anzahl Taktimpulse hoher Geschwindigkeit einen synthetischen Taktimpuls niedriger Geschwindigkeit liefert; und

c13) eine Prozessorschaltung (302), die das zeitdiskrete Phasendifferenzsignal empfängt und in Antwort darauf mit der Geschwindigkeit f_i die Abweichung d zu den die Filterkoeffizienten liefernden Mitteln (31), sowie die Bezugswerte für die Zählerschaltung (304) liefert.

2. Anordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Prozessorschaltung (302) dazu eingerichtet ist, zum Erzeugen von Steuersignalabtastwerten ($H(.)$) an dem zeitdiskreten Phasendifferenzsignal eine zeitdiskrete Filterung durchzuführen.

3. Anordnung nach Anspruch 2, dadurch gekennzeichnet, daß die zeitdiskrete Filterung durch die nachfolgende Übertragungsfunktion beschrieben wird:

$$C_2(1+C_0Z^{-1})/(1-Z^{-1})(1-C_1Z^{-1})$$

worin C_0 , C_1 und C_2 Multiplikationskoeffizienten sind.

4. Anordnung nach Anspruch 2, dadurch gekennzeichnet, daß die Prozessorschaltung (302) weiterhin zum Durchführen der nachfolgenden Verfahrensschritte eingerichtet ist:

a) das Berechnen einer Differenzgröße (P) entsprechend der Differenz zwischen dem Ist-Steuerabtastwert $H(.)$ und einem Hilfsabtastwert $s(.)$ geteilt durch einen festen Gewichtungsfaktor (incr.);

b) das Zuführen derjenigen Bits der Differenzgröße P, die eine Signifikanz aufweisen, die kleiner ist als 2^o als Abweichung (d) zu den die Filterkoeffizienten erzeugenden Mitteln und das Zuführen der übrigen Bits dieser Differenzgröße als Bezugswert zu der Zählerschaltung (304);

c) das Berechnen eines neuen Hilfsabtastwertes $s(.)$ durch Multiplikation der in dem Verfahrensschritt b erhaltenen Abweichung d mit dem Gewichtungsfaktor (incr.).



Revendications

1. Système pour transformer la fréquence d'échantillonnage d'un signal temporel discret d'une valeur f_i en une valeur f_u , une des deux fréquences d'échantillonnage étant égale à f_i et l'autre, à une fréquence plus élevée f_h , le système comprenant:

a) un premier moyen pour fournir des impulsions d'horloge à cadence basse se présentant à la fréquence f_i ;

b) un second moyen pour fournir des impulsions d'horloge à cadence haute se présentant à la fréquence f_h ;

c) un générateur de coefficients de filtrage (3) comprenant:

c1) un circuit de déviation (30) auquel les impulsions d'horloge à cadences basse et haute sont appliquées et qui fournit une déviation d égale au produit de f_h et d'un intervalle de temps T_d entre une impulsion d'horloge à cadence basse et l'impulsion d'horloge à cadence haute immédiatement suivante ou immédiatement précédente;

c2) un moyen (31) pour produire un nombre prédéterminé de (M) coefficients de filtrage en réponse à la déviation d fournie, le nombre ordinal m du coefficient de filtrage étant égal à $a(m)$ et étant défini par l'équation:

$$a(m) = h [(d+m)/f_h]$$

où la fonction $h[.]$ représente la réponse impulsionnelle d'un filtre FIR et $m = 0, 1, 2, \dots, M-1$;

d) un circuit de traitement de signaux (2) pour produire, à une cadence f_u , les échantillons de signal temporel discret présentant la fréquence d'échantillonnage transformée par multiplication d'échantillons du signal temporel discret initial par des coefficients de filtrage sélectionnés et par addition des produits ainsi obtenus;

caractérisé en ce que le circuit de déviation (30) comprend:

c11) un détecteur de phase (301) auquel les impulsions d'horloge à cadence basse sont appliquées d'une part et auquel des impulsions d'horloge synthétiques à cadence basse sont appliquées d'autre part, et qui fournit un signal temporel discret de différence de phase;

c12) un circuit de compteur (304) propre à recevoir une valeur de référence, ce circuit recevant les impulsions d'horloge à cadence haute à titre d'impulsions de comptage et fournissant une impulsion d'horloge synthétique à cadence basse chaque fois qu'il a reçu un nombre d'impulsions d'horloge à cadence haute qui est égal à la valeur de référence, et

c13) un circuit de processeur (302) recevant le signal temporel discret de différence de phase et fournissant, en réponse à celui-ci, la déviation d au moyen (31) qui produit les coefficients de filtrage, ainsi que des valeurs de référence pour le circuit de compteur (304) à la fréquence f_i .

2. Système suivant la revendication 1, caractérisé en ce que le circuit de processeur (302) peut effectuer un filtrage temporel discret sur le signal temporel discret de différence de phase pour produire des échantillons de signal de commande $[H(.)]$.

3. Système suivant la revendication 2, caractérisé en ce que le filtrage temporel discret est décrit par la fonction de transfert:

$$C_2(1+C_0Z^{-1})/(1-Z^{-1})(1-C_1Z^{-1})$$

où C_0 , C_1 et C_2 sont des coefficients de multiplication.

4. Système suivant la revendication 2, caractérisé en ce que le circuit de processeur (302) est, en outre, à même d'effectuer les opérations suivantes:

a) calcul d'une grandeur de différence (P) qui est égale à la différence entre l'échantillon de commande réel $H(.)$ et un échantillon auxiliaire $s(.)$ divisé par un facteur de pondération fixe (incr);

b) application des bits de la grandeur de différence P qui ont une signification inférieure à 2^n en tant que déviation (d) au moyen qui produit les coefficients de filtrage et application des autres bits de cette grandeur de différence en tant que valeur de référence au circuit de compteur (304);

c) calcul d'un nouvel échantillon auxiliaire $s(.)$ par multiplication de la déviation d obtenue dans l'opération b par le facteur de pondération (incr).

