Description

This invention relates generally to a solid state imager device constructed by charge transfer devices (CTD), and more particularly to a solid state imager device of this kind which has a light receiving area formed of a so-called buried channel MOS structure (the MOS structure designates a stacking structure of the form: semiconductor layer - dielectric layer - conduction layer) to thereby form a charge storage layer on the surface thereof.

In an interline transfer CTD type solid state imager device, a remarkable reduction in dark current can be expected to be caused by a current generated on the surface of the device by forming a light receiving section of a buried channel MOS structure to thereby operate the device under conditions that a pinning, i.e. a charge storage layer is formed over the surface thereof.

Fig. 1 shows a cross-sectional view of a main portion of such a solid state imager device which is mainly formed of a silicon semiconductor substrate 1 in which on a substrate forming a p-type region 2 there is formed an n-type semiconductor layer 3. On a major surface 1a of the substrate 1 at the side where the semiconductor layer 3 is provided, there are provided with a light receiving section 4, a charge transfer section 5, i.e. vertical shift register arranged at every vertical line, horizontal shift register, not shown in the drawing, and so on.

The light receiving section 4 is formed of the n-type semiconductor layer 3 itself and is composed of a light receiving area 6 which is sectioned by a plurality of channel stop regions, not shown,
arranged in the horizontal and vertical directions. Further, an n-type overflow drain area or region 8 is arranged adjacent to the light receiving area 6 through a p-type overflow control area or region 7.

The vertical shift register section 5 is formed of an n-type charge transfer region 10 formed on a p-type well region 9 which is selectively formed on the semiconductor layer 3.

Over the major surface 1a of the substrate 1, there is also deposited a light-transmissible dielectric layer 11, e.g. SiO_2 or the like.

There is deposited on the dielectric layer 11 between the light receiving section 4 and the vertical shift register section, i.e. the charge transfer section 5, a transfer control electrode 13 which controls the transfer of signal charges accumulated in the light receiving section 4 to the charge transfer region 10 of the vertical shift register section 5, to thereby form a transfer control section 12. The transfer control electrode 13 is formed in common e.g. with a portion of transfer electrodes of the vertical shift register section 5.

In a forward portion of the light receiving section 4, that is, on the dielectric layer 11 at the light receiving section 4, there is deposited a light-transmissible forward electrode 14 all over the overflow control region 7 and the overflow drain region 8.

The transfer control electrode 13 and the forward electrode 14 can be formed of e.g. a polycrystalline silicon layer. The surface of the device except for the light receiving section 4 is covered with a light shielding member which is not shown in Fig. 1. Further, on the surfaces of the respective electrodes, e.g. the transfer control electrode 13 arranged below the forward electrode 14, there is coated an insulating layer 15 made of e.g. SiO_2 or the like thereby to insulate the respective electrodes electrically from one another.

In the construction described above, a predetermined negative voltage is applied to the forward electrode 14 to form a storage layer for positive charges in the light receiving area 6 at its surface, so that a buried channel is formed from the surface of the area 6 to its inside. Since the voltage actually applied to the forward electrode 14 is limited by the voltage which the material will withstand and so on, the lowest potential point in the buried channel is at most several volts. When charges, that is, electrons, generated by received light are accumulated in this storage layer, the thickness of a depletion layer produced below the light receiving area 6 is actually at most 2 - 3 μm. On the other hand, disturbance or a so-called smear in a picked-up image, caused by the signal charge flowing from inside the substrate into another light receiving area 6 or the charge transfer region 10 of the vertical shift register section 5 depends on the thickness of the depletion layer below the light receiving area 6 as described above. To be specific, the smear becomes larger as the thickness of the depletion layer becomes thinner. In general, a depletion layer having a thickness of only 2 - 3 μm is not sufficient to prevent smear from occurring.

GB-A-2,007,937 discloses a solid state image sensor similar to that described with reference to Figure 1 and suffers from the same disadvantage.

Incidentally, a pinning MOS type CCD imager device which has a charge storage layer formed over the surface thereof is disclosed e.g. by a collection of papers presented at '84 National Conference of the Institute of Television Engineers of Japan, on pages 41 - 42.

Therefore, it is the object of the present invention to provide a solid state imager device which solves the problem of the smear due to the above-mentioned depletion layer being narrow as well as other problems associated therewith.

According to the invention there is provided a solid state imaging device comprising a semiconductor substrate having at its major surface a low impurity concentration region of a second conductivity type in which a light receiving section, a transfer control section and a charge transfer section are provided next to each other, wherein:

said light receiving section comprises at least one light receiving area of said second conductivity type;

a light transmissible dielectric layer is formed on said major surface;

a charge transfer control electrode is formed on said dielectric layer between said light receiving section and said charge transfer section, thereby defining said transfer control section, wherein an edge of said transfer control electrode at a side of said light receiving area substantially coincides with an edge of said light receiving area at a side facing said charge transfer section; and

a light transmissive electrode is formed on the dielectric layer above the light receiving section; characterised in that:

a substrate region of a first conductivity type is formed under said low impurity region; and

said low impurity region has a lower impurity concentration than said light receiving area.

In the present invention, the upper limit of the low impurity concentration is about 1×10^{16} atoms/cm^3.

The above and other features, and advantages of the present invention will becom apparent from the following detailed description of the preferred embodiment taken in conjunction with the accompanying drawings, throughout which like reference numerals designates like elements and parts. In the drawings:-

Fig. 1 is an enlarged cross-sectional view showing a main portion of a prior art device;

Fig. 2 is an enlared cross-sectional view showing a main portion of a device according to the present invenion;

Figs. 3 and 4 are graphs of potential distribution for explaining the operation of the device according to the present invention shown in Fig. 2;

Figs. 5A through 5F are diagrams showing a manufacturing process of the device of the present invention shown in Fig. 2; and

Figs. 6 and 7 are respectively enlarged cross-sectional views showing main portions of other examples of the device according to the present invention.

An embodiment of a solid state imager device according to the present invention will hereinafter be described with reference to Fig. 2 which is

an enlarged cross-sectional view showing a main portion of a solid state imager device according to the invention.

As is clear from Fig. 2, the solid state imager device is formed mainly of a semiconductor substrate 21 which has a first conductivity type, e.g. p-type substrate region 22 on which, through a low impurity concentration region 23 and facing its major surface 21a at its side opposite to the side where the substrate region 22 is formed, there is formed a light receiving section 24 which is composed of a plurality of second conductivity type, e.g. n-type, light receiving areas 26 arranged in the vertical and horizontal directions. Then, a charge transfer section 25, that is, a vertical shift register is arranged along the light receiving areas 26 which are arranged e.g. along a common vertical line. The charge transfer section 25 is also constructed by forming a second conductivity type charge transfer region 30 on a well region 29 of the first conductivity type.

On the major surface 21a of the substrate 21, there is deposited a light-transmissible dielectric layer 31. A transfer control electrode 33 for controlling the transfer of the signal charge accumulated in the light receiving section 24 to the vertical shift register section 25 is deposited on the dielectric layer 31 between the light receiving section 24 and the charge transfer section, that is, the vertical shift register section 25 to thereby form a transfer control section 32. The transfer control electrode 33 can be formed in common with e.g. a portion of the transfer electrode of the vertical shift register section 25.

Further, through an overflow control region 27 of the first conductivity type and surrounding the respective light receiving areas 26, there is formed an overflow drain region 28 of the second conductivity type.

In a forward portion of the light receiving section 24, that is, on the dielectric layer 31 above the light receiving section 24, a light transmissive forward electrode 34 is deposited all over the overflow control region 27 and the overflow drain region 28.

The transfer control electrode 33 and the forward electrode 34 can be formed of e.g. a polycrystalline silicon layer. The surface of the device except for the light receiving section 24 is covered with a light shielding member, not shown. Further, on the surfaces of the respective electrodes, e.g. the transfer control electrode 33 arranged below the forward electrode 34, there is coated an insulating layer 35 made of e.g. SiO_2 or the like thereby to insulate the respective electrodes electrically from one another.

Reference numeral 36 designates a channel stop region formed on the major surface 21a of the substrate 21, surrounding sections to be separated from each other, e.g. the vertical shift register section 25, the light receiving section 24, and so on.

In the above-mentioned solid state imager device, the forward electrode 34 has applied to it a predetermined negative voltage to form a storage layer for the positive charges on the surface of the light receiving area 26, so that a buried channel is formed from the surface of the light receiving area 6 to the inside thereof. Since the low impurity concentration region 23 is arranged below the light receiving area 26, the potential distribution in its thickness direction traversing the light receiving area 26, namely, the depletion layer is thereby extended as indicated by the solid line curve in Fig. 3. In this condition, when light is incident on the light receiving area 26 and thereby car-

riers, (electrons in the illustrated example in Fig. 2) are generated, the electrons are accumulated in a valley of the potential so that the potential distribution changes as indicated by the broken line curve in Fig. 3, and the depletion layer is reduced to some degree. However, due to the existence of the low impurity concentration region 23, the depletion layer is left in a relatively extended condition. By virtue of the effect described above, it is possible largely to reduce the possiblity of charges leaking from the light receiving area 26 to the substrate 21 and hence inhibit charges from flowing into other light receiving area or the charge transfer section 25, so that the smear effect can be effectively avoided.

Further, as described above, according to the present invention, the low impurity concentration region 23 is arranged under the light receiving area 26 or surrounding the same. If the light receiving area 26 is provided, extending to a region below the transfer control electrode 33 of the transfer control section 32, upon read-out of the charges (i.e. when the charges accumulated in the light receiving area 26 are transferred to the shift register section 25, in other words, when a positive voltage is applied to the transfer control electrode 33), the potential in the part of the light receiving area extending to the region below the transfer control electrode 33 is different from that in the other part below the electrode 33. As a result, a valley of potential occurs which interferes with the charge transfer from the light receiving area 26 to the charge transfer region 30. However, according to the present invention, since the end edge of the light receiving area 26 is made coincident with that of the transfer control electrode 33, the above-mentioned inconvenience can be avoided.

Fig. 4 is a graph showing the distribution of potential of signal charges along the surface direction of a portion of the substrate 21 including the light receiving section 24 and the vertical shift register section 25. The solid line curve in the graph represents the light receiving state or the case where a voltage, e.g. 0 V is applied to the transfer control electrode 33 to accmulate signal charges, e.g. electrons, generated by receiving light, e.g. electrons in the light receiving area 26. The broken line curve in the graph represents the case where a voltage, e.g. 10 V is applied to the electrode 33, to transfer the signal charges from the light receiving area 26 to the charge tranfer region 30. Thus, there can be formed in the transfer control section a step-shaped mono-directional gradient toward the charge transfer region 30, without any barrier or valley, so that the signal charges can be effectively transferred.

Next, the manufacturing procedure of the solid state imager device as shown in Fig. 2 will be explained in its order with reference to Figs. 5A through 5F.

First, referring to Fig. 5A, a p-type silicon substrate 42 forming the substrate region 22 is prepared. A semiconductor layer 43 having a lower impurity concentration than the light receiving area 26, to be formed later, is formed on the surface of the substrate by a vapor growth technique or by introducing an n-type impurity all over a major surface of the substrate 42 by an ion implantation or diffusion technique. Thus, the semiconductor substrate 21 comprising the substrate 42 and the semiconductor layer 43 is formed.

Next, as shown in Fig. 5B, the p-type well region 29 is formed by selectively implanting a p-type impurity to a relatively large depth, e.g. to a depth reaching the substrate 42, into the semiconductor layer 43 by the ion implantation or diffusion technique. In the same manner, a p-type impurity is implanted selectively into the semiconductor layer 43 by the ion implantation, diffusion technique or the like to form the flow control region 27 and the channel stop region 36.

As shown in Fig. 5C, an n-type impurity is implanted selectively into the well region 29 outside the overflow control region 27 by the ion implantation, diffusion technique or the like to form the overflow drain region 28 and a charge transfer section, that is, the charge transfer region 30 of the vertical shift register section 25.

As shown in Fig. 5D, over the major surface 21a of the semiconductor substrate 21 opposite to the surface having the substrate 42, the dielectric layer 31 made of, e.g. SiO_2 or the like is deposited by a surface thermal oxidation technique. Then, on the top thereof, e.g. a polycrystalline silicon layer having a low resistivity is formed by a chemical vapor deposition (CVD) technique or the like and thereafter this layer is photoetched to form a predetermined pattern thereby to form the transfer control electrode 33.

Then, as shown in Fig. 5E, while the transfer control electrode 33 is used at least as a mask, an n-type impurity, e.g. phosphorus P is implanted thereinto to form the light receiving area 26.

Next, as shown in Fig. 5F, over the surface of the electrode 33 the insulating layer 35 is formed by, e.g. thermally oxidizing the same. Further, on the insulating layer 35, the forward electrode 34 of apolycrystalline silicon layer is deposited in the same manner as the electrode 33.

By the construction described above, it is possible to obtain the same imager device as that shown in Fig. 2 in which the low impurity concentration region 23 is formed in a portion of the semiconductor layer 43. Actually, other sections such as the horizontal shift register section, the output circuit and so on which construct the interline transfer system imager device, are formed on the semiconductor substrate 21 in the course of the procedure described above.

Further, in the example of the invention shown in Figs. 2 and 5, the charge transfer region 30 is formed on the well region 29 in such a manner that it is locat-

ed in the inside of the well region 29, that is, a portion of the well region 29 faces to the surface of the substrate 21 between the vertical shift register section 25 and the light receiving section 24. In this case, by virtue of the well region 29, it is possible to prevent the signal charge which flows into the inside of the substrate for some reasons from entering the charge transfer region 30 of the vertical shift register section 25 and consequently to suppress the occurrence of flares. Also because part of the well region 29 faces the surface of the substrate 21, when the imager device receives light, a high potential barrier (as can be seen from Figure 4) can be formed between the light receiving area 26 and the charge transfer region 30 so that unnecessary charges can be inhibited from flowing into the charge transfer region 30.

However, the well region 29, as shown in Figs. 6 and 7, may be limited and formed beneath the charge transfer region 30. In the case of Fig. 6, a region 51 is provided on the surface of the substrate 21 which serves as the barrier, or as shown in Fig. 7, only the barrier formed by the low impurity concentration region 23 is used.

As described above, according to the present invention, since the light receiving section is formed as a buried channel type pinning MOS structure, the dark current can be reduced. Further, the low impurity region 23 is arranged under the light receiving area 26 to widen the depletion layer, so that image smear can be effectively suppressed.

In addition to these advantages, since the light receiving area 26 has its edge coincident with the edge of the charge transfer control electrode 33 to prevent the area 26 from extending to the under part of the electrode 33, the defect that when the voltage is applied to the electrode 33 to read out the signal charges, a potential valley is produced between the charge transfer region 30 and the light receiving area 26 which interferes with the charge transfer, can be avoided.

Claims

1. A solid state imaging device comprising a semiconductor substrate (21) having at its major surface (21a) a low impurity concentration region (23) of a second conductivity type in which a light receiving section (24), a transfer control section (32) and a charge transfer section (25) are provided next to each other, wherein:

   said light receiving section (24) comprises at least one light receiving area (26) of said second conductivity type;

   a light transmissible dielectric layer (31) is formed on said major surface;

   a charge transfer control electrode (33) is formed on said dielectric layer (31) between said light receiving section (24) and said charge transfer section (25), thereby defining said transfer control section, wherein an edge of said transfer control electrode (33) at a side of said light receiving area (26) substantially coincides with an edge of said light receiving area (26) at a side facing said charge transfer section (25); and

   a light transmissive electrode (34) is formed on the dielectric layer (31) above the light receiving section (24); characterised in that:

   a substrate region (22) of a first conductivity type is formed under said low impurity region (23); and

   said low impurity region has a lower impurity concentration than said light receiving area (26).

2. A solid state imager device as claimed in claim 1, wherein said charge transfer section (25) is formed of a second conductivity type charge transfer region and a first conductivity type well region formed beneath said charge transfer region (25).

3. A solid state imager device as claimed in claim 2, wherein a part of said well region faces a surface of said semiconductor substrate (21) between said charge transfer section (25) and said light receiving section (26).

4. A solid state imager device as claimed in claim 2, wherein said well region is formed just beneath said charge transfer section (25).

5. A solid state imager device according to claim 4 further comprising a region of the first conductivity type which is formed on a surface of said semiconductor substrate (21) between said charge transfer section (25) and said light receiving section (26) and serves as a barrier.

Patentansprüche

1. Festkörper-Bilderzeugungseinrichtung, die ein Halbleitersubstrat (21) umfaßt, das auf seiner Hauptoberfläche (21a) einen Bereich (23) mit einer niedrigen Störstellenkonzentration eines zweiten Leitfähigkeitstyps hat, in dem ein lichtempfangender Abschnitt (24), ein Übertragungssteuerabschnitt (32) und ein Ladungsübertragungsabschnitt (25) nahe beieinander vorgesehen sind, wobei

   der lichtempfangende Abschnitt (24) zumindest einen lichtempfangenden Bereich (26) des zweiten Leitfähigkeitstyps hat,

   eine lichtdurchlässige dielektrische Schicht (31) auf der Hauptoberfläche ausgebildet ist,

ed in the inside of the well region 29, that is, a portion of the well region 29 faces to the surface of the substrate 21 between the vertical shift register section 25 and the light receiving section 24. In this case, by virtue of the well region 29, it is possible to prevent the signal charge which flows into the inside of the substrate for some reasons from entering the charge transfer region 30 of the vertical shift register section 25 and consequently to suppress the occurrence of flares. Also because part of the well region 29 faces the surface of the substrate 21, when the imager device receives light, a high potential barrier (as can be seen from Figure 4) can be formed between the light receiving area 26 and the charge transfer region 30 so that unnecessary charges can be inhibited from flowing into the charge transfer region 30.

However, the well region 29, as shown in Figs. 6 and 7, may be limited and formed beneath the charge transfer region 30. In the case of Fig. 6, a region 51 is provided on the surface of the substrate 21 which serves as the barrier, or as shown in Fig. 7, only the barrier formed by the low impurity concentration region 23 is used.

As described above, according to the present invention, since the light receiving section is formed as a buried channel type pinning MOS structure, the dark current can be reduced. Further, the low impurity region 23 is arranged under the light receiving area 26 to widen the depletion layer, so that image smear can be effectively suppressed.

In addition to these advantages, since the light receiving area 26 has its edge coincident with the edge of the charge transfer control electrode 33 to prevent the area 26 from extending to the under part of the electrode 33, the defect that when the voltage is applied to the electrode 33 to read out the signal charges, a potential valley is produced between the charge transfer region 30 and the light receiving area 26 which interferes with the charge transfer, can be avoided.

Claims

1. A solid state imaging device comprising a semiconductor substrate (21) having at its major surface (21a) a low impurity concentration region (23) of a second conductivity type in which a light receiving section (24), a transfer control section (32) and a charge transfer section (25) are provided next to each other, wherein:

   said light receiving section (24) comprises at least one light receiving area (26) of said second conductivity type;

   a light transmissible dielectric layer (31) is formed on said major surface;

   a charge transfer control electrode (33) is formed on said dielectric layer (31) between said light receiving section (24) and said charge transfer section (25), thereby defining said transfer control section, wherein an edge of said transfer control electrode (33) at a side of said light receiving area (26) substantially coincides with an edge of said light receiving area (26) at a side facing said charge transfer section (25); and

   a light transmissive electrode (34) is formed on the dielectric layer (31) above the light receiving section (24); characterised in that:

   a substrate region (22) of a first conductivity type is formed under said low impurity region (23); and

   said low impurity region has a lower impurity concentration than said light receiving area (26).

2. A solid state imager device as claimed in claim 1, wherein said charge transfer section (25) is formed of a second conductivity type charge transfer region and a first conductivity type well region formed beneath said charge transfer region (25).

3. A solid state imager device as claimed in claim 2, wherein a part of said well region faces a surface of said semiconductor substrate (21) between said charge transfer section (25) and said light receiving section (26).

4. A solid state imager device as claimed in claim 2, wherein said well region is formed just beneath said charge transfer section (25).

5. A solid state imager device according to claim 4 further comprising a region of the first conductivity type which is formed on a surface of said semiconductor substrate (21) between said charge transfer section (25) and said light receiving section (26) and serves as a barrier.

Patentansprüche

1. Festkörper-Bilderzeugungseinrichtung, die ein Halbleitersubstrat (21) umfaßt, das auf seiner Hauptoberfläche (21a) einen Bereich (23) mit einer niedrigen Störstellenkonzentration eines zweiten Leitfähigkeitstyps hat, in dem ein lichtempfangender Abschnitt (24), ein Übertragungssteuerabschnitt (32) und ein Ladungsübertragungsabschnitt (25) nahe beieinander vorgesehen sind, wobei

   der lichtempfangende Abschnitt (24) zumindest einen lichtempfangenden Bereich (26) des zweiten Leitfähigkeitstyps hat,

   eine lichtdurchlässige dielektrische Schicht (31) auf der Hauptoberfläche ausgebildet ist,

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eine Ladungsübertragungs-Steuerelektrode (33) auf der dielektrischen Schicht (31) zwischen dem lichtempfangenden Abschnitt (24) und dem Ladungsübertragungsabschnitt (25) ausgebildet ist, um dadurch den Übertragungssteuerabschnitt zu definieren, wobei ein Rand der Ladungsübertragungs-Steuerelektrode (33) auf einer Seite des lichtempfangenden Bereichs (26) im wesentlichen mit einem Rand des lichtempfangenden Bereichs (26) auf einer Seite zusammenfällt, die dem Ladungsübertragungsabschnitt (25) gegenüberliegt, und

eine lichtdurchlässige Elektrode (34) auf der dielektrischen Schicht (31) oberhalb des lichtempfangenden Abschnitts (24) ausgebildet ist,

dadurch **gekennzeichnet**, daß

ein Substratbereich (22) eines ersten Leitfähigkeitstyps unter dem Bereich (23) mit der niedrigen Störstellenkonzentration ausgebildet ist und

der Bereich mit der niedrigen Störstellenkonzentration eine niedrigere Störstellenkonzentration als der lichtempfangende Bereich (26) hat.

2. Festkörper-Bilderzeugungseinrichtung nach Anspruch 1, bei der der Ladungsübertragungsabschnitt (25) aus einem Ladungsübertragungsbereich eines zweiten Leitähigkeitstyps gebildet ist und ein Senkenbereich eines ersten Leitfähigkeitstyps unterhalb des Ladungsübertragungsbereichs (25) ausgebildet ist.

3. Festkörper-Bilderzeugungseinrichtung nach Anspruch 2, bei der ein Teil des Senkenbereichs einer Oberfläche des Halbleitersubstrats (21) zwischen dem Ladungsübertragungsabschnitt (25) und dem lichtempfangenden Abschnitt (26) gegenüberliegt.

4. Festkörper-Bilderzeugungseinrichtung nach Anspruch 2, bei der der Senkenbereich genau unterhalb des Ladungsübertragungsabschnitts (25) ausgebildet ist.

5. Festkörper-Bilderzeugungseinrichtung nach Anspruch 4, die ferner einen Bereich des ersten Leitfähigkeitstyps umfaßt, der auf einer Oberfläche des Halbleitersubstrats (21) zwischen dem Ladungsübertragungsabschnitt (25) und dem lichtempfangenden Abschnitt (26) ausgebildet ist und als eine Barriere dient.

Revendications

1. Dispositif imageur à l'état solide comprenant un substrat semiconducteur (21) ayant au niveau de sa surface principale (21a) une région à concentration en impuretés faible (23) d'un second type de conductivité dans laquelle une section de réception de lumière (24), une section de commande de transfert (32) et une section de transfert de charge (25) sont prévues de manière à se faire suite, dans lequel :

ladite section de réception de lumière (24) comprend au moins une zone de réception de lumière (26) dudit second type de conductivité ;

une couche diélectrique laissant passer la lumière (31) est formée sur ladite surface principale ;

une électrode de commande de transfert de charge (33) est formée sur ladite couche diélectrique (31) entre ladite section de réception de lumière (24) et ladite section de transfert de charge (25) de manière à définir ladite section de commande de transfert, dans lequel un bord de ladite électrode de commande de transfert (33) au niveau d'un côté de ladite zone de réception de lumière (26) coïncide sensiblement avec un bord de ladite zone de réception de lumière (26) au niveau d'un côté qui fait face à ladite section de transfert de charge (25) ; et

une électrode laissant passer la lumière (34) est formée sur la couche diélectrique (31) au-dessus de la section de réception de lumière (24),

caractérisé en ce que :

une région de substrat (22) d'un premier type de conductivité est formée sous ladite région à concentration en impuretés faible (23) ; et

ladite région à concentration en impuretés faible présente une concentration en impuretés inférieure à celle de ladite zone de réception de lumière (26).

2. Dispositif imageur à l'état solide selon la revendication 1, dans lequel ladite section de transfert de charge (25) est formée par une région de transfert de charge du second type de conductivité et par une région de puits du premier type de conductivité formée au-dessous de ladite région de transfert de charge (25).

3. Dispositif imageur à l'état solide selon la revendication 2, dans lequel une partie de ladite région de puits fait face à une surface dudit substrat semiconducteur (21) entre ladite section de transfert de charge (25) et ladite section de réception de lumière (26).

4. Dispositif imageur à l'état solide selon la revendication 2, dans lequel ladite région de puits est formée juste au-dessous de ladite section de transfert de charge (25).

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5. Dispositif imageur à l'état solide selon la revendication 4, comprenant en outre une région du premier type de conductivité qui est formée sur une surface dudit substrat semiconducteur (21) entre ladite section de transfert de charge (25) et ladite section de réception de lumière (26) et qui joue le rôle de barrière.