Description

This invention relates to television receivers of a type having the capability of displaying a main picture and a smaller picture that is inset within the main picture.

Television receivers having so-called "picture-in-picture" operating modes in which a main picture is displayed along with a smaller inset picture are known. An example of a television receiver having such features is described in U. S. Patent US-A-4,890,162 which issued to McNeely et al. December 26, 1989. It is a feature of the McNeely et al. receiver that the picture-in-picture processor they disclose includes a tuner input for providing a "main" video signal, an auxiliary input for providing another source of video for the inset picture and a picture "swap" switch in the input of the processor. By this feature it is possible to reverse or interchange the main and small pictures being displayed.

It is herein recognized that in color television receivers of the type including picture-in-picture processing that a problem concerning color distortion may arise under certain conditions of input signal selection. In more detail, when one is displaying a video signal provided by a tuner and associated IF amplifier along with a video signal provided by an external source (e.g., a VCR) there are typically different chrominance signal peaking requires for the two signals. The tuner provided signal normally requires a "slope" type of chrominance peaking to compensate for the IF filter response. Specifically, a conventional IF circuit tends to attenuate the upper side-band of the chrominance signal relative to the lower sideband. To correct for this sideband distortion the chrominance signal provided by the tuner source is conventionally applied to a sideband correction filter (known as a "slope" filter) which attenuates the lower sideband of the chrominance signal relative to the upper sideband to provide a peaked chrominance output signal in which the sidebands are of balanced amplitude. On the other hand, video signal provided by an auxiliary baseband video source are typically reasonably well balanced and require only band pass filtering or a "flat" (unfiltered) response characteristic for optimum color fidelity.

From the foregoing it is apparent that different peaking requirements are needed for the two different types of video input signals. This is normally not a problem for receivers which do not have picture-in-picture processing as one may simply select the appropriate peaking for the input signal being displayed. However, for receivers with picture-in-picture processing the different peaking requirements for the two simultaneously displayed images may be quite noticeable. Although chrominance peaking circuits having switchable characteristics are known, such circuits typically are not sufficiently fast to provide chrominance peaking changes at video signal rates and so this precludes selection of different chrominance signal peaking responses for the main and inset pictures.

The present invention is directed to meeting the need for an effective reduction in the visibility of chrominance signal peaking errors in a color television receiver employing picture-in-picture processing.

A color television receiver embodying the invention includes a picture-in-picture processor comprising a large picture processor, a small picture processor and a multiplex switch coupled to the processors for providing multiplexed luminance and chrominance output signals to a display processor for providing an image having a small picture area processed by said small picture processor that is inset within a larger picture area processed by the large picture processor. An input switch is provided having a first state for applying first and second video input signals supplied thereto to respective inputs of said large and small picture processors and having a second state for interchanging the video signals applied to said processors. A variable peaking circuit is connected between a chrominance signal output of said multiplex switch and a chrominance signal input of said display processor, said variable peaking circuit having a first operating mode for applying a first peaking characteristic to said multiplexed chrominance signal when said first video signal is applied to said large picture processor and having a second operating mode for applying a second peaking characteristic to said multiplexed chrominance signal otherwise.

In accordance with a further feature of the invention, the receiver includes a tuner, IF amplifier and video detector unit for providing the first video signal to the input switch, the first peaking characteristic exhibits a sloped response within a chrominance signal band and the second peaking characteristic exhibits a substantially symmetrical response within the chrominance signal band.

The sole FIGURE is a block diagram of a color television receiver embodying the invention.

As a brief overview of the color television receiver of the sole FIGURE, there is provided a picture-in-picture processor and a variable peaking circuit for imparting a first peaking characteristic to the chrominance component of displayed signals when the main picture being displayed is from a tuner video source and for imparting a second peaking characteristic to the chrominance component when the main picture picture being displayed is from an auxiliary video source thereby providing an effective reduction in the visibility of chrominance signal peaking errors when displaying picture-in-picture images from different types of sources.

The receiver of the sole FIGURE comprises a picture-in-picture processor 10 (outlined in phantom) including a large picture processor 12 (illustratively, a

comb filter), a small picture processor 14 (illustratively, a random access memory and control circuit) and a multiplex switch 16 coupled to the large and small picture processors for providing a multiplexed luminance and chrominance output signals to a display processor 20 for providing an image on a kinescope 22 (or other suitable display device) having a small picture area processed by the small picture processor that is inset within a larger picture area processed by the large picture processor. An input switch 30 in processor 10 provides input signal swapping so as to interchange the large and small images displayed by kinescope 22. The switch of the double pole double throw type in which the switch outputs are coupled to video inputs of respective ones of the large and small picture processors. For the switch position shown the upper switch section couples the video signal provided by a further switch 40 to the large picture processor and the lower section couples a video output signal provided by a tuner 50 and IF processing unit 52 to the small picture processor. Reversing the position of switch 30 interchanges the coupled signals thereby interchanging the content of the large and small pictures displayed on kinescope 22. The switch 40 selects between two auxiliary input signals provided by input terminals 42 and 44 and the tuner provided baseband video signal for application to switch 30. Control of switches 30, 16 and the small picture processor is provided by a decoder 18 responsive to control signals provided by a main control unit (e.g., a microprocessor) 54 responsive to user inputs provided by a remote control unit 55.

Elements of the picture-in-picture processor are all of conventional design and a more detailed description of the processor is given in the aforementioned United States patent No. 4,890,162 of McNeely et al. which issued December 26, 1989 and is herein incorporated by reference. special effects

The receiver of the sole FIGURE further includes a luminance chrominance (Y-C) processing unit 60 which provides conventional luminance and chrominance signal processing function in units 62 and 64 which coupled the multiplexed luminance and chrominance signals provided by multiplex switch 16 to corresponding inputs of the display processing unit 20 that provides conventional functions such as matrixing, sweep generation and the like. Y-C processor 60 further includes a pair of chrominance peaking filters 66 and 68 having band pass and sloped response characteristics, respectively. A switch 70, controlled by a level detector 72 selectively couples the multiplexed chrominance signal at input terminal 74 to the two peaking filters responsive to a DC level change in the signal applied to terminal 74. An integrated circuit containing the foregoing elements of processor 60 is the type TA8680 integrated circuit manufactured by Toshiba. Other processors are suitable provided they include some means for changing the chrominance signal peaking.

Control of the peaking provided by processor 60 is provided by control unit 54 which applies a DC voltage level to terminal 74 by means of an adder circuit 76 connected to the multiplexed chrominance signal output of multiplex switch 16. This method of peaking control is used by the manufacturer of the aforementioned integrated circuit in order to reduce the pin-count of the integrated circuit. It is not, however, essential to use this form of peaking control by DC level changes. In a given application the variable peaking circuit may be implemented by discrete circuit elements rather than in an integrated circuit in which case the peaking may be controlled directly rather than by adding DC levels to the chrominance signal and detecting the levels as shown.

The effect of always matching the peaking to the source providing the large picture is that in some cases the peaking will be correct for both pictures and in cases where the peaking is not optimum for the inset (small) picture the greater size of the correctly peaked large picture tends to mask the defects in the smaller picture due strictly to the difference in picture size. As a first example, assume that the user activates control 54 via remote control 55 to select the tuner video applied to switch 40. In this case, regardless of the position of picture swap switch 30 both the large picture and the small picture will display the signal provided by the tuner 50 and the variable peaking circuit will select the slope type chrominance peaking filter 68. Thus, in this case there is no chrominance peaking error for either picture. Now consider another case where switch 30 selects tuner video for the large picture processor and switch 40 selects the auxiliary video signal from terminal 42 for application to the small picture processor via switch 30. For this case control 54 will activate the slope type filter 68 and the tuner signal processed by the large picture processor will be correctly peaked but the auxiliary video processed by the small picture processor will be peaked by the tuner peaking filter 68 rather than the correct (flat response) filter 66. For this case the greatest area of the picture will be correctly peaked which makes imperfections in peaking of the small picture relatively unnoticeable. The same result obtains if picture swap switch 30 is changed over to apply the auxiliary video to the large picture processor and to apply the tuner video to the small picture processor. This results because at the same time control 54 will also change over the peaking selector switch 70 thereby providing normal peaking for the auxiliary video signal processed by the large picture processor and the peaking errors due to use of filter 66 on the tuner video processed by the small picture processor 14 will be relatively unnoticeable.

Claims

1. A color television receiver comprising:

a picture-in-picture processor including a large picture processor (12), a small picture processor (14) and a multiplex switch (16) coupled to said processors for providing multiplexed luminance and chrominance output signals to a display (20,22) for providing an image having a small picture area processed by said small picture processor that is inset within a larger picture area processed by the large picture processor;

an input switch (30) having a first state for applying first and second video input signals supplied thereto to respective inputs of said large and small picture processors and having a second state for interchanging the video signals applied to said processors; characterized by:

a variable peaking circuit (54,66,68,70, 72, 74,76) connected between a chrominance signal output of said multiplex switch and a chrominance signal input of said display processor (20) said variable peaking circuit having a first operating mode for applying a first peaking characteristic (68) to said multiplexed chrominance signal when said first video signal is applied to said large picture processor and having a second operating mode for applying a second peaking characteristic (66) to said multiplexed chrominance signal otherwise.

2. A color television receiver as recited in Claim 1 characterized in that:

said receiver includes a tuner, IF amplifier and detector unit (50,52) for providing said first video signal to said input switch;

said first peaking characteristic (68) exhibits a sloped response within a chrominance signal band; and

said second peaking characteristic (66) exhibits a substantially uniform response within said chrominance signal band.

Patentansprüche

1. Ein Farbfernsehempfänger mit:
einem Bild-im-Bild-Prozessor mit einem Großbildprozessor (12), einem Kleinbildprozessor (14) und einem an die besagten Prozessoren angekoppelten Multiplexschalter (16) zur Bereitstellung von gemultiplexten Luminanz- und Chrominanz-Ausgangssignalen für eine Anzeige (20, 22) zur Bereitstellung eines Bildes mit einem vom besagten Kleinbildprozessor verarbeiteten Kleinbildbereich, der in einen vom Großbildprozessor verarbeiteten größeren Bildbereich eingesetzt ist;

einem Eingangsschalter (30) mit einem ersten Zustand zum Anlegen von ihm zugeführten ersten und zweiten Bildeingangssignalen an entsprechende Eingänge des besagten Groß- und Kleinbildprozessors und mit einem zweiten Zustand zum Austauschen der an die besagten Prozessoren angelegten Bildsignale; gekennzeichnet durch

eine veränderliche Höchstwerteinstellschaltung (54, 66, 68, 70, 72, 74, 76), die zwischen einen Chrominanzsignalausgang des besagten Multiplexschalters und einen Chrominanzsignaleingang des besagten Anzeigeprozessors (20) geschaltet ist, wobei die besagte veränderliche Höchstwerteinstellschaltung eine erste Betriebsart zum Anlegen einer ersten Höchstwerteinstellkennlinie (68) an das besagte gemultiplexte Chrominanzsignal, wenn das besagte erste Bildsignal an den besagten Großbildprozessor angelegt ist, aufweist, und sonst eine zweite Betriebsart zum Anlegen einer zweiten Höchstwerteinstellkennlinie (66) an das besagte gemultiplexte Chrominanzsignal aufweist.

2. Farbfernsehempfänger nach Anspruch 1, dadurch gekennzeichnet, daß der besagte Empfänger ein Tuner, einen ZF-Verstärker und eine Detektoreinheit (50, 52) zum Zuführen des besagten ersten Bildsignals zum besagten Eingangsschalter umfaßt; daß die besagte erste Höchstwerteinstellkennlinie (68) einen geneigten Gang innerhalb eines Chrominanzsignalbandes aufweist; und daß die besagte zweite Höchstwerteinstellkennlinie (66) einen im wesentlichen gleichförmigen Gang im besagten Chrominanzsignalband aufweist.

Revendications

1. Récepteur de télévision couleur comprenant:

un processeur d'image dans l'image comportant un processeur de grande image (12), un processeur de petite image (14) et un commutateur multiplex (16) couplé auxdits processeurs pour fournir à un affichage (20,22) des signaux de sortie de luminance et chrominance multiplexés de façon à obtenir une image ayant une zone de petite image traitée par ledit processeur de petite image qui est insérée dans une zone de plus grande image traitée par le processeur de grande image;

un commutateur d'entrée (30) ayant un premier état pour appliquer des premier et second signaux d'entrée vidéo qui lui sont fournis à des entrées respectives desdits processeurs de grande et petite images et ayant un second état pour intervertir les signaux vidéo appliqués aux-

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dits processeurs; caractérisé par:

Un circuit de correction ajustable (54,66,68,70,72,74,76) connecté entre une sortie de signal de chrominance dudit commutateur multiplex et une entrée de signal de chrominance dudit processeur d'affichage (20) ledit circuit de correction ajustable ayant un premier mode de fonctionnement pour appliquer une première caractéristique de correction (68) audit signal de chrominance multiplexé quand ledit premier signal vidéo est appliqué audit processeur de grande image et ayant un second mode de fonctionnement pour appliquer autrement une seconde caractéristique de correction (66) audit signal de chrominance multiplexé.

2. Récepteur de télévision couleur selon la revendication 1, caractérisé en ce que:

ledit récepteur comporte un syntonisateur, un amplificateur FI et une unité de détection (50,52) pour fournir ledit premier signal vidéo audit commutateur d'entrée;

ladite première caractéristique de correction (68) présentant une réponse avec pente au sein d'une bande de signal de chrominance; et

ladite seconde caractéristique de correction (66) présentant une réponse substantiellement uniforme au sein de ladite bande de signal de chrominance.

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