WHAT IS CLAIMED IS:

1. A package structure comprising:

a first encapsulation member comprising a first metal layer, a first insulation layer and a second metal layer, the first metal layer comprising at least one first groove, the first insulation layer being formed between the first metal layer and the second metal layer;

a second encapsulation member comprising a third metal layer, the third metal layer comprising at least one first protrusion disposed at a position corresponding to the at least one first groove;

at least one semiconductor chip disposed between the first encapsulation member and the second encapsulation member and accommodated in the at least one first groove, the at least one semiconductor chip comprising a plurality of conductive terminals connected with the first metal layer or the third metal layer;

a plurality of metal pins disposed between the second encapsulation member and the first encapsulation member and extended outward from the first encapsulation member and the second encapsulation member, the plurality of metal pins being electrically connected with the plurality of conductive terminals respectively; and

a second insulation layer contacted with the plurality of metal pins and disposed between the first encapsulation member and the second encapsulation member for securing the first encapsulation member, the second encapsulation member, the at least one semiconductor chip, and the plurality of metal pins.

2. The package structure according to claim 1, wherein the first metal layer is formed on the first insulation layer and comprises a first part and a second part separated from each other, wherein the at least one

semiconductor chip comprises a first surface, a second surface opposite to the first surface, at least one first conductive terminal of the plurality of conductive terminals and at least one second conductive terminal of the plurality of conductive terminals, wherein the at least one first conductive terminal and the at least one second conductive terminal are disposed on the second surface, the at least one first conductive terminal is connected with the first part of the first metal layer, and the at least one second conductive terminal is connected with the second part of the first metal layer, wherein the second insulation layer comprises a first part, a second part and a third part, wherein the first part of the second insulation layer is disposed among the at least one semiconductor chip, the first part of the first metal layer, the second part of the first metal layer and the first insulation layer, the second part of the second insulation layer is disposed among the at least one semiconductor chip, a metal pin of the plurality of metal pins, the first part of the first metal layer and the third metal layer, and the third part of the second insulation layer is disposed among the at least one semiconductor chip, the second part of the first metal layer and the third metal layer.

3. The package structure according to claim 2, further comprising a first conduction layer disposed between the first encapsulation member and the second encapsulation member, wherein a part of the first conduction layer is connected between the first surface of the at least one semiconductor chip and the third metal layer, and another part of the first conduction layer is connected between a first surface of the metal pin of the plurality of metal pins and the third metal layer.

4. The package structure according to claim 2, further comprising a second conduction layer disposed between the first encapsulation member

and the second encapsulation member and comprising a first part, a second part and a third part, wherein the first part of the second conduction layer is connected between the at least one first conductive terminal and the first part of the first metal layer, the second part of the second conduction layer is connected between the at least one second conductive terminal and the second part of the first metal layer, and the third part is connected between a second surface of the metal pin of the plurality of metal pins and the first metal layer.

5. The package structure according to claim 2, wherein the first metal layer comprises at least one second groove, the at least one first groove and the at least one second groove are located between the first part of the first metal layer and the second part of the first metal layer, wherein the second groove is disposed in the first groove, a portion of the second insulation layer is exposed through the first groove and the second groove, wherein the at least one semiconductor chip is accommodated in the first groove.

6. The package structure according to claim 5, wherein the second encapsulation member further comprises:

a third insulation layer formed on the third metal layer; and

a fourth metal layer formed on the third insulation layer.

7. The package structure according to claim 6, wherein the first metal layer comprises at least one second groove and at least one third groove, and the third metal layer comprises at least one fourth groove, wherein portion of the first insulation layer is exposed through the third groove, portion of the third insulation layer is exposed through the fourth groove, and the at least one third groove is corresponding in position to the at least one fourth groove, wherein the third part of the second insulation layer is disposed in the third groove and the fourth groove and is disposed among

the second part of the first metal layer, the first insulation layer, the semiconductor chip, the third metal layer and the third insulation layer.

8. The package structure according to claim 4, wherein the at least one second conductive terminal of the semiconductor chip comprises a plurality of second conductive terminals, wherein the package structure further comprises:

at least one first conductive pillar connected with the at least one first conductive terminal of the semiconductor chip and the first part of the second conduction layer; and

a plurality of second conductive pillars connected between the plurality of the second conductive terminals of the semiconductor chip and the second part of the second conduction layer.

9. The package structure according to claim 4, wherein the at least one second conductive terminal of the semiconductor chip comprises a plurality of second conductive terminals, wherein the package structure further comprises:

a first conductive pillar connected with the first conductive terminal of the semiconductor chip and the first part of the second conduction layer; and

a second conductive pillar connected between the plurality of the second conductive terminals of the semiconductor chip and the second part of the second conduction layer.

10. The package structure according to claim 2, wherein the first surface of the semiconductor chip is coplanar with one surface of the metal pin.

11. The package structure according to claim 2, further comprising a first conduction layer connected between the first surface of the at least one semiconductor chip and the third metal layer, wherein the second part of

the second insulation layer is disposed among the first part of the first metal layer, the metal pin, the third metal layer and the at least one semiconductor chip.

12. The package structure according to claim 2, wherein the metal pin includes a first part and a second part, wherein the first part of the metal pin is partially disposed between the first part of the first conduction layer and the third metal layer, and the second part of the metal pin is vertically connected with one end of the first part of the metal pin.

13. The package structure according to claim 1, further comprising an insulation structure disposed on lateral sides of the first encapsulation member and the second encapsulation member, wherein the metal pin is partially embedded in the insulation structure.

14. The package structure according to claim 1, wherein the first metal layer comprises at least one recess, wherein a part of the metal pin is disposed in the recess.

15. The package structure according to claim 1, further comprising a spacer disposed between the first metal layer and the third metal layer for electrically connecting the first metal layer and the third metal layer.

16. The package structure according to claim 15, wherein the top surface of the spacer is coplanar with a first surface of the semiconductor chip.

17. The package structure according to claim 1, further comprising a housing covering the second encapsulation member and comprising an accommodation space and an opening in communication with the accommodation space, wherein the second encapsulation member is accommodated in the accommodation space, and portion of the second encapsulation member is exposed through the opening.

18. The package structure according to claim 1, further comprising at least one heat dissipation device disposed on one surface of the first encapsulation member or one surface of the second encapsulation member.

19. The package structure according to claim 1, wherein the at least one semiconductor chip is a flip-chipped integrated circuit chip.