## CLAIMS

1. An unterminated endpoint for a first die, comprising: a pad; a driver having an active mode in which the driver is configured to drive signals over the pad to a remote die; a receiver having an active mode in which the receiver is configured to receive signals over the pad from the remote die; a capacitor; a switch connected to the capacitor, wherein the switch is configured to couple the pad to ground through the capacitor while the switch is closed and to not couple the pad to ground through the capacitor while the switch is open; and a controller configured to close the switch while the receiver is in the active mode and to open the switch while the driver is in the active mode.

2. The unterminated endpoint of claim 1, wherein the controller is further configured to close the switch only while both the receiver is in the active mode and a data rate for the receiver is above a threshold value.

3. The unterminated endpoint of claim 1, wherein the capacitor comprises a gate of a transistor.

4. The unterminated endpoint of claim 1, wherein the switch is connected between the capacitor and ground.

5. The unterminated endpoint of claim 1, wherein the capacitor comprises a plurality of capacitors, and wherein the switch comprises a plurality of switches corresponding on a one-to-one basis with the plurality of capacitors.

6. The unterminated endpoint of claim 1, wherein the controller is further configured to selectively close switches from the plurality of switches to tune a capacitive load from the capacitors while the receiver is in the active mode.

7. The unterminated endpoint of claim 1, wherein the switch comprises an NMOS transistor, and wherein the controller is configured to close the switch by charging a gate of the NMOS transistor.

8. The unterminated endpoint of claim 1, wherein the first die is a system-on-a-chip (SoC) die and wherein the remote die is a dynamic random access memory (DRAM) die.

9. The unterminated endpoint of claim 8, wherein the SoC die is integrated within a bottom package of a package-on-package integrated circuit and wherein the DRAM die is integrated within a top package of the package-on-package integrated circuit.

10. The unterminated endpoint of claim 9, wherein the DRAM die is a low power double data rate (LPDDR) DRAM die.

11. The unterminated endpoint of claim 1, wherein the DRAM die comprises a plurality of DRAM dies.

12. A method, comprising: while receiving first signals at a pad for an unterminated endpoint in a first die, closing a switch to load the pad with a capacitance from a capacitor; and while transmitting second signals from the pad for the unterminated endpoint in the first die to a remote die, opening the switch to not load the pad with the capacitance.

13. The method of claim 12, wherein receiving the first signals occurs at a first data rate above a threshold value, the method further comprising: while receiving third signals at the pad, opening the switch, wherein receiving the third signals occurs at a second data rate below the threshold value.

14. The method of claim 12, wherein closing the switch connects the pad to ground through a gate capacitance of a transistor to capacitively load the pad for the unterminated endpoint.

15. The method of claim 14, wherein closing the switch connects a drain and source of the transistor to ground.

16. The method of claim 14, wherein opening the switch isolates the gate capacitance of the transistor from ground.

17. The method of claim 12, further comprising: tuning a capacitance for the capacitor to adjust the capacitive loading of the pad.

18. An unterminated endpoint for a die, comprising: a pad; a driver having an active mode in which the driver is configured to drive signals over the pad to a remote die; a receiver having an active mode in which the receiver is configured to receive signals over the pad from the remote die; a capacitor; and means for loading the pad with a capacitance from the capacitor while the receiver is in the active mode and a data rate for the receiver is above a threshold value and for isolating the pad from the capacitor while the driver is in the active mode or while the receiver is in the active mode and a data rate for the receiver is below a threshold value.

19. The unterminated endpoint of claim 18, wherein the capacitor comprises a gate for a transistor.

20. The unterminated endpoint of claim 19, wherein the transistor comprises an NMOS transistor.