

CONFIGURABLE INPUTS AND OUTPUTS FOR MEMORY STACKING SYSTEM AND METHOD

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates generally to memory devices having stacked die configurations with configurable inputs and outputs (I/O). Specific embodiments relate to stacked die configurations without requiring redistribution layers (RDLs) to allow through wafer interconnects (TWIs) or edge bonding. Indeed, embodiments of the present invention relate to die that incorporate path selectors, which enable configuration of each die for a particular stacking requirement.

2. Description Of The Related Art

This section is intended to introduce the reader to various aspects of art that may be related to various aspects of the present invention, which are described and/or claimed below. This discussion is believed to be helpful in providing the reader with background information to facilitate a better understanding of the various aspects of the present invention. Accordingly, it should be understood that these statements are to be read in this light, and not as admissions of prior art.

Processing speeds, system flexibility, and size constraints are typically considered by design engineers tasked with developing computer systems and system components. Computer systems typically include a plurality of memory devices which may be used to store programs and data and which may be accessible to other system

components such as processors or peripheral devices. Typically, memory devices are grouped together to form memory modules such as dual-inline memory modules (DIMMs). Computer systems may incorporate numerous modules to increase the storage capacity of the system.

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Die stacking has recently emerged as a powerful tool for satisfying requirements for increased memory storage capacity within restricted packaging space. Die stacking includes the process of mounting multiple chips on top of one another within a single semiconductor package. Packages having a number of vertically stacked chips or die in a single package (i.e., die stacking) advantageously increase the amount of memory that can be located within a given footprint on the substrate or printed circuit board on which the die stack is arranged. Further, die stacking may enable shorter routing interconnects from chip to chip, thus increasing signal speeds between chips, reducing noise, and reducing cross-talk. Another benefit of die stacking is that surface-mount to printed circuit board assembly is simplified because fewer components are required to be placed on the printed circuit board.

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As processing demands and storage capacity continue to increase, while system size continues to decrease, die stacking is becoming increasingly useful for different memory configurations. For example, requirements for dynamic random access memory (DRAM) configurations can make it desirable or even necessary to stack die to increase density or to increase I/O widths. Current stacking techniques generally require inclusion of a redistribution layer (RDL) on each DRAM to allow through wafer interconnect (TWI) or edge bonding. It should be noted that inclusion of such an RDL

adds costs. Additionally, inclusion of an RDL generally requires uniquely configured die to be used within a die stack for certain stack elements. Indeed, to accommodate stacking requirements for each particular die, each layer of a die stack will typically have a different RDL configuration.

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Embodiments of the present invention may address one or more of the problems set forth above.

BRIEF SUMMARY

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Techniques for providing and implementing configurable I/O in stacked die are provided. Specifically, embodiments of the present technique include making input signals in stacked die configurable using path selectors, which can be set as desired for a particular stacking requirement. For example, path selectors may be coupled with TWIs and enabled to accommodate a stacking requirement for a particular die stack such that each of the die in the stack receives the correct control signals. The path selectors may be enabled using a path selector control circuit that designates one of multiple signals to establish a signal path (e.g., via a multiplexer). It should be noted that I/O signals can be configurable between bytes to allow wide I/O configurations.

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BRIEF DESCRIPTION OF THE DRAWINGS

Advantages of the invention may become apparent upon reading the following detailed description and upon reference to the drawings in which:

Fig. 1 illustrates a block diagram of an exemplary processor-based system;

Fig. 2 illustrates an exemplary memory sub-system in accordance with
embodiments of the present invention;

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Fig. 3 is a block diagram of two x4 memory devices arranged in two ranks of
x4 devices which may be configured in accordance with embodiments of the present
invention;

10 Fig. 4 illustrates four x8 memory devices arranged in two ranks of x16 devices
which may be configured in accordance with embodiments of the present invention;

Fig. 5 illustrates four x4 memory devices arranged in four ranks of x4 devices
which may be configured in accordance with embodiments of the present invention;

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Fig. 6 illustrates a single rank of two x16 memory devices which may be
configured in accordance with embodiments of the present invention;

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Fig. 7 is a diagrammatical view of a die stack associated with Fig. 5 and
employing a number of redistribution layers;

Fig. 8 is a diagrammatical view of a configurable die stack associated with Fig.
5 and formed from four die in accordance with embodiments of the present invention;

Fig. 9 is a block diagram of four path selectors in accordance with embodiments of the present invention;

Fig. 10 is a block diagram illustrating a CKE path selector having a path selector control circuit that is fuse controlled in accordance with embodiments of the present invention; and

Figs. 11-14 is a block diagram of path selectors and selected paths in each of four die in a die stack associated with Fig. 8 in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

One or more specific embodiments of the present invention will be described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

Turning now to the drawings, and referring initially to Fig. 1, a block diagram depicting an exemplary processor-based system, generally designated by reference numeral 10, is illustrated. The system 10 may be any of a variety of types such as a computer, pager, cellular phone, personal organizer, control circuit, etc. In a typical processor-based system, one or more processors 12, such as microprocessor, control the processing of system functions and requests in the system 10.

The system 10 typically includes a power supply 14. For instance, if the system 10 is a portable system, the power supply 14 may advantageously include permanent batteries, replaceable batteries, and/or rechargeable batteries. The power supply 14 may also include an AC adapter, so the system 10 may be plugged into a wall outlet, for instance. The power supply 14 may also include a DC adapter such that the system 10 may be plugged into a vehicle cigarette lighter, for instance. Various other devices may be coupled to the processor 12 depending on the functions that the system 10 performs. For instance, a user interface 16 may be coupled to the processor 12. The user interface 16 may include buttons, switches, a keyboard, a light pen, a mouse, and/or a voice recognition system, for instance. A display 18 may also be coupled to the processor 12. The display 18 may include an LCD display, a CRT, LEDs, and/or an audio display, for example. Furthermore, an RF sub-system/baseband processor 20 may also be couple to the processor 12. The RF sub-system/baseband processor 20 may include an antenna that is coupled to an RF receiver and to an RF transmitter (not shown). One or more communication ports 22 may also be coupled to the processor 12. The communications port 22 may be adapted to be coupled to one or more peripheral devices 24 such as a modem, a

printer, a computer, or to a network, such as a local area network, remote area network, intranet, or the Internet, for instance.

The processor 12 generally controls the system 10 by implementing software programs stored in the memory. The memory is operably coupled to the processor 12 to store and facilitate execution of various programs. For instance, the processor 12 may be coupled to the volatile memory 26 which may include DRAM and/or static random access memory (SRAM). The volatile memory 26 is typically quite large so that it can store dynamically loaded applications and data. As described further below, the volatile memory 26 may be configured in a stacked orientation in accordance with embodiments of the present invention.

The processor 12 may also be coupled to non-volatile memory 28. The non-volatile memory 28 may include a read-only memory (ROM), such as an EPROM, and/or flash memory to be used in conjunction with the volatile memory. The size of the ROM is typically selected to be just large enough to store any necessary operating system, application programs, and fixed data. Additionally, the non-volatile memory 28 may include a high capacity memory such as a tape or disk drive memory.

Fig. 2 generally illustrates a block diagram of a portion of a memory subsystem, such as the volatile memory 26. A memory controller 30 is generally provided to facilitate access to storage devices in the volatile memory. The memory controller 30 may receive requests to access the storage devices via one or more processors, such as the processor 12, via peripheral devices, such as the peripheral

device 24, and/or via other systems. The memory controller 30 is generally tasked with facilitating the execution of the requests to the memory devices and coordinating the exchange of information, including configuration information, to and from the memory devices.

5 The memory sub-system may include a plurality of slots 32, 34, 36, 38, 40, 42, 44, and 46. Each slot 32 – 46 is configured to operably couple a memory module, such as a dual-inline memory module (DIMM), to the memory controller 30 via one or more memory buses. Each memory module generally includes a plurality of memory
10 devices such as DRAM devices capable of storing data. Each memory module has a number of memory devices arranged in “ranks.” Ranks traditionally include the arrangement of memory devices on each opposing side of the module. However, in accordance with present embodiments, multiple ranks may be disposed on a single side (e.g., in a stacked configuration). Accordingly, each slot 32 – 46 may be
15 configured to receive a single memory module having two ranks. For instance, the slot 32 is configured to receive a memory module having ranks 32A and 32B, the slot 34 is configured to receive a DIMM having ranks 34A and 34B, and so forth. In the present exemplary embodiment, each of the eight memory slots 32 – 46 is capable of supporting a module comprising eight individual memory devices on each rank 32A/B
20 – 46A/B. As will be appreciated, and as describe further below, each memory module may include four or more ranks.

Referring again to Fig. 2, the memory buses may include a memory data bus 48 to facilitate the exchange of data between each memory device on the DIMMs and

the memory controller 30. The memory data bus 48 may comprise a plurality of single bit data buses (e.g., DQ0-DQ63) each coupled from the memory controller 30 to a memory device. In one embodiment of the volatile memory 26, the memory data bus 48 may include 64 individual data buses. Further, the memory data bus 48 may include one or more individual buses to each memory rank 32A/B – 48A/B which may be used for ECC error detection and correction. As can be appreciated by those skilled in the art, the individual buses of the memory data bus 48 will vary depending on the configuration and capabilities of the system 10.

The volatile memory 26 also includes a command bus 50 on which address information such as command address (CA), row address select (RAS), column address select (CAS), write enable (WE), bank address (BA), chip select (CS), clock enable (CKE), and on-die termination (ODT), for example, may be delivered for a corresponding request. Further, the command bus 50 may also be used to facilitate the exchange of configuration information at boot-up. As with the memory data bus 48, the command bus 50 may comprise a plurality of individual command buses. In the present embodiment, the command bus 50 may include 20 individual buses. As previously described with reference to the memory data bus 48, a variety of embodiments may be implemented for the command bus 50 depending on the system configuration.

Fig. 3 is a block diagram of two memory devices 54 and 56 arranged in two ranks in accordance with embodiments of the present invention. Specifically, Fig. 3 illustrates two DRAM devices which each have a “x4” (by 4) bit memory width. The

DRAMs are arranged as two ranks of x4 memory in accordance with present embodiments, which are discussed in further detail below. Each DRAM includes four data input/output pins (DQ0-3), which are configured to receive data signals, such as data signals DQ0-3_{signal}. Additionally, each DRAM includes a number of control input pins. In the illustrated embodiment, the control input pins include a chip select pin (CS), a clock enable pin (CKE), an on-die termination pin (ODT), and a calibration input pin (ZQ). Each of the control input pins is configured to receive a control signal, such as the control signals CS_{signal}, CKE_{signal}, ODT_{signal}, ZQ_{signal}, sCS_{signal}, sCKE_{signal}, sODT_{signal}, and sZQ_{signal}, wherein the prefix "s" refers to a stacked signal. It should be noted that each DRAM includes a lower data strobe (LDQS) and a lower data mask (LDM). It should also be noted that V_{ss} represents power. Each of the control input pins, data input/output pins and control signals will be recognized by one of ordinary skill in the art.

As set forth above, the two x4 DRAMs in Fig. 3 are arranged as two ranks of x4 memory. In one embodiment, these two x4 DRAMs are disposed in a stacked orientation on a single side of a memory module. As one of ordinary skill in the art will recognize, different arrangements of memory may be utilized to increase storage, the number of available data pins, and so forth. Indeed, Figs. 4-6 are illustrative of such embodiments. For example, Fig. 4 illustrates four x8 memory devices (e.g., DRAMs) arranged in two ranks of x16 bit width. The memory configuration illustrated in Fig. 4 have a greater widths than those of Fig. 3 and include additional data input/output pins (DQ0-7 and DQ8-15). Fig. 5 illustrates four x4 devices arranged in four ranks of x4 bit width memory, wherein additional chip select signals

sCS1, sCS2, and sCS3 are employed for the additional ranks. Fig. 6 illustrates a single rank of x32 memory built from two x16 memory devices. The memory configuration illustrated in Fig. 6 has a greater width than that of Fig. 3 and accordingly includes additional data input/output pins (DQ0-15 and DQ16-31).

Fig. 7 is a diagrammatical view of a die stack 60 having four die that is illustrative of issues addressed by embodiments of the present invention. Specifically, the die stack 60 includes two ranks of x16 built from four x8 devices. Further, the die stack 60 comprises RDLs disposed on three of the four die. Indeed, Fig. 7 illustrates a first die 62 having a first RDL 64 disposed thereon, a second die 66 having a second RDL 68 disposed thereon, a third die 70 having no RDL, and a fourth die 74 having a third RDL 76 disposed thereon. It should be noted that each die 62, 66, 70, and 74 is distinct from the others because of the different configurations of the associated RDLs 64, 68, and 76 or the lack of an RDL (die 70) disposed on each die. Fig. 7 also illustrates Lower DQs and Upper DQs along with arrows 78 and 80, which are representative of data flow.

Because the external control signals (e.g., CKE_{signal} , CS_{signal} , SCS_{signal} , ODT_{signal} , ZQ_{signal} , and sZQ_{signal}) originate from outside of the die stack 60 and enter the die stack 60 from an underlying substrate or PCB (not shown) through the bottom die 62, it is desirable to provide routing through the die stack 60 to allow the desired signals to reach the control inputs for each die. The RDLs 64, 68, and 76 operate to direct the signals to appropriate pins (e.g., CKE, Dum0, CS, Dum1, ODT, Dum2, ZQ, or Dum3) on each die. For example, the CS_{signal} control signal enables the CS control

input pins on the first die 62 and the fourth die 74. However, the CS pins on the second die 66 and third die 70 are enabled by the sCS_{signal} control signal, rather than the CS_{signal} control signal. Accordingly, the RDLs are utilized to route the CS_{signal} and sCS_{signal} signals to the appropriate pins. Specifically, for example, the first RDL 64 routes the CS_{signal} signal from the CS pin on the first die 62 to an available pin, such as Dum0, on the first die 62. As will be appreciated, Dum0 – Dum3 represent unassigned or unused pins on each die 62, 66, 70, and 74. The Dum0 pin on the first die 64 is coupled to other Dum0 pins on dies 66 and 70, thus establishing a communication route that passes through both the second die 66 and third die 70 to the RDL 76 on the fourth die 74. The RDL 76 on the fourth die 74 routes the CS_{signal} signal to the CS pin on the fourth die 74, thus enabling it. While this is a simple example, one of ordinary skill in the art will recognize that the RDLs also provide similar routing through the die stack 60 to enable other control input pins with the corresponding required signals.

As noted above, providing RDLs (e.g., 64, 68, and 76) within a die stack (e.g., 60) can be beneficial because it enables communication of external signals to appropriate pins within the die stack. However, the use of RDLs can be expensive and inefficient. For example, as noted above, each of the die 62, 66, 70, and 74 are different because each requires a different RDL configuration to enable the appropriate pins throughout the die stack 60. Accordingly, separate processes, equipment, material, and procedures are required to provide each of the die configurations. This may not be desirable. Accordingly, embodiments of the present

invention facilitates the provision of die that are fabricated equivalent to one another but that can be configured to meet the requirements of a particular die stack element.

Fig. 8 is a diagrammatical view of a configurable die stack 90 formed from
5 four die in accordance with embodiments of the present invention. Specifically, the die stack 90 includes two ranks of x16 memory built from four x8 devices, which include a first configurable die 92, a second configurable die 94, a third configurable die 96, and a fourth configurable die 98. The die stack 90 does not require that RDLs be disposed on any of the die to enable signal routing, as in Fig. 7. Advantageously,
10 in accordance with embodiments of the present invention, the configurable die (i.e., 92, 94, 96, and 98) incorporate path selectors 100 (e.g., multiplexer devices) that facilitate die customization. It should be noted that each configurable die 92, 94, 96, and 98 may be initially indistinct from the others (e.g., no path selections in the die having been activated). Thus, the fabrication of each die 92, 94, 96, and 98 is
15 essentially identical. However, in the embodiment illustrated by Fig. 8, the die 92, 94, 96, and 98 have been customized by activating the path selectors 100. Specifically, the die 92, 94, 96, and 98 have been customized to operate like the die illustrated by Fig. 7 without using RDLs. In other words, the path selectors 100 have been activated such that they function similarly to the RDLs in Fig. 7. The path selectors 100 will be
20 described in more detail with regard to Figs. 9-11. In the interest of providing context, it should be noted that Fig. 8 also illustrates Lower DQs and Upper DQs on each of the die.

Because the external signals (e.g., CKE_{signal} , CS_{signal} , sCS_{signal} , ODT_{signal} , ZQ_{signal} , and sZQ_{signal}) originate from outside of the configurable die stack 90 and enter the die stack 90 through the bottom die 92, it is desirable to provide routing through the die stack 90 to allow the desired signals to reach the control inputs for each die. It is also desirable to achieve this without using RDLs and without requiring that each die be uniquely manufactured. Accordingly, the illustrated embodiment includes the path selectors 100, which can be configured such that they direct the signals to appropriate pins (e.g., CKE, Dum0, CS, Dum1, ODT, Dum2, ZQ, or Dum3). For example, the CS_{signal} control signal enables the CS control input pin on the first die 92 and on the fourth die 98. However, the CS pins on the second die 94 and third die 96 are enabled by the sCS_{signal} control signal, not the CS_{signal} control signal. Accordingly, the path selectors 100 are enabled such that they can be utilized to route the CS_{signal} and sCS_{signal} signals to the appropriate pins while avoiding inappropriate pins.

In the embodiment illustrated by Fig. 8, the path selectors 100 coupled between the CS pins and the Dum 1 pins of the first die 92 and fourth die 98 are configured such that they route the CS_{signal} signal from the CS pins on the first and fourth dies 92 and 98 to the related circuits 102 and 104 on each die. Correspondingly, the path selectors 100 coupled between the CS pins and the Dum 1 pins of the second die 94 and third die 96 cause the CS_{signal} signal to bypass the related circuits 106 and 108 on each die. It is desirable for the circuits 106 and 108 to be bypassed by the CS_{signal} signal because they are enabled by the sCS_{signal} signal, not the CS_{signal} signal. The opposite path selector configuration is implemented for the

sCS_{signal} signal route. For example, the fuse 100 between the CS and Dum1 pins of the second die 94 is burned such that the corresponding circuit receives the sCS_{signal} signal rather than the CS_{signal} signal, as illustrated. While this is a simple example, one of ordinary skill in the art will recognize that the path selectors 100 may also provide similar routing, as illustrated in Fig. 8 and more clearly described below, through the die stack 90 to enable other control input pins with corresponding signals.

Fig. 9 is a block diagram of four path selectors 100 in accordance with embodiments of the present invention. Specifically, Fig. 9 illustrates a CKE path selector 120, a CS path selector 122, a ZQ path selector 124, and an ODT path selector 126. Each of the path selectors 120, 122, 124, and 126 incorporates a multiplexer to facilitate signal path selection. For example, the CKE path selector 120 and the ZQ path selector 124 incorporate two-to-one multiplexers 128, the ODT path selector 126 incorporates a three-to-one multiplexer 130, and the CS path selector 122 incorporates a four-to-one path selector 132. It should be noted that the sCS1 and sCS2 signal inputs on the CS path selector 122 may not be utilized if the die does not support quadrank.

In operation, the path selectors 100 receive signals (e.g., CKE_{signal} and sCKE_{signal}), that pass through buffers 134 (with exception to the ZQ path selector 124) and into the multiplexer (e.g., 128, 130, and 132), which designates a signal path. The selected signal then enables the corresponding circuit 136. As will be appreciated, each circuit 136 simply represents the active ICS that are associated and enabled by each of the respective control signals. The path selectors 100 may be fuse controlled

(e.g., using a fuse or an antifuse) or may utilize mode register select (MRS) to implement path selection. For example, Fig. 10 is a block diagram illustrating the CKE path selector 120 having a path selector control circuit 140 that is fuse controlled. The path selector control circuit 140 provides a signal to a select input 142 of the multiplexer 128 depending on a condition of a fuse 144. The fuse 144 is either blown (open) or not blown (short) to select which signal (i.e., CKE_{signal} or $sCKE_{signal}$) will pass through the multiplexer 128 and into the related circuit 136. When the fuse 144 is blown, the signal to the select input is pulled high (e.g., a value of 1) by a weak pullup transistor 146. If the fuse 144 is not blown, the signal to the select input 142 is pulled low (e.g., a value of 0) to ground 148. As one of ordinary skill in the art will recognize an antifuse may be utilized in other embodiments to achieve the same or similar functionality. Further, while a single example is illustrated by Fig. 10, other embodiments may utilize similar path selection schemes and path selector control circuits, as illustrated in Fig. 11.

Figs. 11-14 are block diagrams of the path selectors 100 and selected paths 160 in each of the four die discussed above with respect to Fig. 8. Specifically, the columns of path selectors 100 in Figs. 11-14 are representative of the die 92, 94, 96, and 98 in Fig. 8 respectively. For example, the CKE path selector 120 of the first die in Fig. 11 indicates that the CKE_{signal} signal is passed through the multiplexer 128 and into the corresponding circuit 136 based on its path selector control circuit 140 and so forth, as described above. Additionally, Figs. 11-14 illustrate path selectors 100 and selected paths 160 for the data input/output pins (DQ0-7 and DQ8-15). It should be

noted that in the illustrated embodiment, the path selectors 100 for the data input/output pins include two-to-one demultiplexers.

While the invention may be susceptible to various modifications and
5 alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended
10 claims.

CLAIMS

1. A memory device comprising:
 - a first die including a top surface and a bottom surface separated by a thickness, the first die configured to receive a control signal through a first path disposed through the first die in a direction generally parallel to the thickness and a second path disposed through the first die in a direction generally parallel to the thickness;
 - a circuit included in the first die, the circuit configured to be enabled by the control signal via the first path or the second path;
 - a path selector configured to select the first path or the second path; and
 - a second die communicatively coupled to the first die.
2. The memory device of claim 1, comprising a first set of input pins enclosing the first path and a second set of input pins enclosing the second path.
3. The memory device of claim 2, wherein the input pins comprise solder balls disposed on the top and bottom surfaces of the die.
4. The memory device of claim 1, wherein the path selector comprises a multiplexer.
5. A memory module comprising:
 - a die configured to route a plurality of control signals through the die along paths from bottom pins disposed on a bottom surface of the die to top pins disposed on a top surface of the die, wherein the paths are disposed transverse to an axis generally parallel to the top surface and the bottom surface, and wherein the die is configured to support a quadrank configuration;
 - a circuit disposed within the die and configured to be enabled by an enabling signal selected from the plurality of control signals; and

a path selector arranged between the paths and the circuit, the path selector being configured to selectively couple one of the paths to the circuit.

6. The memory module of claim 5, wherein the bottom pins are configured to receive the plurality of control signals.
7. The memory module of claim 5, wherein the path selector comprises a four-to-one multiplexer.
8. The memory module of claim 5, comprising a memory controller configured to transmit the plurality of control signals to the die.
9. The memory module of claim 5, wherein the path selector includes a control circuit comprising a fuse.
10. The memory module of claim 5, wherein the plurality of signals include a chip select signal, a clock enable signal, an on-die termination signal, and a calibration signal.
11. A die stack comprising:
 - a plurality of memory devices stacked to form a plurality of signal paths through the memory devices from a bottom of the die stack to a top of the die stack, wherein the paths are disposed internally within the die stack in a direction generally transverse to the die stack;
 - a plurality of pins disposed along the signal paths and between the memory devices, wherein the plurality of pins are configured to transmit control signals between the devices;
 - a plurality of circuits disposed within each of the plurality of memory devices, each of the plurality of circuits being electrically coupled to a respective assigned path selected from the plurality of signal paths; and
 - a plurality of path selectors disposed between the circuits and the signal paths, the plurality of path selectors configured to select the respective assigned path for each of the

plurality of circuits and to electrically couple each of the plurality of circuits to the respective assigned path.

12. The die stack of claim 11, wherein one of the path selectors comprises a two-to-one multiplexer, one of the path selectors comprises a three-to-one multiplexer, and one of the path selectors comprises a four-to-one multiplexer.

13. The die stack of claim 11, wherein the signal paths are configured to receive the control signals and the control signals include a chip select signal, a clock enable signal, an on-die termination signal, a calibration signal, and stacked versions thereof.

14. The die stack of claim 11, wherein an arrangement of the plurality of circuits is identical within each of the plurality of memory devices.

15. The die stack of claim 11, wherein the die stack is configured in a two rank configuration.

16. The die stack of claim 11, wherein the pins include solder balls electrically coupled to the memory devices.

17. A computer system comprising :
a processor; and
a memory system coupled to the processor, wherein the memory system comprises:
a memory controller;
a memory device having a first surface and a second surface positioned opposite the first surface;
a circuit disposed within the memory device, the circuit configured to be coupled to a plurality of generally parallel signal paths disposed within the memory device, wherein the signal paths are configured to route control signals through the die from the first surface to the second surface;

a path selector arranged between the plurality of signal paths and the circuit and configured to couple the circuit to an assigned path selected from the plurality of signal paths; and

a plurality of input pins disposed on the first surface of the memory device configured to transmit the control signals to the plurality of signal paths, wherein the signal paths are configured to transmit the control signals within the device from the input pins disposed on the first surface to input pins disposed on the second surface.

18. The memory system of claim 17, wherein the memory device comprises at least one path selector control circuit comprising a fuse or antifuse, the path selector control circuit being configured to control the path selector and determine the assigned path.

19. The memory system of claim 17, wherein the memory device comprises a die stack configured as four ranks of memory.

20. A memory module comprising:

a die configured to route a plurality of control signals through the die along paths from bottom pins disposed on a bottom surface of the die to top pins disposed on a top surface of the die, wherein the paths are disposed transverse to an axis generally parallel to the top surface and the bottom surface;

a circuit disposed within the die and configured to be enabled by an enabling signal selected from the plurality of control signals; and

a path selector arranged between the paths and the circuit, the path selector comprising a four-to-one multiplexer and being configured to selectively couple one of the paths to the circuit.

21. The memory module of claim 20, wherein the bottom pins are configured to receive the plurality of control signals.

22. The memory module of claim 20, comprising a memory controller configured to transmit the plurality of control signals to the die.
23. The memory module of claim 20, wherein the path selector includes a control circuit comprising a fuse.
24. The memory module of claim 20, wherein the plurality of signals include a chip select signal, a clock enable signal, an on-die termination signal, and a calibration signal.
25. A computer system comprising :
a processor; and
a memory system coupled to the processor, wherein the memory system comprises:
a memory controller;
a memory device having a first surface and a second surface positioned opposite the first surface, wherein the memory device comprises a die stack configured as four ranks of memory;
a circuit disposed within the memory device, the circuit configured to be coupled to a plurality of generally parallel signal paths disposed within the memory device, wherein the signal paths are configured to route control signals through the die from the first surface to the second surface;
a path selector arranged between the plurality of signal paths and the circuit and configured to couple the circuit to an assigned path selected from the plurality of signal paths; and
a plurality of input pins disposed on the first surface of the memory device configured to transmit the control signals to the plurality of signal paths.
26. The memory system of claim 25, wherein the memory device comprises at least one path selector control circuit comprising a fuse or antifuse, the path selector control circuit being configured to control the path selector and determine the assigned path.