USING PATTERNS AS ALIGNMENT MARKERS

BACKGROUND

Field

[0001] Embodiments described herein generally relate to semiconductor processing. More specifically, embodiments described herein relate to using patterns on a die formed on a semiconductor substrate (e.g., wafer) or using patterns from previous layers of materials placed on the substrate as an alignment marker.

Description of the Related Art

[0002] Many steps of the semiconductor manufacturing process require highly precise alignment, such as the photolithography process, substrate probe and test, substrate mounting, and dicing. To meet industry demand, semiconductor manufacturers use high-speed automation production systems that require minimal intervention. Poorly performing vision alignment systems stop more frequently for manual intervention and maintenance, which disrupts the production process and adds to support costs. In addition to production inefficiencies, poor alignment can decrease substrate yields and electrical functionality of die circuits.

[0003] Accordingly, what is needed in the art are improved methods for creating alignment markers.

SUMMARY

[0004] Embodiments of the present disclosure provide a method including capturing images of features on a die formed on a semiconductor substrate, extracting patterns from a portion of each captured image, and combining the patterns to form an alignment marker. In one example, the images are captured from four corners of the die. In another example, the images are captured from side regions of the die. In yet another example, the images are captured from a plurality of different central and non-central regions of the die. In one example, the patterns are combined in a tile format. In another example, the patterns are combined in a cross geometry. The patterns from the portion of each captured image are compared to other patterns on the die to determine uniqueness of the patterns. The patterns are circuit designs. The

alignment marker facilitates precise alignment of lithographic masks. The alignment marker is stored in a memory device and retrieved when lithographic mask alignment positioning is performed.

[0005] Embodiments of the present disclosure provide a method including capturing images on a semiconductor substrate, extracting, from the images captured, patterns from previous material layers placed on the semiconductor substrate, and combining the patterns extracted from the previous material layers placed on the semiconductor substrate to form an alignment marker.

[0006] Embodiments of the present disclosure provide an alignment marker generator including a camera to capture images of features on a die of a plurality of dies formed on a semiconductor substrate or directly from the semiconductor substrate, a pattern extractor to extract patterns from a portion of each captured image, and a pattern assembler to combine the extracted patterns to form an alignment marker. In one example, the images are captured from four corners of the die. In another example, the images are captured from side regions of the die. In yet another example, the images are captured from a plurality of different central and non-central regions of the die. In one example, the patterns are combined in a tile format. In another example, the patterns are combined in a cross geometry. The patterns from the portion of each captured image are compared to other patterns on the die to determine uniqueness of the patterns. The alignment marker facilitates precise alignment of lithographic masks. The alignment marker is stored in a memory device and retrieved when lithographic mask alignment positioning is performed. In another example embodiment, patterns are extracted from the substrate itself, and not from dies placed on the substrate. That is, the patterns can be extracted from previous layers of materials placed on the substrate before placing the dies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended

drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, and may admit to other equally effective embodiments.

[0008] Figure 1A illustrates taking snapshots of portions on a die to extract patterns, according to one or more of the embodiments described herein.

[0009] Figure 1B illustrates forming an alignment marker by combining portions of the patterns from the snapshots of the portions of the die, according to one or more of the embodiments described herein.

[0010] Figures 1C-1E illustrate different shapes and sizes of the alignment marker.

[0011] Figure 2 illustrates a circular semiconductor substrate with a plurality of die formed thereon, where patterns from at least one die are used to form an alignment marker, according to one or more of the embodiments described herein.

[0012] Figure 3 illustrates a rectangular panel with a plurality of die formed thereon, where patterns from at least one die are used to form an alignment marker, according to one or more of the embodiments described herein.

[0013] Figure 4 is a flowchart for implementing a method to create an alignment marker from portions of patterns extracted from one or more die, according to one or more of the embodiments described herein.

[0014] Figure 5 is a flowchart for implementing a method to create an alignment marker from extracted patterns, according to one or more of the embodiments described herein.

[0015] Figure 6 is an alignment marker generator for generating a single alignment marker from multiple patterns of a die formed on a semiconductor substrate, according to one or more of the embodiments described herein.

[0016] Figure 7A illustrates a substrate including a plurality of patterns from previous layers of materials and taking snapshots of portions of the patterns on the substrate, according to one or more embodiments described herein.

[0017] Figure 7B illustrates forming an alignment marker by combining portions of the patterns from the snapshots taken of the portions of the substrate, according to one or more embodiments described herein.

[0018] Figure 7C illustrates a shape of the alignment marker after combining patterns from the substrate, according to one or more embodiments described herein.

[0019] Figure 8 illustrates an alignment marker generator for generating a single alignment marker from multiple patterns on a semiconductor substrate, according to one or more of the embodiments described herein.

[0020] Figure 9 illustrates a flowchart for implementing a method to create an alignment marker from portions of patterns extracted from the semiconductor substrate, according to one or more of the embodiments described herein.

[0021] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0022] Embodiments of the present disclosure generally relate to improving semiconductor manufacturing by implementing new methodologies for aligning different layers or materials or structures during the fabrication process. The new methodologies involve implementing a novel approach to creating alignment markers. In typical systems, alignment markers are placed on scribe lines between the die of a semiconductor substrate. One common geometric shape of an alignment marker is a cross. However, such alignment markers with the scribe lines take up too much space on the semiconductor substrate. Instead, the example embodiments use portions or subsets of patterns on one or more die as alignment markers. In another example embodiment, patterns are extracted from the substrate itself, and not from dies placed on the substrate. That is, the patterns can be extracted from previous layers of materials placed on the substrate before placing the dies.

[0023] The fabrication of microelectronic devices typically involves a complicated process sequence requiring hundreds of individual processes performed on semi-conductive, dielectric, and conductive substrates. Examples of these processes include oxidation, diffusion, ion implantation, thin film deposition, cleaning, etching, and lithography, among other operations. Each operation is time consuming and expensive.

[0024] With ever-decreasing critical dimensions for microelectronic devices, the design and fabrication for these devices on substrates is becoming or has become increasingly complex. Control of the critical dimensions and process uniformity becomes increasingly more significant. Complex multilayer stacks used to make microelectronic devices involve precise process monitoring of the critical dimensions for the thickness, roughness, stress, density, and potential defects. Process recipes for forming the devices have multiple incremental processes to ensure critical dimensions are maintained. Typically, each incremental process may utilize one or more processing chambers that adds additional time for forming the devices and also increases opportunities for forming defects. As critical dimensions on these devices shrink, past fabrication techniques encounter new hurdles. One fabrication technique involves using alignment markers.

[0025] In semiconductor manufacturing, an alignment marker is a feature used for precisely aligning different layers of materials or structures during the fabrication process. These markers serve as reference points for aligning photolithography masks, which are used to pattern the semiconductor substrate. Alignment markers are specially designed gratings that are created on the semiconductor substrate alongside each layer's pattern. The alignment markers are made up of lines with vertical sides that are perpendicular to the substrate's surface.

[0026] Alignment markers are typically small patterns or structures that are designed to be easily recognizable under a microscope or through automated alignment systems. Common types of alignment markers include crosses, squares, or other geometric shapes.

[0027] During the semiconductor fabrication process, multiple layers of materials are deposited or patterned onto a silicon substrate to create integrated circuits (ICs). Each layer must be aligned accurately with the previously patterned layers to ensure proper functionality of the final device. Alignment markers play a crucial role in achieving this alignment by providing a reference point for aligning the photolithography masks used in patterning each layer.

[0028] Advanced semiconductor manufacturing processes may use various techniques to enhance alignment accuracy, such as overlay metrology systems that precisely measure the alignment of multiple layers based on the alignment markers' positions. Overall, alignment markers are essential for achieving the high precision required in semiconductor fabrication to ensure the reliability and performance of ICs.

[0029] Alignment markers in semiconductor manufacturing play an important role in ensuring precise alignment of different layers during the fabrication process. However, several issues can arise with alignment markers, which can impact the quality and yield of semiconductor devices. Some of these issues include:

[0030] The feature size and density variation of alignment markers. Alignment markers are typically fabricated using lithography techniques similar to those used for patterning the semiconductor devices themselves. Variations in feature size and density across the substrate can affect the accuracy of alignment, leading to misalignment issues.

[0031] Overlay errors associated with alignment markers. Overlay errors refer to the discrepancy between the intended alignment of different layers and the actual alignment achieved during fabrication. Various factors, such as equipment imperfections, thermal expansion, and mechanical stress, can contribute to overlay errors, leading to misalignment between layers.

[0032] Pattern recognition and detection errors associated with alignment markers. Automated alignment systems rely on pattern recognition algorithms to detect alignment markers accurately. However, issues such as pattern distortion, contamination, or low contrast can hinder the detection process, leading to alignment errors.

[0033] Process induced distortion issues with alignment markers. Semiconductor manufacturing processes, such as deposition, etching, and annealing, can induce stress and distortion in the substrate. This can result in the misalignment of alignment markers between different layers, affecting device performance and yield.

[0034] Mask alignment accuracy issues also arise. Alignment markers on photolithography masks must be accurately positioned to ensure proper alignment during the patterning process. Any inaccuracies in mask alignment can propagate as misalignment issues in the fabricated devices.

[0035] Alignment across large areas can also be challenging. In advanced semiconductor processes, where larger substrates or multiple dies are fabricated simultaneously, achieving consistent alignment across large areas can be challenging. Variations in alignment markers' positions across the substrate or die can lead to yield loss and decreased device performance.

[0036] Process integration challenges can also arise from using alignment markers. Semiconductor fabrication involves multiple process steps, each of which can impact alignment accuracy. Coordinating these processes to ensure consistent alignment throughout fabrication poses integration challenges that can affect overall yield and device performance.

[0037] Therefore, designs of alignment markers typically have strict definition in shape and dimension. Alignment markers can also take up significant space on a substrate. Also, alignment markers are not typically compatible from one company or customer to another.

[0038] Addressing these alignment issues requires continuous improvement in fabrication processes, equipment precision, and alignment techniques. Advanced metrology tools, process optimization strategies, and tighter control over fabrication parameters are essential for mitigating alignment-related issues and improving semiconductor manufacturing yield and device performance.

[0039] In the example embodiments, alignment markers need not be placed or etched onto scribe lines of semiconductor substrates. Instead, in one example, the

alignment markers are derived from patterns on die formed on the semiconductor substrate. Snapshots of patterns are taken from a die on the substrate. Patterns are extracted from the snapshots and combined to form a single alignment marker. The snapshots may be taken from the four corners of a die. In other examples, the snapshots may be taken from other areas of the die. The combination of extracted patterns forms a reference alignment marker that can be compared to other patterns in various alignment processes. In another example, the alignment markers are derived from patterns on the substrate itself. In particular, the patterns are extracted from previous layers of materials placed on the substrate. Snapshots are taken from the substrate. Patterns are extracted from the previous material layers placed on the substrate. The patterns are combined to a form a single alignment marker. The snapshots may be taken from any portion of the substrate.

[0040] This alignment marker creation strategy allows for manufacturers to pack more die on a single substrate. Packing more die on a substrate increases manufacturing efficiency and reduces production costs per chip. Higher die density on a substrate can thus be achieved and scribe line width can be significantly reduced. Optimizing scribe line width allows for closer placement of die, thus increasing the number of die that can be placed on a single semiconductor substrate.

[0041] Figure 1A illustrates taking snapshots of portions on a die to extract patterns, according to one or more of the embodiments described herein.

[0042] In the schematic 100, a die 110 of a plurality of dies includes a plurality of patterns. The patterns on the die 110 of the substrate include transistor structures, such as gates, sources, drains, and channels, which form the basic components of metal oxide semiconductor field effect transistors (MOSFETs) or other types of transistors. Other patterns include interconnects, which are metal lines or wires used to connect various components within an integrated circuit (IC). These patterns include metal layers deposited on the substrate surface, with vias used to connect different layers. Patterns on the substrate can also include structures for creating capacitors and resistors. Patterns on the substrate can include PN junctions, which form the basis for diodes and other semiconductor devices. Patterns on the substrate can also represent individual memory cells, which store data as electrical charge.

Moreover, logic gates and circuits can be formed by arranging transistors and interconnects on the substrate according to specific design layouts. The patterns can be created by using photolithography, etching, deposition, and other semiconductor manufacturing processes. The design and arrangement of these patterns are critical for the functionality, performance, and reliability of semiconductor devices.

[0043] In conventional systems, alignment markers are used to ensure accurate alignment of different layers during the fabrication process. These alignment markers are formed directly on the substrate including the plurality of dies. These alignment markers are placed on scribe lines formed between the dies of the substrate.

[0044] In contrast, the example embodiments do not create alignment markers on the scribe lines of the semiconductor substrate. Instead, the alignment markers are created from existing patterns formed on the die of the semiconductor substrate. The patterns are created by a customer.

[0045] A camera 160 can take snapshots of portions of the die 110. The die 110 can be any random die found on the semiconductor substrate. The camera 160 can take snapshots or images from the four corners of the die 110. For example, a first image 120 is taken from the top left corner, a second image 130 is taken from the top right corner, a third image 140 is taken from the bottom left corner, and a fourth image 150 is taken from the bottom right corner. Thus, in one instance, images from the four corners of a die on a semiconductor substrate are selected to form an alignment marker.

[0046] The first image 120 is expanded to illustrate the patterns 122 formed thereon. A user can select a portion 124 of the first image 120 to use as an alignment marker section 125. The second image 130 is expanded to illustrate the patterns 132 formed thereon. A user can select a portion 134 of the second image 130 to use as an alignment marker section 135. The third image 140 is expanded to illustrate the patterns 142 formed thereon. A user can select a portion 144 of the third image 140 to use as an alignment marker section 145. Similarly, an alignment marker section (not shown) can also be selected from the fourth image 150.

[0047] The portion 124 includes a unique or distinct segment or fragment or piece of the pattern 122 formed on the die 110. The portion 124 is a subset of entire pattern 122. The pattern 122 is part of a customer's feature design. The pattern 122 is unique to the customer. The features present on the portion 124 are different than other features in other areas of the die 110. As such, the portion 124 can be used as the alignment marker section 125 because of its uniqueness compared to other patterns found on the die 110.

[0048] Similarly, the portion 134 includes a unique or distinct segment or fragment or piece of the pattern 132 formed on the die 110. The portion 134 is a subset of entire pattern 132. The pattern 132 is part of a customer's feature design. The pattern 132 is unique to the customer. The features present on the portion 134 are different than other features in other areas of the die 110. As such, the portion 134 can be used as the alignment marker section 135 because of its uniqueness compared to other patterns found on the die 110.

[0049] Similarly, the portion 144 includes a unique or distinct segment or fragment or piece of the pattern 142 formed on the die 110. The portion 144 is a subset of entire pattern 142. The pattern 142 is part of a customer's feature design. The pattern 142 is unique to the customer. The features present on the portion 144 are different than other features in other areas of the die 110. As such, the portion 144 can be used as the alignment marker section 145 because of its uniqueness compared to other patterns found on the die 110.

[0050] Similarly, a unique alignment marker section can also be obtained from the fourth image 150 (and designated as 155 in Figure 1C).

[0051] The alignment marker sections can be selectively obtained from the respective images captured by the camera 160. For example, the user may select the leftmost area of the first image 120 to represent the alignment marker section and the user may select the rightmost area of the second image 130 to represent the alignment marker section. Thus, the user can select portions of the patterns within each captured image as representative of alignment marker sections. Once the alignment marker

sections are selected, they are combined to form a single alignment marker, as discussed below with reference to Figure 1B.

[0052] Figure 1B illustrates forming an alignment marker by combining portions of the patterns from the snapshots of the portions of the die, according to one or more of the embodiments described herein.

[0053] The alignment marker 170 is formed by combining the alignment marker section 125 found in the first image 120, the alignment marker section 135 found in the second image 130, the alignment marker section 145 found in the third image 140, and another alignment marker section 155 (Figure 1C) found in the fourth image 150. Therefore, four alignment marker sections from the four corners of the die 110 are used to form the alignment marker 170. The alignment marker 170 can be referred to as a template marker or a reference alignment marker.

[0054] In other example embodiments, the images may be captured from side regions of the die 110. In other words, the images need not only be captured from the four corners of the die 110, but can be selected from any side areas or regions of the die 110.

[0055] In other example embodiments, the images may be captured from both corners of the die 110 and side regions of the die 110. The alignment marker 170 may be formed from more than 4 images. The alignment marker 170 may be formed from 5 images, 7 images, 10 images, 20 images, etc. The user may be able to select any number of images from the die 110 to form the alignment marker 170.

[0056] In other example embodiments, the images may be captured from a plurality of different central and non-central regions of the die 110. For example, images may be captured from two corners of the die 110 and several central regions of the die 110 to form the alignment marker 170. The user may be able to select any number of images from the die 110 to form the alignment marker 170.

[0057] In certain embodiments, the camera 160 may scan the die 110 to detect unique patterns suitable for forming the alignment marker 170. The camera 160 may store the unique patterns in a storage device, such as a memory device (Figure 6).

The storage device may be local to the camera 160 or may be associated with an external computing device.

[0058] Therefore, even though the alignment marker 170 is constructed from patterns derived or extracted from images of the four corners of the die 110, it is contemplated that the alignment marker 170 may be constructed from any number of images captured from any areas or regions of the die 110.

[0059] Figures 1C-1E illustrate different shapes and sizes of the alignment marker.

[0060] Once the alignment marker sections are selected, they are combined in a number of different ways to construct the alignment marker 170.

[0061] In one example, in Figure 1C, the alignment marker section 125, the alignment marker section 135, the alignment marker section 145, and the alignment marker section 155 are combined in a tile format, such as a 2x2 tile, to form the single alignment marker.

[0062] In another example, in Figure 1D, if more than four alignment marker sections are selected, then a larger tile configuration may be constructed. For example, 12 patterns may be selected from 12 images captured by the camera 160. The 12 patterns may be combined as a 4x3 tile designated as alignment marker 180A. The alignment marker 180A may include a plurality of tiles 182, where each tile includes a different or unique pattern. Thus, 12 different patterns extracted from the die 110 form the alignment marker 180A, and assembled as a rectangle.

[0063] In another example, in Figure 1E, if more than four alignment marker sections are selected, then a larger tile configuration may be constructed. For example, 9 patterns may be selected from 9 images captured by the camera 160. The 9 patterns may be combined as a cross designated as alignment marker 180B. The alignment marker 180B may include a plurality of tiles 184, where each tile includes a different or unique pattern. Thus, 9 different patterns extracted from the die 110 form the alignment marker 180B, and assembled as a cross.

[0064] Therefore, alignment markers can be constructed in any shape or size. The shape or size may be selected by the customer. In other embodiments, the shape or size may be selected by the user to meet certain customer design requirements. The shape or size may also be selected by machine learning techniques.

[0065] Figure 2 illustrates a circular substrate with a plurality of die formed thereon, where patterns from at least one die are used to form an alignment marker, according to one or more of the embodiments described herein.

[0066] A substrate 200 includes a plurality of die 210. An alignment marker can be extracted from one of the die 210. In one example, a camera takes a snapshot of the four corners of one of the die 210. A first image 212 at a first corner of the die 210 is taken, a second image 214 at a second corner of the die 210 is taken, a third image 216 at a third corner of the die 210 is taken, and a fourth image 218 at a fourth corner of the die 210 is taken. A first pattern is extracted from the first image 212, a second pattern is extracted from the second image 214, a third pattern is extracted from the third image 216, and a fourth pattern is extracted from the fourth image 218. The first pattern is a portion or subset of the entire pattern captured in the first image 212. The second pattern is a portion or subset of the entire pattern captured in the second image 214. The third pattern is a portion or subset of the entire pattern captured in the third image 216. The fourth pattern is a portion or subset of the entire pattern captured in the fourth image 218.

[0067] The first, second, and third patterns are combined to form a single alignment marker or reference marker. The patterns from the portion of each captured image are compared to other patterns on the die 210 to determine uniqueness of the patterns. The patterns are circuit designs. The single alignment marker may facilitate precise alignment of lithographic masks.

[0068] Figure 3 illustrates a rectangular panel with a plurality of die formed thereon, where patterns from at least one die are used to form an alignment marker, according to one or more of the embodiments described herein.

[0069] A rectangular panel 300 includes a plurality of die 310. An alignment marker can be extracted from one of the die 310. In one example, a camera takes a snapshot

of the four corners of one of the die 310. A first image 312 at a first corner of the die 310 is taken, a second image 314 at a second corner of the die 310 is taken, a third image 316 at a third corner of the die 310 is taken, and a fourth image 318 at a fourth corner of the die 310 is taken. A first pattern is extracted from the first image 312, a second pattern is extracted from the second image 314, a third pattern is extracted from the third image 316, and a fourth pattern is extracted from the fourth image 318. The first pattern is a portion or subset of the entire pattern captured in the first image 312. The second pattern is a portion or subset of the entire pattern captured in the second image 314. The third pattern is a portion or subset of the entire pattern captured in the third image 316. The fourth pattern is a portion or subset of the entire pattern captured in the fourth image 318.

[0070] The first, second, and third patterns are combined to form a single alignment marker or reference marker. The patterns from the portion of each captured image are compared to other patterns on the die 310 to determine uniqueness of the patterns. The patterns are circuit designs. The single alignment marker may facilitate precise alignment of lithographic masks.

[0071] The rectangular panel 300 depicts scribe lines 320 separating the die 310. In conventional configurations, alignment markers are placed on the scribe lines 320. The scribe lines 320 run horizontally and vertically along the surface of the semiconductor substrate. The width of the scribe lines 320 can vary depending on the specific manufacturing process and the requirements of the semiconductor manufacturer. However, the scribe lines 320 can typically range from a few tens to a few hundreds of micrometers (um) in width. The width of the scribe lines is carefully controlled to accommodate conventional alignment markers.

[0072] However, in accordance with the example embodiments, the width of the scribe lines can be significantly reduced, as such scribe lines do not need to accommodate conventional alignment markers. Instead, an alignment marker can be created from portions or subsets of the patterns formed on the die. The alignment marker created from the portions or subsets of the patterns on the die need not be placed or etched on the scribe lines. Instead, the alignment marker created from the

patterns on the die can be stored in a memory device and retrieved when lithographic mask alignment positioning is performed.

[0073] As such, process complexity can be reduced by not providing alignment markers directly on the scribe lines of a semiconductor substrate. Developing and implementing scribe line patterns for each customer requires careful consideration of the manufacturing process. Complexity in scribe line design and execution can increase manufacturing costs and cycle times. In accordance with the example embodiments, by removing the alignment markers from the scribe lines of the semiconductor substrate, manufacturing costs and cycle times can be significantly reduced. Additionally, scribe lines can weaken the structural integrity of the semiconductor substrate, making it more susceptible to breakage during handling or processing. In accordance with the example embodiments, by removing the alignment markers from the scribe lines of the semiconductor substrate, the scribe lines can be thinner, and thus the structural integrity of the substrate itself can be strengthened.

[0074] Therefore, the width of the scribe lines can be significantly reduced and the width of the scribe lines may be designed for substrate dicing and chip separation purposes only, thus minimizing any negative impact they may have on semiconductor manufacturing processes and device performance.

[0075] Figure 4 is a flowchart for implementing a method to create an alignment marker from portions of patterns extracted from one or more die, according to one or more of the embodiments described herein.

[0076] At block 410, snapshots or images are taken of the four corners of a die formed on a semiconductor substrate. The snapshots are taken with a camera. The snapshots are provided to a user. The snapshots or images may be stored in a memory device (Figure 6).

[0077] At block 420, a pattern is extracted from each of the four snapshots. Thus, a first pattern is extracted from the first snapshot of the first corner, a second pattern is extracted from the second snapshot of the second corner, a third pattern is extracted from the third snapshot of the third corner, and a fourth pattern is extracted from the fourth snapshot of the fourth corner.

[0078] At block 430, it is determined whether the four extracted patterns are unique.

[0079] If NO, the process proceeds to block 432.

[0080] In block 432, other patterns are extracted from the snapshots that include unique features.

[0081] If YES, the process proceeds to block 440.

[0082] In block 440, the four patterns are combined to form a single alignment marker. The four patterns may be combined in a tile format to form a 2x2 tile. The first, second, third, and fourth patterns are different from each other. Each of the first, second, third, and fourth patterns includes different or unique features or circuit designs.

[0083] In block 450, the single alignment marker is used as a reference alignment marker for comparison with other patterns during alignment steps in, e.g., a lithography process.

[0084] Figure 5 is a flowchart for implementing a method to create an alignment marker from extracted patterns, according to one or more of the embodiments described herein.

[0085] In block 510, images of features on a die formed on a semiconductor substrate are captured.

[0086] In block 520, subsets of patterns are extracted from a portion of each captured image.

[0087] In block 530, the patterns are combined to form an alignment marker. The patterns can be combined in a number of different configurations.

[0088] Figure 6 is an alignment marker generator for generating a single alignment marker from multiple patterns of a die formed on a semiconductor substrate, according to one or more of the embodiments described herein.

[0089] The alignment marker generator 600 includes a camera 610 to capture images of features on a die 612 of a plurality of dies formed on a semiconductor substrate 614, a pattern extractor 620 to extract patterns 622 from a portion of each captured image, and a pattern assembler 630 to combine the extracted patterns to form an alignment marker 640. The alignment marker 640 can be stored in a storage device, such as a memory device 650. The alignment marker 640 can be retrieved from the memory device 650. The memory device 650 may store the final alignment markers for each customer. The memory device 650 may also store the patterns extracted from the die of each customer. For example, customer A, may have 100 extracted patters, customer B may have 500 extracted patterns, and customer C may have 1000 extracted patterns. A mechanism may also be provided to determine whether any newly extracted patterns have substantial similarity to previously extorted and stored patterns associated with a customer.

[0090] Figure 7A illustrates a substrate including a plurality of patterns from previous layers of materials and taking snapshots of portions of the patterns on the substrate, according to one or more embodiments described herein.

[0091] In another embodiment, the alignment marker can be generated from patterns from previous layers on the substrate of semiconductor substrate. For example, the semiconductor substrate or substrate 705 includes a plurality of patterns 710. The plurality of patterns 710 are not formed on any die. Instead, the plurality of patterns 710 are formed on the substrate 705 from previous layers before placing any dies on the substrate 705. In one example, the camera 160 (Figure 1) can take snapshots of portions of the plurality of patterns 710. A user can select, e.g., a first pattern portion 715 and a second pattern portion 717. The first pattern portion 715 and the second pattern portion 717 each include unique designs.

[0092] In one embodiment, the patterns extracted from the semiconductor substrate or substrate 705 are compared to other patterns on the semiconductor substrate or substrate 705 to determine uniqueness of the patterns.

[0093] Figure 7B illustrates forming an alignment marker by combining portions of the patterns from the snapshots taken of the portions of the substrate, according to one or more embodiments described herein.

[0094] The first pattern portion 715 and the second pattern portion 717 are combined to form an alignment marker 720. The first pattern portion 715 and the second pattern portion 717 can be selected from any portions or sections of the substrate 705. The selection of 2 pattern portions is merely an example. A user can select any number of pattern portions from the substrate 705 to form the alignment marker 720. In one example, 5, 7, 10, 12 or more pattern portions can be selected from the substrate 705 to form the alignment marker 720. The pattern portions can be combined in any number of configurations to form the alignment marker 720.

[0095] Figure 7C illustrates a shape of the alignment marker after combining patterns from the substrate, according to one or more embodiments described herein.

[0096] In one example, the alignment marker 720 can form a rectangular shape 722. Thus, the first pattern portion 715 and the second pattern portion 717 can be combined to form the rectangular shape 722. In other example embodiments, where more than 2 pattern portions are selected, the final shape of the alignment marker 720 may be a square or a cross or any other shape contemplated by one skilled in the art.

[0097] Therefore, alignment markers can be constructed in any shape or size. The shape or size may be selected by the customer. In other embodiments, the shape or size may be selected by the user to meet certain customer design requirements. The shape or size may also be selected by machine learning techniques.

[0098] Figure 8 illustrates an alignment marker generator for generating a single alignment marker from multiple patterns on a semiconductor substrate, according to one or more of the embodiments described herein.

[0099] The alignment marker generator 800 includes a camera 610 to capture patterns formed on the semiconductor substrate or substrate 705, a pattern extractor 620 to extract the first pattern portion 715 and the second pattern portion 717 from a portion of each captured image, and a pattern assembler 630 to combine the extracted

patterns to form the alignment marker 720. The alignment marker 720 can be stored in a storage device, such as a memory device 650. The alignment marker 720 can be retrieved from the memory device 650. The memory device 650 may store the final alignment markers for each customer. The memory device 650 may also store the patterns extracted from substrate 705.

[00100] Figure 9 illustrates a flowchart for implementing a method to create an alignment marker from portions of patterns extracted from the semiconductor substrate, according to one or more of the embodiments described herein.

[00101] In block 910, images of patterns on a semiconductor substrate of substrate are captured by a camera.

[00102] In block 920, target patterns are extracted from multiple portions of the semiconductor substrate or substrate.

[00103] In block 930, the target patterns are combined to form an alignment marker directly from patterns extracted from previous layers positioned on the semiconductor substrate or substrate.

[00104] In an alternative embodiment, a machine learning model may be trained using annotated data to extract patterns from a die of a substrate or directly from the substrate. The machine learning model may be built using data collection, data annotation, data preprocessing, feature extraction, model selection, and model training. The data collection step may include gathering a dataset of videos or images of previous patterns used by a customer or found on the substrate. As such, the machine learning model may be trained to extract specific unique patterns from a die on substrate or directly from the substrate. The machine learning model may use previously extracted patterns from a same customer to determine unique patterns for subsequent applications of the same customer. As such, the machine learning model can, e.g., learn to discard any patterns on a die or patterns on the substrate that may have been previously used to construct an alignment marker for such customer.

[00105] In summary, lithography systems print patterns onto substrates. As many as 100 of these patterns are needed to make a microchip and they all have to align

with each other precisely for the chip to work. A lithography system's ability to line up one pattern with the previous one is measured by its overlay performance. To achieve that kind of overlay, a lithography system needs to know the position of a substrate to within fractions of a nanometer before it exposes. Alignment masks can be used for system calibration and for aligning patterns to previously fabricated layers. According to the example embodiments, alignment markers need not be etched onto scribe lines of substrates. Instead, in one example, the alignment markers are derived from patterns on die formed on the substrate. Snapshots of patterns are taken from a die on the substrate. Patterns are extracted from the snapshots and combined to form a single alignment mark. The snapshots may be taken from the four corners of a die. In other examples, the snapshots may be taken from other areas of the die. The combination of extracted patterns forms a reference alignment marker that can be compared to other patterns in various alignment steps. In another example, the alignment markers are derived from patterns on the substrate itself. In particular, the patterns are extracted from previous layers of materials placed on the substrate. Snapshots are taken from the substrate. Patterns are extracted from the previous material layers placed on the substrate. The patterns are combined to a form a single alignment marker. The snapshots may be taken from any portion of the substrate.

[00106] This alignment marker creation strategy allows for manufacturers to pack more die on a single substrate. Packing more die on a substrate is a key strategy for increasing manufacturing efficiency and reducing production costs per chip. Higher die density on a substrate can thus be achieved and scribe line width can be significantly reduced. Optimizing scribe line width allows for closer placement of die, thus increasing the number of die that can be placed on a single semiconductor substrate.

[00107] While this specification contains many specific implementation details, these should not be construed as limitations on the scope of what may be claimed, but rather as descriptions of features that may be specific to particular implementations. Certain features that are described in this specification in the context of separate implementations may also be implemented, in combination, in a single implementation. Conversely, various features that are described in the context of a

single implementation may also be implemented in multiple implementations, separately, or in any suitable sub-combination. Moreover, although previously described features may be described as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination may, in some cases, be excised from the combination, and the claimed combination may be directed to a sub-combination or variation of a sub-combination.

[00108] Particular implementations of the subject matter have been described. Other implementations, alterations, and permutations of the described implementations are within the scope of the following claims as will be apparent to those skilled in the art. While operations are depicted in the drawings or claims in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed (some operations may be considered optional) to achieve desirable results. In certain circumstances, multitasking or parallel processing (or a combination of multitasking and parallel processing) may be advantageous and performed as deemed appropriate. While the various steps in an embodiment method or process are presented and described sequentially, one of ordinary skill in the art will appreciate that some or all of the steps may be executed in different order, may be combined, or omitted, and some or all of the steps may be executed in parallel. The steps may be performed actively or passively. The method or process may be repeated or expanded to support multiple components or multiple users within a field environment. Accordingly, the scope should not be considered limited to the specific arrangement of steps shown in a flowchart or diagram.

[00109] Furthermore, any claimed implementation is considered to be applicable to at least a computer-implemented method; a non-transitory, computer-readable medium storing computer-readable instructions to perform the computer-implemented method; and a computer system including a computer memory interoperability coupled with a hardware processor configured to perform the computer-implemented method or the instructions stored on the non-transitory, computer-readable medium.

[00110] As used herein, “a CPU”“, controller”, “a processor”, “at least one processor”, or “one or more processors”, generally refers to a single processor

configured to perform one or multiple operations or multiple processors configured to collectively perform one or more operations. In the case of multiple processors, performance the one or more operations could be divided amongst different processors, though one processor may perform multiple operations, and multiple processors could collectively perform a single operation. Similarly, "a memory"", at least one memory", or "one or more memories", generally refers to a single memory configured to store data and/or instructions, multiple memories configured to collectively store data and/or instructions.

[00111] As used herein, "gas" and "fluid" may be used interchangeable with either term generally referring to elements, compounds, materials, etc., having the properties of a gas, a fluid, or both a gas and a fluid.

[00112] Unless defined otherwise, all technical and scientific terms used have the same meaning as commonly understood by one of ordinary skill in the art to which these systems, apparatuses, methods, processes and compositions belong.

[00113] In this disclosure, the terms "top", "bottom", "side", "above", "below", "up", "down", "upward", "downward," "horizontal," "vertical," and the like do not refer to absolute directions. Instead, these terms refer to directions relative to a nonspecific plane of reference. This non-specific plane of reference may be vertical, horizontal, or other angular orientation.

[00114] The singular forms "a", "an", and "the", include plural referents, unless the context clearly dictates otherwise. Within a claim, reference to an element in the singular is not intended to mean "one and only one" unless specifically so stated, but rather "one or more". Unless specifically stated otherwise, the term "some" refers to one or more.

[00115] Embodiments of the present disclosure may suitably "comprise", "consist", or "consist essentially of", the limiting features disclosed, and may be practiced in the absence of a limiting feature not disclosed. As used here and in the appended claims, the words "comprise", "has", and "include", and all grammatical variations thereof are each intended to have an open, non-limiting meaning that does not exclude additional elements or steps.

[00116] "Optional" and "optionally" means that the subsequently described material, event, or circumstance may or may not be present or occur. The description includes instances where the material, event, or circumstance occurs and instances where it does not occur.

[00117] "Coupled" and "coupling" means that the subsequently described material is connected to previously described material. The connection may be a direct, or indirect connection, and may, or may not, include intermediary components such as plumbing, wiring, fasteners, mechanical power transmission, electrical communication, wired and/or wireless transmission, etc., which may suitable to affect operation of the components.

[00118] As used, the term "determining" encompasses a wide variety of actions. For example, "determining" may include calculating, computing, processing, deriving, investigating, looking up, for example, looking up in a table, a database, or another data structure, and ascertaining. In addition, "determining" may include receiving, for example, receiving information, and accessing, for example, accessing data in a memory. In addition, "determining" may include resolving, selecting, choosing, and establishing.

[00119] When the word "approximately" or "about" are used, this term may mean that there may be a variance in value of up to ±10%, of up to 5%, of up to 2%, of up to 1%, of up to 0.5%, of up to 0.1%, or up to 0.01%.

[00120] Ranges may be expressed as from about one particular value to about another particular value, inclusive. When such a range is expressed, it is to be understood that another embodiment is from the one particular value to the other particular value, along with all particular values and combinations thereof within the range.

[00121] As used, terms such as "first" and "second" are arbitrarily assigned and are merely intended to differentiate between two or more components of a system, an apparatus, or a composition. It is to be understood that the words "first" and "second" serve no other purpose and are not part of the name or description of the component, nor do they necessarily define a relative location or position of the component.

Furthermore, it is to be understood that that the mere use of the term “first” and “second” does not require that there be any “third” component, although that possibility is envisioned under the scope of the various embodiments described.

[00122] Although only a few example embodiments have been described in detail, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the disclosed scope as described. Accordingly, all such modifications are intended to be included within the scope of this disclosure as defined in the following claims. In the claims, means-plus-function clauses are intended to cover the structures described as performing the recited function and not only structural equivalents, but also equivalent structures. It is the express intention of the applicant not to invoke 35 U.S.C. § 112(f), for any limitations of any of the claims, except for those in which the claim expressly uses the words ‘means for’ together with an associated function.

[00123] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method comprising:
capturing images of features on a die formed on a semiconductor substrate;
extracting patterns from a portion of each captured image; and
combining the patterns to form an alignment marker.

2. The method of claim 1, wherein the images are captured from four corners of the die.

3. The method of claim 1, wherein the images are captured from side regions of the die.

4. The method of claim 1, wherein the images are captured from a plurality of different central and non-central regions of the die.

5. The method of claim 1, wherein the patterns are combined in a tile format.

6. The method of claim 1, wherein the patterns are combined in a cross geometry.

7. The method of claim 1, wherein the patterns from the portion of each captured image are compared to other patterns on the die to determine uniqueness of the patterns.

8. The method of claim 1, wherein the patterns are circuit designs.

9. The method of claim 1, wherein the alignment marker facilitates precise alignment of lithographic masks.

10. The method of claim 1, wherein the alignment marker is stored in a memory device and retrieved when lithographic mask alignment positioning is performed.

11. A method comprising:

capturing images on a semiconductor substrate;

extracting, from the images captured, patterns from previous material layers placed on the semiconductor substrate; and

combining the patterns extracted from the previous material layers placed on the semiconductor substrate to form an alignment marker.

12. The method of claim 11, wherein the patterns are combined in a tile format.

13. The method of claim 11, wherein the patterns are combined in a cross geometry.

14. The method of claim 11, wherein the patterns extracted from the semiconductor substrate are compared to other patterns on the semiconductor substrate to determine uniqueness of the patterns.

15. An alignment marker generator comprising:

a camera to capture images of features on a die of a plurality of dies formed on a semiconductor substrate or directly from a semiconductor substrate;

a pattern extractor to extract patterns from a portion of each captured image; and

a pattern assembler to combine the extracted patterns to form an alignment marker.

16. The alignment marker generator of claim 15, wherein the patterns are combined in a tile format.

17. The alignment marker generator of claim 15, wherein the patterns are combined in a cross geometry.

18. The alignment marker generator of claim 15, wherein the patterns from the portion of each captured image are compared to other patterns on the die or the semiconductor substrate to determine uniqueness of the patterns.

19. The alignment marker generator of claim 15, wherein the alignment marker facilitates precise alignment of lithographic masks.

20. The alignment marker generator of claim 15, wherein the alignment marker is stored in a memory device and retrieved when lithographic mask alignment positioning is performed.