

PATENT SPECIFICATION

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- (21) Application No. 39595/73 (22) Filed 15 Aug. 1973
 (31) Convention Application No. 12 570/72 (32) Filed 24 Aug. 1972 in
 (33) Switzerland (CH)
 (44) Complete Specification published 10 Dec. 1975
 (51) INT. CL.³ H03K 21/36
 G04C 5/00
 (52) Index at acceptance
 G4D 6C1 6C2 6L 6Y 7X
 G3T A5B1 A5T A5X



(54) AN ELECTRONIC REFERENCE ISOCHRONOUS PERIOD GENERATOR AND APPLICATIONS

(71) We, DYNACORE S.A., a corporation organised under the laws of the confederation of Switzerland of Rue D'Argent, 9 2500 Bienne, Canton of Berne, Switzerland, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly in and by the following statement:—

10 The present invention relates to an electronic reference isochronous period generator for a time computation device intended for supplying an electrical output signal defining a succession of isochronous periods of time adjustable to a desired value of sufficient accuracy that at most a predetermined absolute adjustment error is tolerated.

15 According to the present invention there is provided an electronic reference isochronous period generator for a time computation device intended for supplying an electrical output signal defining a succession of isochronous periods of time adjustable to a desired value of sufficient accuracy that at most a predetermined absolute adjustment error is tolerated, comprising, a high-frequency source supplying a high frequency signal, the frequency of which lies within a predetermined frequency range, the lower limit thereof corresponding to a frequency having a period equal to said tolerated adjustment error, a dividing counter having a counting input connected to said high-frequency source and having outputs delivering counting position data, said dividing counter being adapted for establishing said succession of isochronous periods by recurrently counting a certain number of periods of said high frequency signal, each counting of said certain number corresponding to one said isochronous period, programming means adapted for controlling the operation of said dividing counter and provided with

[Price 33p]

adjustable means for determining an actual value of said certain number, said actual value of said certain number having to be dependent upon said desired value of said isochronous period and upon said actual frequency of said high frequency signal, means for receiving from an external source information defining a standard period of time, to which said desired value of said isochronous period is related, said standard period of time being intended for adjusting said isochronous period as a new function of the frequency of said high frequency signal within said frequency range, mode selection means connected to said means for receiving information and adapted, simultaneously with receiving of said information, for causing the generator to pass from a usual autonomous mode of operation to an adjustment mode of operation, wherein said programming means comprise, a memory register forming part of said adjustable means and comprising setting inputs, said actual value of said certain number being memorized in said memory register, gated connection means disposed between said outputs of said dividing counter and said setting inputs of said memory register, reset-to-zero means for said counter, responsive to said mode selection means and adapted for causing said dividing counter to be reset to zero at the very instant when a said standard period of time begins to be applied under readjustment working conditions, thereby allowing said dividing counter to re-start its counting from zero and then to count during the entirety of said standard period of time, means for enabling said mode selection means to block said gated connection means in the autonomous mode of operation and to open said gated connection means during at least a final portion of said standard period of time in the adjustment mode of operation, thereby causing

said setting inputs of said memory register to be connected to said outputs of said dividing counter for allowing said memory register to take a position corresponding to that of said dividing counter at the very instant when said standard period of time finishes, said memorized actual value of said certain number thereby being automatically redetermined for a correct adjustment of said isochronous period whatever may then be the actual frequency of the high frequency signal within said frequency range, inhabitable subjection means responsive to said mode selection means and effective in the autonomous mode of operation for compelling said dividing counter re-currently to count, into one counting cycle each time, a number of periods of high frequency applied to said counting input which is equal to said certain number having said memorized value and, in the adjustment mode of operation, for inhibiting any compelling action from said memory register upon said dividing counter, and output means connected at least indirectly to said dividing counter for delivering said electrical output signal as a signal exhibiting recurrent level changes originated in said dividing counter and occurring synchronously with each said counting cycle.

Specific embodiments of the invention will now be described with reference to the accompanying drawings in which:

35 Figure 1A is an overall block diagram of an embodiment of a reference, isochronous, period generator with adjustment capability;

40 Figure 1B is an overall block diagram of an alternative embodiment of a reference, isochronous period generator;

Figure 2 is a more detailed diagram of part of the generator of the embodiment of Figure 1A;

45 Figure 3 is a more detailed diagram of part of the generator of the embodiment of Figure 1B;

50 Figure 4 is a more detailed diagram of a shaping circuit for the adjustment input provided on both the Figure 1A embodiment and the Figure 1B embodiment.

As seen in Figure 1A, the generator comprises an oscillator 1, which is arranged to provide, in the independent mode, an output signal having a basic frequency of such value that a signal having a desired isochronous period appears at an output terminal SS. This period may be adjusted at any time, the generator then operating in an adjustment mode, its operating conditions in this mode being based on a standard time period applied to an adjustment input ER. In order to realize these two modes of operation, i.e., the autonomous mode and the adjustment

mode, this generator, besides oscillator 1, also comprises an input selection circuit 2 which is connected to the oscillator on one hand directly and on the other hand by the intermediary of a pre-divider 3. The input selection circuit is further connected to dividing counter 4. The generator further comprises programming logic 5 for the counter 4 and a shaping stage 12 for shaping wave forms received at adjustment input ER via sensing coil 15 from an external time source. The program logic 5 in turn comprises a multiple memory 6, a multiple gate 7 for controlling the inputs of memory 6, a multiple coincidence detector 8, an inhibitor 9 connected to the output of this detector, and lastly a differentiator 10 for the adjustment information followed by a shaping stage 11 which provides a reset to zero signal to the dividing counter 4.

The oscillator 1 generates an output signal having an output signal being within a predetermined frequency range, the range being such that the period corresponding to the frequency of oscillator 1 be appreciably shorter than the isochronous period desired at the SS output, because the period of the oscillator's output signal determines the maximum deviation in the isochronous period, which can be tolerated, even when the generator is in its adjustment mode.

The operation of this generator will be explained, assuming that an isochronous period of the order of a second or a fraction of a second with an adjustment accuracy of at least 10^{-6} is desired at output SS, so that a frequency of the order of 10 MHz will be assumed for oscillator 1. It will be further assumed that oscillator 1 is of a known type and includes an output shaping stage, hence providing a pulse train of square pulses. That is, it will jump successively and alternately from a logic level 0 to a logic level 1, and vice versa, at output s. Assuming the generator has already been adjusted, operation in the autonomous mode will be presently examined, this being the most common mode, with no standard time period data applied to input ER. The input selector 2 will transmit either the signal received at its input e_1 directly from the oscillator, or the signal received at its input e_2 from the oscillator by the intermediary of pre-divider 3. A logic signal applied to input c of selector 2 determines the choice between the two inputs e_1 and e_2 . As there is no adjustment input signal at input ER, the logic level at input c of selector 2 is 0 (the particulars in shaper 12 ensuring this condition will be described further below). Therefore, as indicated by the logic equation in the block showing the selector 2, input e_1 will be selected and the signal di-

rectly transmitted via this input from the oscillator will be emitted from output s of this selector 2, and from there will pass to input e of the programmable dividing counter 4.

The counter 4 shown in Figure 1A is a conventional unidirectional dividing counter comprising n stages of binary dividers allowing counting up to 2^n (hence a division for a maximum ratio of $1/2^n$). The output signal of the dividing counter 4, therefore, is in the form of a plurality of binary information elements (bits), each of which will appear on a particular conductor or upon a particular pair of conductors (complementary signals). This set of output data is symbolically localized in Figure 1 by the multiple binary output sbm . It will be observed from Figure 1 transmissions of single binary information elements are denoted by single lines whereas parallel transmissions of a plurality of binary information elements (in this instance n binary information elements) are denoted by double lines. The data leaving the sbm output of the dividing counter 4 is applied to multiple binary input ebm of the program logic 5 within which the data is applied on one hand to input em_i of the multiple coincidence detector 8 and on the other hand to input em of the multiple gate 7 which comprises in parallel n AND gates controlled by input c of the multiple gate circuit 7. When in the autonomous mode, (that is, input ER receives no information concerning standard time periods) multiple gate 7 is blocking, but it will be assumed that it was previously conducting in order to transmit a set of n binary information elements to multiple memory 6 where they are still stored. From its multiple output sm , this multiple memory 6 transmits binary multiple data (corresponding to the states of its memory flip-flops) to input em_2 of the multiple coincidence detector 8. The latter, which comprises n "exclusive OR" circuits, with the output connected to respective inputs of an inverted OR circuit having n inputs (or another circuit filling the same overall logic function), detects when the dividing counter 4 passes to a state precisely corresponding to that stored in multiple memory 6. At that instant, this coincidence detector 8 will apply an output s signal to input e_1 of inhibitor 9, the output s of which in turn feeds as signal to input e_3 of the reset-to-zero shaper 11 which comprises an OR gate. The output of reset-to-zero shaper 11 then will pass to logic level 1 which issues from the program logic 5 at its output srz to be applied to the input of the zero reset rz of dividing counter 4. The latter, therefore, is reset to zero after having effected a counting cycle of a number of bits deter-

mined by the multiple binary information stored in memory 6.

Dividing counter 4 continually starts the same cycle and, at the termination of the cycle, a pulse from the inhibitor 9 output will be emitted by the end-of-cycle output sfc of the program logic and will appear at the SS output of the generator. In order to avoid perturbations when there is resetting to zero on account of some stages of the dividing counter possibly returning to zero faster than others, and thus causing the signal at the output of coincidence detector 8 to disappear before all the stages are back to zero, inhibitor 9 will be very slightly time-delayed to an extent compatible with the period of oscillator 1. For a frequency of about 10 MHz, such a period is approximately 100 ns. As is the case for all the program logic 5 elements, the dividing counter 4 consists of integrated circuit components of the complementary MOS type, trigger times being kept to the order of a dozen ns., and the time-delay of the inhibitor 9 being about twice this trigger time.

As long as the generator will operate in the autonomous mode in this manner, the SS output will provide periodic pulses recurring at the end of each counting cycle of dividing counter 4. As long as the frequency of the oscillator will remain perfectly stable, the periods of the signals at output SS also will remain perfectly stable. If, for whatever reason, the frequency of oscillator 1 changes, or if the generator is to be set for the first time upon assembly, use is made of a standard time period generated by the external standard time source and magnetically transmitted to coil 15 which period will be thus applied at the input ER of the generator. By means of a pulse shaping circuit 12 for the adjustment input ER, a pulse of precise calibration and typically lasting one or two seconds arrives at input ec of the program logic. The particular design of stage 12 ensuring the pulse input will be described further below. This data at input ec (logic level 1) will be transmitted within logic 5 to input c of the multiple gate 7 and to input e_2 of inhibitor 9, and, outside the logic, and via its output sc , to input c of the input selector 2. This results in the following: first, the multiple gate 7 will be rendered conducting; second, transmission of an output pulse of inhibitor 9 will be blocked; and third, no longer will the input signal e_1 of selector 2 appear as an output signal at s , but rather it will be the input signal from e_2 which will appear at said output signal of selector 2, that is, it will be the oscillator output signal after it has passed through pre-divider 3. It will be seen below what the exact role of this pre-divider is, and presently it will be assumed that it provides at its output s a

signal having a frequency equal to one-tenth of the frequency of the output signal of oscillator 1 which is applied to its input *e*. Hence counting divider 4 will count at a rate which is ten times slower. Generally, if the division ratio of the pre-divider 3 is $1/a$, the oscillator output signal's frequency being f , a signal having a frequency of f/a will appear at the input *e* of the dividing counter 4. Further, multiple gate 7 presently being conducting, the binary memory stages of the multiple memory 6 will constantly follow the information provided at output *sbm* of dividing counter 4. The multiple coincidence detector 8, hence, would permanently provide an output signal, indicating there is coincidence, but this is without significance because of the inhibition taking place in inhibitor 9.

It will be observed, furthermore, that the input signal at *ec* arrives at the differentiating stage 10 which provides a short pulse when logic level 1 appears at control input *ec*. This short pulse transmitted from output s_1 to input e_1 of zero to reset shaper 11 causes reset to zero of the counter precisely at the moment when the standard time period begins. Thus, the counter will count at a rate one-tenth (or $1/a$) of the normal rate, starting with the zero position and during the entire standard time period. At the end of latter, input *ec* again goes back to logic level 0, multiple gate 7 becomes blocking, and multiple memory 6 remains in the state prior to the very end of the standard time period. At this time also, the differentiator 10 sends a second pulse (differentiation of the complement of *ec*) from its output s_2 to input e_2 of the zero-reset shaper 11 which in turn emits a new reset-to-zero pulse to dividing counter 4. Simultaneously too, the suppression of the 1 level at the input of selector 2 reestablishes the direct path between the oscillator and the counter 4, and the suppression of the 1 level at input e_3 of inhibitor 9 allows it again to transmit the pulse appearing at the output of the multiple coincidence detector 8. From that instant, the counting cycle in the autonomous mode of operation will be reproduced as previously described, but the binary combination recorded in memory 6 will exactly correspond to the number of bits that the counter 4 must count in order that the period at the output SS of the generator be equal to the standard time period divided by 10 (the division ratio of pre-divider 3; in the general case, the standard time period will be divided by a). If, for instance, the standard time period at input *ec* of the logic had been 1 sec., the synchronous period cyclically appearing at output SS of the generator would be exactly $1/10$ sec., but if on the other hand the standard time period had been 2 sec. at

input *ec* of logic 5, the synchronous period at output SS would be precisely 0.2 sec.

Shaping stage 12 of the adjustment input ER serves to supply a pulse of precisely determined length to input *ec* of logic 5. The data from input ER arriving at this stage 12 is shown in Figure 1A as being obtained by means of a coil 15 which is temporarily brought into magnetic coupling with an external standard source. Alternatively the data may be obtained electrically and directly or, especially if the generator is used to control the operation of a wrist-watch, by the intermediary of photoelectric receiver subject to outside information. The response characteristics of this receiver possibly differ between beginning and end of the pulse, which may be magnetic or optical. Preferably, the generation of an exact duration pulse will be performed by means of the measured time between two short successive pulses. The beginning and end of each pulse transmitted to input *ec* will be determined by the appearance (or possibly the disappearance) of this short pulse, so that the response conditions will be exactly the same at the beginning and end of the pulse of known length. Therefore, the input reset shaper 12 must obtain from input ER (to which the receiver is connected), two successive pulses or an even number of successive pulses. The diagram showing the block of stage 12 in Figure 1A shows how the pulse of predetermined length is obtained. Generally the external standard time period circuit sending the short pulses to the receiver, that is, in this case, to the coil 15, will be properly made in order always to transmit two pulses of a number of pairs of pulses. If somehow these short pulses were uneven in number, or if they succeeded one another at a rate always higher than the capacity of the dividing counter 4 and of memory 6, taking into account the pulse rate applied to the input of counter 4, the level of the input data at point *ec* still would be at 1 when the dividing counter and the memory arrive at their last position. It is clear that under these conditions, adjustment will be impossible; however, in order to bring the data at input *ec* back to the 0 level, when the memory 6 following counter 4 arrives at its last position, memory 6 will apply to output *sd* of programming logic 5 and therefrom to input *rz* of shaping stage 12 a datum causing reset-to-zero of the output of the shaping stage 12. To do so, use is made of the rising edge of the inverse output of the last flip-flop of the memory. It will be seen below in connection with Figure 4 how this process is effected.

In one ----- form of the generator of Figure 1A a discriminator 13 may be provided, as shown in dashed lines. The dis-

criminator 13 controls the pre-divider 3 by selecting a divisor from a predetermined group of divisors. The discriminator 13 can, itself be controlled by coded information 5 incorporated in the output signal from the external time source which does not affect the main input pulses. Each divisor corresponds to a particular isochronous period for the generator's output signal. One might 10 for instance require an isochronous period of either 1/5, or 1/6 or 1/10 of a second to set the generator period if the generator was used to control the oscillations of a sprung balance in a wristwatch. To that end 15 one may use a discriminator 13 transmitting logic data to one or possibly several of three outputs s_1 , s_2 , s_3 as a function of this coded information in order to set the pre-divider 3 in such manner that it will 20 effect a division, for instance by 5, 6 or 10, corresponding to the case previously discussed. Thus, depending on the coding being distinguished, the isochronous period at the SS output will be 1/5, 1/6 or 1/10 of a 25 second with any other value also being feasible if required.

Figure 1B shows another possible embodiment of the generator. This embodiment includes some elements of the embodiment of Figure 1 and these elements 30 are indicated by the same reference numerals. In this latter embodiment, the programmable dividing counter 4' is bi-directional that is it will count either forward or backward, depending on the logic level being 35 applied to a counting direction controlling input ar . In the programming logic 5' stage 8' no longer receives, both, the binary multiple data from counter and the multiple 40 binary data from memory 6, as does stage 8 in Figure 1A, but only the multiple binary data from counter 4'. Stage 8' in this instance does not operate as a coincidence detector but as a null detector, that is, it 45 senses the counter's arrival at the zero position. In this case multiple binary data supplied by memory 6, which is the same as in the first described embodiment, is applied to a multiple gate 14 which controls 50 the presetting of counter 4' and which will transmit or block this data as a function of the output level of inhibitor 9. In the Figure 1B embodiment output s of the inhibitor, which constitutes the output at SS, 55 is no longer connected to input e_2 of the zero to reset shaper 11, but it is connected to a control input c of multiple gate 14. When the output signal from memory 6 is transmitted from input em to output sm 60 of this multiple gate 14, it will be applied to a multiple preselection input prs of counter 4'. The direction of operation of the latter is such that when the generator is in the adjustment mode, it will count 65 forward as in the embodiment previously

discussed whereas when the generator is the autonomous mode it will count backward. At the moment when null-detector 8' has detected a null or zero position, it will send 70 a pulse to inhibitor 9 which will render gate 14 conducting, causing the multiple binary data contained in memory 6 to be fed to counter 4' and presetting all the stages of the latter to a position corresponding to the combination stored in memory 75 6. Then, dividing counter 4' counts backwards the number of desired bits until it reaches zero, at which time, as previously mentioned, it will again be reset to the pre-selected position. In order to obtain the 80 backward counting of counter 4, the input selector 2 applies to the counter's input ar a signal from output m of the selector 2 which signal is the complement of the signal applied to the selector's input c . Thus, 85 in the adjustment mode, the counter's input ar is at the logic level 0 and the counter counts forward, whereas in the autonomous mode, this ar input is at the logic level 1 and the counter counts backward. 90

The Figure 1B embodiment provides an adjustable cycle with the same accuracy as the Figure 1A embodiment, the former, however, providing the advantage of not 95 requiring a multiple coincidence circuit which is fairly difficult to achieve.

It will further be noted that resetting the counter to zero at the end of the adjustment cycle by means of the connection between the output s_2 of the differentiator 10 100 and the input e_2 of the zero to reset shaper 11 is not absolutely required. Indeed, in the Figure 1B embodiment, the counter already is in the desired position for starting the first cycle in the autonomous mode at the 105 end of the adjustment cycle. If it is reset to zero, this act will immediately cause null-detector 8' to operate, whereupon, after the pulse is supplied by the latter, there will be resetting of the counter to the state corresponding to the multiple information stored 110 in memory 6. In this instance one might therefore omit resetting to zero. Further, in the Figure 1B embodiment, the multiple memory 6 and the dividing counter 4 ought 115 to be in exactly the same position at the end of the first adjustment cycle, so that the multiple coincidence detector also ought to operate and, by itself, cause the counter to reset to zero as soon as inhibitor 9 activated by level 1 vanishing at its input e_1 . 120 One may, therefore, eliminate the connection between output s_2 differentiator 10 and input e_2 of zero reset shaper 11, this simplifying both circuits, but there would be 125 present the very slight risk of the memory being incapable of following the last step of the counter in the case of exact coincidence of the end of the input pulse at ec with a trigger of counter 4' from a pulse at 130

the latter's input, so that there would be failure to detect coincidence. In such a case the counter would carry out a first and longer cycle in order to return to zero following its latest possible position. Starting with the second cycle, however, the duration of the isochronous period again would be proper. There would merely be a shift as regards being "on time", but there would be no deviation with respect to the magnitude of the isochronous period.

Figure 1B shows the light transducer 15' arranged as a receiver for the standard period of time optically transmitted by the external standard time source, this light transducer 15' is arranged to supply adjustment pulse to the adjustment input ER in order to adjust the isochronous period. Alternatively a magnetic system as shown in Figure 1A may be used.

One will also observe that the accuracy of adjusting of the isochronous period by nature will be equal to the period of the oscillator 1. That is if, for instance, the frequency of this oscillator is 10 megacycles and an isochronous period of one second is desired, the adjusting accuracy would be 10^{-7} ; but it would be only 10^{-6} if the pre-divider were to operate at a ratio of 1/10 and an isochronous period of 1/10 of a second were established. The fact that in the adjustment mode the counter input will receive pulses at a lower rate on account of the action of pre-divider 3, whereby the maximum possible deviation of the resetting cycle is being increased, has no influence on the effective deviation as to the independent mode, because then the isochronous period will be reduced in the same ratio to the period being used as the standard during adjustment. The relative accuracy in effect is less, but the absolute one remains unchanged because there will be a relative accuracy a times large if the period is a times smaller.

The embodiment of Figure 1B may also include a discriminator circuit 13 connected in the same manner as shown in Figure 1A.

Figure 2 shows the major part of the embodiment of Figure 1A in greater detail. Only the oscillator, the pre-divider and the shaping edge for the adjustment input and the discriminator are omitted. Figure 2 makes use of known logic notation showing clearly how the different components are realized; therefore, the discussion will be restricted to differences or particularities with respect to Figure 1. Thus, multiple gate 7 and multiple memory 6 form a single functional block in the embodiment of Figure 2, the multiple memory making use of flip-flops comprising a direct selection input D which is controlled, that is, made to act or not, by an input V of the flip-flop. Gate 7 therefore is limited to a multiple connec-

tion of the inputs V of all the flip-flops of the memory 6, the multiple data from the dividing counter entering the flip-flops at their input D. It was assumed these flip-flops might be set in position by acting on their single input D; however, the dotted line shows the possibility of feeding the information in the form of two complementary levels, one applied to input D and the other to a possible input $\bar{D}$. The multiple coincidence detector 8 also was obtained in a special manner, the "exclusive OR" circuits indicating coincidence by a zero level having been replaced by a set of three NAND gates which in fact form an "exclusive OR" circuit. Therefore, the gate gathering the data of the individual coincidence tests is not an inverted OR (NOR) but a direct AND gate.

Similarly, the differentiating components of circuit 10 are shown as RC-sets, but it is obvious that other logic means such as is comprised in the technique of complementary MOS integrated circuits might be advantageously used as differentiation components. It will also be noted that in Fig. 2 the dot-dash line shows the boundary between that part constituting the program logic 5 and the other shown components of the generator.

Fig. 3 shows in more detailed manner and similarly to Fig. 2 the second embodiment shown schematically in block form in Fig. 1. The general considerations relating to Fig. 2 and stated above also apply to Fig. 3. The multiple gate 7 and memory 6 again are compacted into a single functional block, and the same applies for the null-detector 8 and inhibitor 9, these latter, however, are made compact merely for the sake of clarity in the drawing. Null-detection consists of a simple AND gate with n inputs, each of which is connected to the output $\bar{Q}$ of the flip-flops of the dividing counter.

In the embodiment of Fig. 3, multiple gate 14, either transmitting or blocking the multiple data from the memory to the multiple input of the preselection counter, is directly combined with the latter by the provision of flip-flops with direct selection inputs D controlled by an input gate V in the counter. The previously discussed considerations concerning the settings of the flip-flops of the memory in the first embodiment equally apply to this embodiment to both flip-flops for the memory and counter.

Fig. 3 further shows that all the flip-flops of counter 4 except the first are provided with an arrangement at their inputs for inverting the direction of the counting operation. It is known that to invert the direction of operation in a binary counter,

it suffices to provide all the pulse inputs C_p of all the flip-flops past the first one with a signal constituting the logic complement of the one applied to make the counter operate forward. In order to do so, one may apply to each flip-flop the output $\bar{Q}$ of the previous one rather than its output Q , but the sets of gates required for this interconnection are more complex (or require more input connections) than the set of gates shown in Fig. 3 and serving the same purpose. When there is a level 0 at input ar of the counter, the output signal Q of a flip-flop following is transmitted with its original phase, after double inversion, to the input C_p of the following flip-flop, whereas in the presence of a logic level 1 at the counter input ar , this signal is transmitted to the ensuing flip-flop with a phase inversion. Therefore, the programmable dividing counter operates forward when the logic lever 0 is present at input ar and backward when the logic level 1 is present at that input.

The dot-dashed line in Fig. 3 shows the location of the components indicated, these being either within program logic 5 or outside of it.

Fig. 4 shows in greater detail the diagram of the shaping stage for the adjustment input, this embodiment of Fig. 4 obviously being only one of the many possibilities for achieving this stage. It is seen that the signal from input ER (supplied for instance by a magnetic, capacitive or optical receiver) first enters a regenerative trigger such as a Schmitt trigger so that the pulses are square with well defined logic levels. Then the pulses are differentiated to avoid the value of the data being processed from remaining permanently at the logic level 1, as might be the case with an accidentally, permanently illuminated photoelectric receiver. These differentiated pulses then are applied to a flip-flop of which the output provides with great accuracy the standard time period applied to the input ec of the logic. In case there is no second input pulse, which means this flip-flop would stay in state 1, the data from output $\bar{Q}$ of the last flip-flop of memory 6 will be applied to an input rz of that stage. In case of normal adjustment, when the memory need never effect a complete cycle following the counter, this flip-flop will only pass from state 1 to state 0 when the counter is reset to zero at the beginning of the adjustment cycle, or at the end of this cycle when the output of the forming stage for adjustment already is back at the logic level 0.

In case the flip-flop in that stage was to remain in the logic state 1 a relatively long period because of lack of an input pulse, the trigger edge of this last memory flip-flop, which is transmitted by a differ-

entiator, will reset to zero the forming stage flip-flop by acting on its reset-to-zero input R. In order to avoid the drop on the last memory flip-flop at the very beginning of the adjustment cycle from resetting the forming stage flip-flop to zero, the above mentioned differentiated pulse is transmitted through an AND gate which, by means of a differentiating circuit and a slightly delayed inverter, will be blocking at the very beginning of the resetting cycle. Thus, even if an odd number of pulses were to arrive at input ER, the adjustment cycle will not be permanently locked in. Rather, the independent mode will be re-established, though with a non-adjusted output isochronous period that corresponds to the period of oscillator 1 multiplied by 2^n , where n is the number of binary stages of the counter. This latitude allows, when so desired, the application of only one pulse to input ER and the determination in this manner of the effective frequency of oscillator 1, which is not known with precision since it is without importance for the operation of the generator.

It will be noted that this generator may be designed in many ways, the described and shown embodiments only being illustrations, and that this generator may be advantageously applied to time-measuring instruments or to devices which for any reason must effect time measurements. This circuit would equally well apply to a wrist-watch of economical manufacture, the setting of which would be very simply effected by means of a coil i.e. coil 15 connected to input ER and subject to an external magnetic pulse generator, so that there would be no need to open the watch. It will be observed that the isochronous period supplied by output SS may be advantageously used to control or synchronize the oscillations of a tuning-fork or sprung-balance regulator or for activating a stepping motor driving time-indicating organs, this isochronous period also being applicable to another part of the electronic circuitry, preferably in integrated circuit form, providing indications relating to seconds, minutes, hours, even days or dates, or to a digital or analogue electronic display, or also to a device such as a computer print out, or a stamping machine, etc., these electronic circuits, activated by the synchronous period from output SS, being denoted in generalized fashion by the term "time-computation devices".

Lastly it should be noted that the time intervals, or isochronous periods, supplied by the SS output are given by very short pulses, a state of affairs which in some cases may entail drawbacks. In the case of a generator made to supply a well-defined isochronous period, as for a watch, a uni-

vibrator may be connected to this SS output, the univibrator being of a period about half that of the isochronous one. One may also, independently of the value of this
 5 isochronous period, connect a flip-flop to output SS, the flip-flop being in state 1 during one isochronous period of SS, then in state 0 during another isochronous period at SS, hence ultimately providing a
 10 complete isochronous period of double duration.

WHAT WE CLAIM IS:—

1. An electronic reference isochronous period generator for a time computation
 15 device intended for supplying an electrical output signal defining a succession of isochronous periods of time adjustable to a desired value of sufficient accuracy that at most a predetermined absolute adjustment
 20 error is tolerated, comprising, a high-frequency source supplying a high frequency signal, the frequency of which lies within a predetermined frequency range, the lower limit thereof corresponding to a
 25 frequency having a period equal to said tolerated adjustment error, a dividing counter having a counting input connected to said high-frequency source and having outputs delivering counting position data, said
 30 dividing counter being adapted for establishing said succession of isochronous periods by recurrently counting a certain number of periods of said high frequency signal, each counting of said certain number
 35 corresponding to one said isochronous period, programming means adapted for controlling the operation of said dividing counter and provided with adjustable means for determining an actual value of said certain
 40 number, said actual value of said certain number having to be dependent upon said desired value of said isochronous period and upon said actual frequency of said high frequency signal, means for receiving
 45 from an external source information defining a standard period of time, to which said desired value of said isochronous period is related, said standard period of time being intended for adjusting said isochronous period as a new function of the
 50 frequency of said high frequency signal within said frequency range, mode selection means connected to said means for receiving information and adapted, simultaneously with receiving of said information, for causing the generator to pass from a usual autonomous mode of operation to an adjustment mode of operation, wherein said programming means
 55 comprise, a memory register forming part of said adjustable means and comprising setting inputs, said actual value of said certain number being memorized in said memory register, gated connection means
 60 disposed between said outputs of said

dividing counter and said setting inputs of said memory register, reset-to-zero means for said counter, responsive to said mode
 selection means and adapted for causing
 70 said dividing counter to be reset to zero at the very instant when a said standard period of time begins to be applied under readjustment working conditions, thereby allowing said dividing counter to re-start
 75 its counting from zero and then to count during the entirety of said standard period of time, means for enabling said mode selection means to block said gated connection means in the autonomous mode of
 80 operation and to open said gated connection means during at least a final portion of said standard period of time in the adjustment mode of operation, thereby causing said setting inputs of said memory register to be connected to said outputs of
 85 said dividing counter for allowing said memory register to take a position corresponding to that of said dividing counter at the very instant when said standard period of time finishes, said memorized actual
 90 value of said certain number thereby being automatically redetermined for a correct adjustment of said isochronous period whatever may then be the actual frequency of the high frequency signal within said
 95 frequency range, inhibitable subjection means responsive to said mode selection means and effective in the autonomous mode of operation for compelling said dividing counter recurrently to count, into
 100 one counting cycle each time, a number of periods of high frequency applied to said counting input which is equal to said certain number having said memorized value and, in the adjustment mode of operation,
 105 for inhibiting any compelling action from said memory register upon said dividing counter, and output means connected at least indirectly to said dividing counter for delivering said electrical output signal as a
 110 signal exhibiting recurrent level changes originated in said dividing counter and occurring synchronously with each said counting cycle.

2. A generator as claimed in claim 1,
 115 wherein said dividing counter comprises a plurality of binary counter stages and operates on a binary base, said value of said certain number memorized in said memory register having the form of a combination
 120 of binary data elements.

3. A generator as claimed in claim 2, wherein said inhibitable subjection means causes the dividing counter to count said
 125 certain number of periods of said high frequency signal by means of coincidence detection means detecting a coincidence between the state of said binary dividing counter stages and said combination of
 130 memorized binary data elements, said coin-



vibrator may be connected to this SS output, the univibrator being of a period about half that of the isochronous one. One may also, independently of the value of this isochronous period, connect a flip-flop to output SS, the flip-flop being in state 1 during one isochronous period of SS, then in state 0 during another isochronous period at SS, hence ultimately providing a complete isochronous period of double duration.

WHAT WE CLAIM IS:—

1. An electronic reference isochronous period generator for a time computation device intended for supplying an electrical output signal defining a succession of isochronous periods of time adjustable to a desired value of sufficient accuracy that at most a predetermined absolute adjustment error is tolerated, comprising, a high-frequency source supplying a high frequency signal, the frequency of which lies within a predetermined frequency range, the lower limit thereof corresponding to a frequency having a period equal to said tolerated adjustment error, a dividing counter having a counting input connected to said high-frequency source and having outputs delivering counting position data, said dividing counter being adapted for establishing said succession of isochronous periods by recurrently counting a certain number of periods of said high frequency signal, each counting of said certain number corresponding to one said isochronous period, programming means adapted for controlling the operation of said dividing counter and provided with adjustable means for determining an actual value of said certain number, said actual value of said certain number having to be dependent upon said desired value of said isochronous period and upon said actual frequency of said high frequency signal, means for receiving from an external source information defining a standard period of time, to which said desired value of said isochronous period is related, said standard period of time being intended for adjusting said isochronous period as a new function of the frequency of said high frequency signal within said frequency range, mode selection means connected to said means for receiving information and adapted, simultaneously with receiving of said information, for causing the generator to pass from a usual autonomous mode of operation to an adjustment mode of operation, wherein said programming means comprise, a memory register forming part of said adjustable means and comprising setting inputs, said actual value of said certain number being memorized in said memory register, gated connection means disposed between said outputs of said

dividing counter and said setting inputs of said memory register, reset-to-zero means for said counter, responsive to said mode selection means and adapted for causing said dividing counter to be reset to zero at the very instant when a said standard period of time begins to be applied under readjustment working conditions, thereby allowing said dividing counter to re-start its counting from zero and then to count during the entirety of said standard period of time, means for enabling said mode selection means to block said gated connection means in the autonomous mode of operation and to open said gated connection means during at least a final portion of said standard period of time in the adjustment mode of operation, thereby causing said setting inputs of said memory register to be connected to said outputs of said dividing counter for allowing said memory register to take a position corresponding to that of said dividing counter at the very instant when said standard period of time finishes, said memorized actual value of said certain number thereby being automatically redetermined for a correct adjustment of said isochronous period whatever may then be the actual frequency of the high frequency signal within said frequency range, inhibitable subjection means responsive to said mode selection means and effective in the autonomous mode of operation for compelling said dividing counter recurrently to count, into one counting cycle each time, a number of periods of high frequency applied to said counting input which is equal to said certain number having said memorized value and, in the adjustment mode of operation, for inhibiting any compelling action from said memory register upon said dividing counter, and output means connected at least indirectly to said dividing counter for delivering said electrical output signal as a signal exhibiting recurrent level changes originated in said dividing counter and occurring synchronously with each said counting cycle.

2. A generator as claimed in claim 1, wherein said dividing counter comprises a plurality of binary counter stages and operates on a binary base, said value of said certain number memorized in said memory register having the form of a combination of binary data elements.

3. A generator as claimed in claim 2, wherein said inhibitable subjection means causes the dividing counter to count said certain number of periods of said high frequency signal by means of coincidence detection means detecting a coincidence between the state of said binary dividing counter stages and said combination of memorized binary data elements, said coin-



cidence detection means being arranged to reset said dividing counter to zero when a said coincidence is being sensed.

4. A generator as claimed in claim 1, wherein said dividing counter is further adapted to operate reversibly for operating in forward counting direction in the adjustment mode of operation and in reverse direction in the autonomous mode of, said inhibitable subsection means comprising means for detecting a zero position of said dividing counter and causing said dividing counter to count said certain number of periods of high frequency signal by pre-setting said dividing counter by means of pre-selection to a state corresponding to said certain number having said memorized value every time said means for detecting a zero position detect that said dividing counter, operating in the reverse counting direction, reaches its zero position.

5. A generator as claimed in any one of the preceding claims further comprising: an input frequency divider, pre-set to divide said high frequency signal from said high-frequency source in a predetermined ratio for providing a sub-multiple of it, and input selection means connected to said high-frequency source, to said input frequency divider, and to said counting input of said dividing counter for supplying said counting input with said high frequency signal from said source under said autonomous working conditions and with said sub-multiple thereof under said adjustment working conditions, thereby allowing said isochronous period to be adjusted to a value given by said standard period of time divided by said ratio of said input frequency divider.

6. A generator as claimed in claim 5, wherein said working-condition selection means comprise logic circuits for controlling said gated connection means, said reset-to-zero means, said inhibitable subsection means, and said input selection means.

7. A generator as claimed in any one of the preceding claims wherein said high-frequency source comprises a quartz oscillator in which a quartz oscillates at its natural frequency without impressed correction.

8. A generator as claimed in any one of the preceding claims, wherein said working-condition selection means comprise logic circuits for controlling said gated connection means, said reset-to-zero means and said inhibitable subsection means.

9. A generator as in any one of the preceding claims, wherein said means for receiving said information defining said standard period of time comprises a receiver responding to a suitable physical datum externally provided, without requiring electrical contact.

10. A generator as claimed in claim 9, wherein the receiver comprises at least one magnetic coupling coil.

11. A generator as claimed in claim 9, wherein the receiver comprises at least one photoelectric transducer.

12. A generator as claimed in any one of the preceding claims for a time computation device consisting of a wrist-watch, wherein at least said dividing counter and said programming means are in the form of integrated circuitry.

13. An electronic reference isochronous period generator substantially as hereinbefore described with reference to and as illustrated in Figure 1A of the accompanying drawings or Figure 1A as modified by Figure 2 and/or Figure 4.

14. An electronic reference isochronous generator substantially as hereinbefore described with reference to Figure 1B of the accompanying drawings or Figure 1B as modified by Figure 3 and/or Figure 4.

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