ABSTRACT

A METHOD TO FORM SELF-ALIGNED SILICIDE WITH REDUCED SHEET RESISTANCE

A new method of forming MOS transistors with self-aligned silicide has been achieved. A gate oxide layer is formed overlying a semiconductor substrate. A polysilicon layer is deposited. The polysilicon layer and the gate oxide layer are patterned to form gates. Ions are implanted to form lightly doped drain regions. A dielectric layer is deposited. The dielectric layer is polished down to expose the top surface of the gates. The dielectric layer is then anisotropically etched down to form dielectric sidewall spacers. The dielectric sidewall spacers cover a portion of the vertical sidewalls of the gates while exposing a portion of the vertical sidewalls of the gates. Ions are implanted to form source and drain regions. A metal layer is deposited. Contact surfaces are formed between the metal layer with: the exposed top surfaces of the gates, the exposed portions of the vertical sidewalls of the gates, and the exposed source and drain regions. The integrated circuit device is annealed to react the metal layer and the polysilicon layer and silicon to selectively form a silicide layer in the surface of the polysilicon layer and in the surface of the semiconductor substrate at the contact surfaces. The remaining metal layer is removed to complete the device.

FIGURE 3 IS SUGGESTED FOR PUBLICATION