ABSTRACT

A non-volatile memory device includes a first semiconductor layer and a second semiconductor layer. The first semiconductor layer includes memory cells electrically connected to bit lines each extending in a first direction and word lines each extending in a second direction and stacked in a vertical direction, word line pads which respectively correspond to the word lines and are arranged in a stair shape, and word line contacts respectively electrically connected to the word line pads. The second semiconductor layer includes pass transistors respectively electrically connected to the word line contacts to respectively overlap the word line pads in the vertical direction. Each of the word line pads has a first width in the first direction and a second width in the second direction. Each of the pass transistors has a first pitch in the first direction and a second pitch in the second direction.

FIG. 6