What is claimed is:

1. A method of forming a field effect transistor, comprising:

forming trench isolation material on opposing sides of a semiconductor material channel region along a length of the channel region, the trench isolation material being formed to comprise upper sidewalls and opposing insulative projections below the upper sidewalls that extend laterally relative to the upper sidewalls toward one another, the insulative projections being received partially elevationally under the channel region along the channel length and with semiconductor material being received elevationally over the projections;

exposing opposing sides of the semiconductor material along the channel length by removing some of the trench isolation material;

removing some of the semiconductor material from the exposed opposing sides along the channel length to form a channel fin projecting upwardly relative to the projections; and

forming a gate over a top and opposing sides of the fin along the channel length.

2. The method of claim 1 wherein forming the trench isolation material comprises forming insulative projection inner surfaces extending along the length of the channel which are convexly curved relative to fin thickness transverse the channel length.

3. The method of claim 1 wherein the semiconductor material along the channel length has a top, the top being masked during the removing of semiconductor material from the exposed opposing sides to form the channel fin.

4. The method of claim 1 wherein the removing of the trench isolation material does not remove any insulative material within the projections.

5. The method of claim 1 wherein the etching of the trench isolation material is into insulative material which is laterally adjacent insulative material of the opposing insulative projections.

6. The method of claim 5 wherein the removing of the trench isolation material is into insulative material within the opposing insulative projections.

7. The method of claim 5 comprising forming the opposing insulative projections to have an elevational thickness, the removing of the trench isolation being at least to a midpoint of the elevational thickness.

8. The method of claim 7 wherein the opposing insulative projections are formed to have floors, the removing of the trench isolation not being to said floors.

9. A method of forming a field effect transistor, comprising:

forming trench isolation material on opposing sides of a semiconductor material channel region along a length of the channel region, the trench isolation material being formed to comprise upper sidewalls and opposing insulative projections below the upper sidewalls that extend laterally relative to the upper sidewalls toward one another along the channel length and with semiconductor material being received elevationally over the projections;

exposing opposing sides of the semiconductor material along the channel length by removing some of the trench isolation material and removing some of the trench isolation material from the opposing insulative projections;

removing some of the semiconductor material from the exposed opposing sides along the channel length to form a channel fin; and

forming a gate over a top and opposing sides of the fin along the channel length.

10. The method of claim 9 wherein the semiconductor material that is removed comprises bulk monocrystalline silicon.

11. The method of claim 9 wherein the semiconductor material that is removed comprises semiconductor material of a semiconductor-on-insulator substrate.

12. The method of claim 9 wherein the removing of some of the trench isolation material from the opposing insulative projections occurs prior to removing the exposed opposing sides of the semiconductor material to form the channel fin.

13. The method of claim 9 wherein at least some of the removing of the trench isolation material from the opposing insulative projections occurs commensurate with the removing of the exposed opposing sides of the semiconductor material to form the channel fin.

14. A method of forming a field effect transistor, comprising:

etching a pair of trenches within a semiconductor substrate on opposing sides of a semiconductor material channel region along a length of the channel region, the trenches comprising lined sidewalls and an exposed semiconductor material base;

etching the semiconductor material bases effective to form a bulbous lower portion of each trench, each of the bulbous lower portions comprising projections extending laterally outward relative to the lined sidewalls, a

projection of each bulbous lower portion opposing and extending toward a projection of the other bulbous lower portion;

etching through floors of the bulbous lower portions to extend the pair of trenches deeper within the semiconductor substrate;

after extending the pair of trenches, filling remaining volume of the trenches with insulative material;

after said filling, etching the insulative material to expose opposing sides of the semiconductor material along the channel length;

etching the exposed opposing sides of the semiconductor material along the channel length forming an upwardly projecting channel fin; and

forming a gate over a top and opposing sides of the fin along the channel length.

15. The method of claim 14 comprising providing the insulative material within each of the opposing projections to be at least partially received under the upwardly projecting channel fin.

16. The method of claim 14 comprising providing none of the insulative material within each of the opposing projections to be received under the upwardly projecting channel fin.

17. A field effect transistor comprising:

a semiconductor substrate comprising a pair of source/drain regions having a fin channel region received therebetween; the fin channel region comprising a channel length extending between the pair of source/drain regions, opposing channel sides extending along the length of the channel region, and a top extending along the length of the channel region; the fin channel region having a maximum thickness transverse the channel length;

a gate received over the fin channel top and the fin channel sides along the channel length; and

insulative material received immediately beneath the fin channel region and beneath the gate, such insulative material beneath the fin channel region and beneath the gate extending along all of the channel length and extending only partially across the fin channel maximum thickness transverse the channel length, such insulative material beneath the fin channel region and beneath the gate including opposing portions projecting inwardly toward one another beneath the fin channel region relative to the fin channel region maximum thickness along all of the channel length and beneath the gate along all of the channel length.

18. A field effect transistor comprising:

a bulk semiconductor substrate comprising a pair of source/drain regions having a fin channel region received therebetween; the fin channel region comprising a channel length extending between the pair of source/drain regions, opposing channel sides extending along the length of

the channel region, and a top extending along the length of the channel region;

a gate received over the fin channel top and the fin channel sides along the channel length; and

trench isolation received within the bulk semiconductor substrate elevationally lower than the fin channel region and beneath the gate, said trench isolation extending along the opposing channel sides along all of the channel length, the trench isolation in cross section transverse the channel length comprising a lower trench stem and upper transverse projections, the upper transverse projections extending from the stem transversally towards and elevationally lower than the fin channel and the gate.

19. The field effect transistor of claim 17 wherein the inwardly projecting portions respectively comprise an inwardly projecting convex surface immediately beneath the fin channel region.

20. The field effect transistor of claim 17 wherein the inwardly projecting portions respectively comprise an arcuate surface extending continuously from immediately beneath the fin channel region to parallel a line transverse the channel length.

21. A method of forming a field effect transistor, comprising:

forming trench isolation material on opposing sides of a semiconductor material channel region along a length of the channel region, the trench isolation material being formed to comprise opposing insulative projections extending toward one another partially under the channel region along the channel length and with semiconductor material being received over the projections;

exposing opposing sides of the semiconductor material along the channel length by removing some of the trench isolation material;

removing some of the semiconductor material from the exposed opposing sides along the channel length to form a channel fin projecting upwardly relative to the projections, the semiconductor material along the channel length having a top, the top being unmasked during the etching of the exposed opposing sides of the semiconductor material to form the channel fin, and further comprising etching the top during the etching of the exposed opposing sides of the semiconductor material to form the channel fin; and

forming a gate over a top and opposing sides of the fin along the channel length.

The invention clamed is:

1. A method of forming a field effect transistor, comprising:

forming trench isolation material within semiconductor material elevationally inward of opposing sides of a semiconductor material channel region lengthwise of the channel region, the trench isolation material that is elevationally inward of each of the opposing sides being formed to comprise a lower trench stem and a pair of upper transverse projections that project transversely relative to the lower trench stem, opposing sides of the semiconductor material being exposed lengthwise laterally outward of the channel region;

removing some of the semiconductor material that is laterally outward of the channel region lengthwise along the channel region and forming a channel fin with remaining of the semiconductor material; and forming a gate over a top and opposing sides of the fin lengthwise along the channel region.

2. The method of claim 1 wherein the semiconductor substrate comprises bulk monocrystalline silicon.

3. The method of claim 1 wherein the semiconductor substrate comprises a semiconductor-on-insulator substrate.

4. The method of claim 1 wherein forming the trench isolation material comprises forming the upper transverse projections to have outer surfaces which are convexly curved relative to fin thickness transverse the channel region.

5. The method of claim 1 wherein the semiconductor material lengthwise along the channel region has a top, the top being masked during the removing of semiconductor material that is laterally outward of the channel region.

6. The method of claim 1 wherein the semiconductor material lengthwise along the channel region has a top, the top being unmasked during the removing of semiconductor material that is laterally outward of the channel region, and further comprising removing semiconductor material from the top during the removing of semiconductor material that is laterally outward of the channel region.

7. The method of claim 6 wherein the removing semiconductor material from the top forms the channel region to comprising a rounded top lengthwise.

8. The method of claim 1 comprising providing the trench isolation material within one of each of the pairs of upper transverse projections to be at least partially under the channel fin.

9. The method of claim 1 comprising providing none of the trench isolation material within each of the pairs of upper transverse projections to be under the channel fin.

10. The method of claim 1 comprising forming the lower trench stems to have sidewalls that taper transversely inward.

11. A method of forming a field effect transistor, comprising:

etching a pair of trenches within a semiconductor substrate on opposing sides of a semiconductor material channel region along a length of the channel region;

etching the semiconductor material bases to form a bulbous lower portion of each trench, each of the bulbous lower portions comprising projections extending laterally outward relative to sidewalls of the trench, a projection of each bulbous lower portion opposing and extending toward a projection of the other bulbous lower portion;

etching through floors of the bulbous lower portions to extend the pair of trenches deeper within the semiconductor substrate;

after extending the pair of trenches, filling remaining volume of the trenches with insulative material;

after said filling, etching the insulative material to expose opposing sides of the semiconductor material along the channel length;

etching the exposed opposing sides of the semiconductor material along the channel length forming an upwardly projecting channel fin; and

forming a gate over a top and opposing sides of the fin along the channel length.

12. The method of claim 11 comprising providing the insulative material within each of the opposing projections to be at least partially received under the upwardly projecting channel fin.

13. The method of claim 11 comprising providing none of the insulative material within each of the opposing projections to be received under the upwardly projecting channel fin.

14. A plurality of field effect transistors wherein individual of the field effect transistors of the plurality comprise:

a bulk semiconductor substrate comprising a pair of source/drain regions having a fin channel region received therebetween; the fin channel region comprising a channel length extending between the pair of source/drain regions, opposing channel sides extending along the length of the channel region, and a top extending along the length of the channel region;

a gate received over the fin channel top and the fin channel sides along the channel length; and

trench isolation received within the bulk semiconductor substrate elevationally lower than the fin channel region and beneath the gate, said trench isolation extending along the opposing channel sides along the channel length, the trench isolation in cross section transverse the channel length comprising a lower trench stem and upper transverse projections, the upper transverse projections extending from the stem transversally towards and elevationally lower than the fin channel and the gate.

15. The transistors of claim 14 wherein the lower trench stem has sidewalls that taper transversely inward.

16. DRAM circuitry comprising a plurality of individual memory cells wherein individual of the memory cells comprise a field effect transistor having a pair of source/drain regions, a capacitor connected with one of the source/drain regions, and a bit line contact connected with another of the source/drain regions, the field effect transistor comprising:

a semiconductor substrate comprising the pair of source/drain regions and having a fin channel region received between the pair of source/drain regions; the fin channel region comprising a channel length extending between the pair of source/drain regions, opposing channel sides extending along the length of the channel region, and a top extending along the length of the channel region; the fin channel region having a maximum thickness transverse the channel length;

a gate received over the fin channel top and the fin channel sides along the channel length; and

insulative material received immediately beneath the fin channel region and beneath the gate, such insulative material beneath the fin channel region and beneath the gate extending along the channel length and extending only partially across the fin channel maximum thickness transverse the channel length, such insulative material beneath the fin channel region and beneath the gate including opposing portions projecting inwardly toward one another beneath the fin channel

region relative to the fin channel region maximum thickness and beneath the gate along the channel length.

17. The DRAM circuitry of claim 16 wherein the lower trench stem has sidewalls that taper transversely inward.

18. DRAM circuitry comprising a plurality of individual memory cells wherein individual of the memory cells comprise a field effect transistor having a pair of source/drain regions, a capacitor connected with one of the source/drain regions, and a bit line contact connected with another of the source/drain regions, the field effect transistor comprising:

a bulk semiconductor substrate comprising the pair of source/drain regions and having a fin channel region received between the source/drain regions; the fin channel region comprising a channel length extending between the pair of source/drain regions, opposing channel sides extending along the length of the channel region, and a top extending along the length of the channel region;

a gate received over the fin channel top and the fin channel sides along the channel length; and

trench isolation received within the bulk semiconductor substrate elevationally lower than the fin channel region and beneath the gate, said trench isolation extending along the opposing channel sides along the channel length, the trench isolation in cross section transverse the channel length comprising a lower trench stem and upper transverse projections, the upper transverse projections extending from the stem transversally towards and elevationally lower than the fin channel and the gate.

19. The DRAM circuitry of claim 18 wherein the lower trench stem has sidewalls that taper transversely inward.