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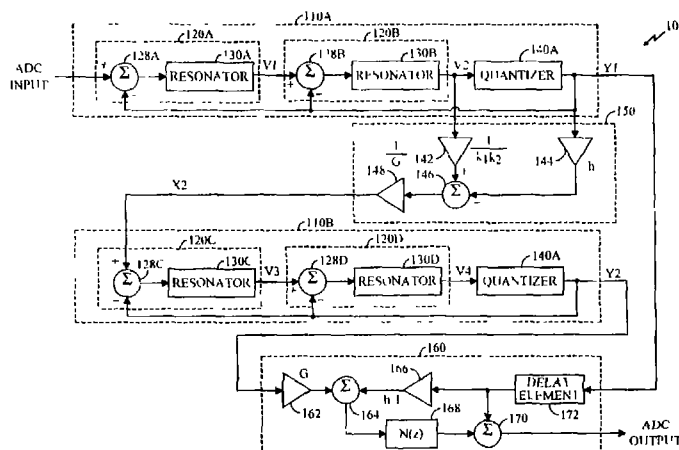
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(54) Title: METHOD AND APPARATUS FOR CONTROLLING STAGES OF A MULTI-STAGE CIRCUIT



(57) Abstract: A control mechanism that can be used to control a $\Sigma\Delta$ to provide the required level of performance while reducing power consumption. The $\Sigma\Delta$ ADC is designed with multiple stage (i.e., loops or sections), and provides improved performance (e.g., higher dynamic range) as more stages are enabled. The control mechanism selectively enables a sufficient number of stages to provide the required performance and disables remaining stages to conserve power. The control mechanism achieves this by measuring one or more characteristics (e.g., signal level) of the ADC input signal through a $\Sigma\Delta$ ADC that is similar to the $\Sigma\Delta$ ADC on the signal path, comparing the measured characteristic(s) to particular threshold level(s), and controlling the stages such that the desired objectives are achieved. In one implementation, the control circuit includes one or more detector stages, a conditioning circuit, and a signal processor. The detector stage(s) receive the input signal and provide a detected signal. The conditioning circuit receives the detected signal and provides conditioned samples. The signal processor receives the conditioned samples and provides a control signal that selectively disables zero or more $\Sigma\Delta$ stages in the $\Sigma\Delta$ ADC.