

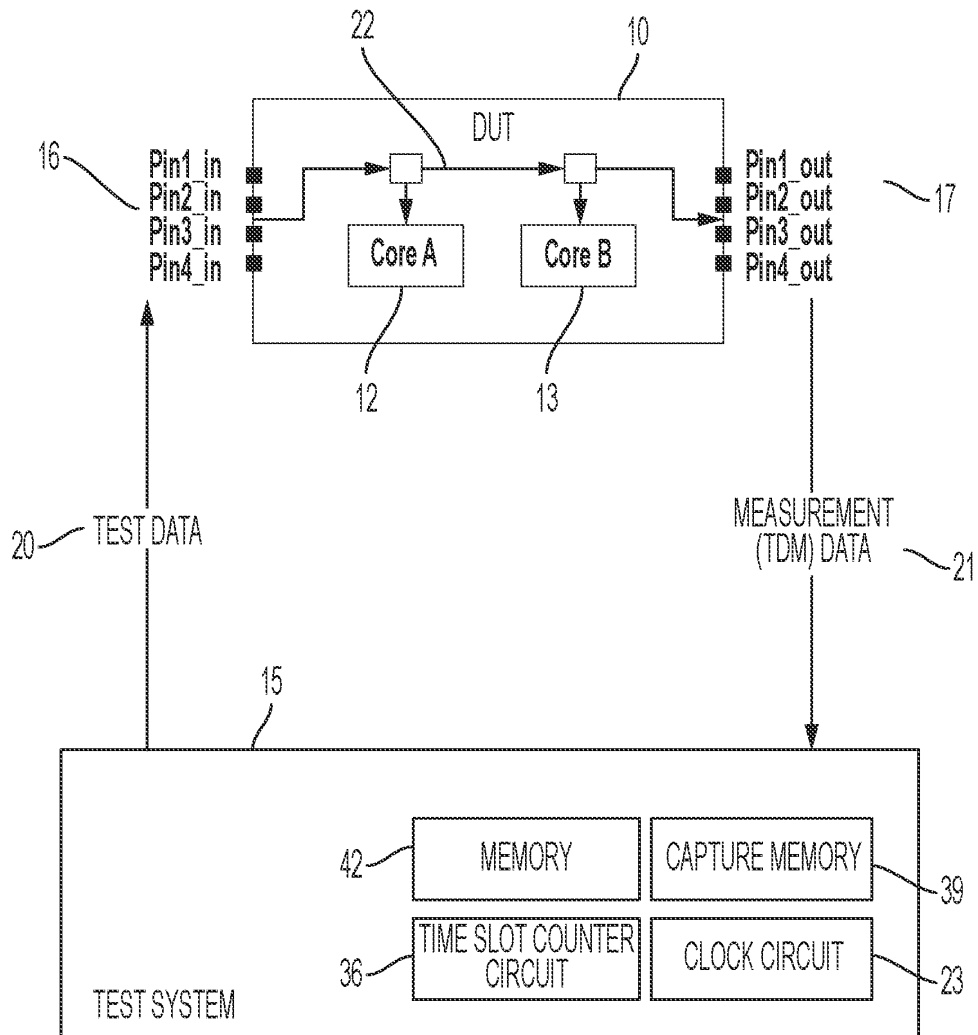


FIG. 1

256

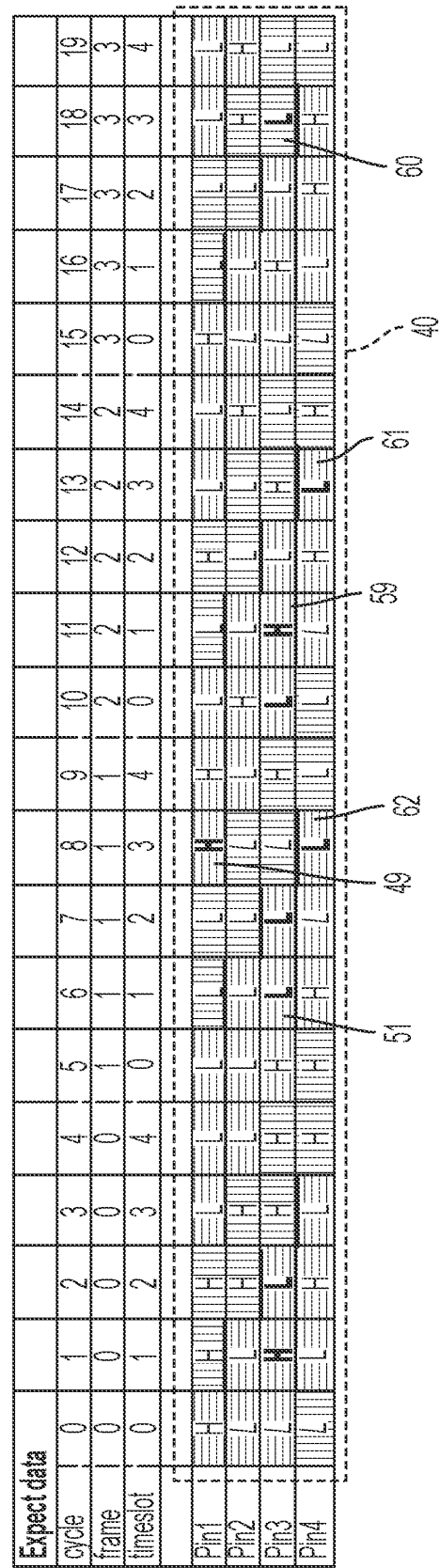


FIG. 4

Stored Result (by Pin)					Fall limit-5																									
cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19										
frame	0	0	0	0	0	1	1	1	1	1	2	2	2	2	2	3	3	3	3	3										
timeslot	0	1	2	3	4	0	1	2	3	4	0	1	2	3	4	0	1	2	3	4										
Pin1	H					L					L					L														
Pin2	L					L					H					L														
Pin3	H					L					L					L														
Pin4	L					H					L					L														

FIG. 5
PRIORART

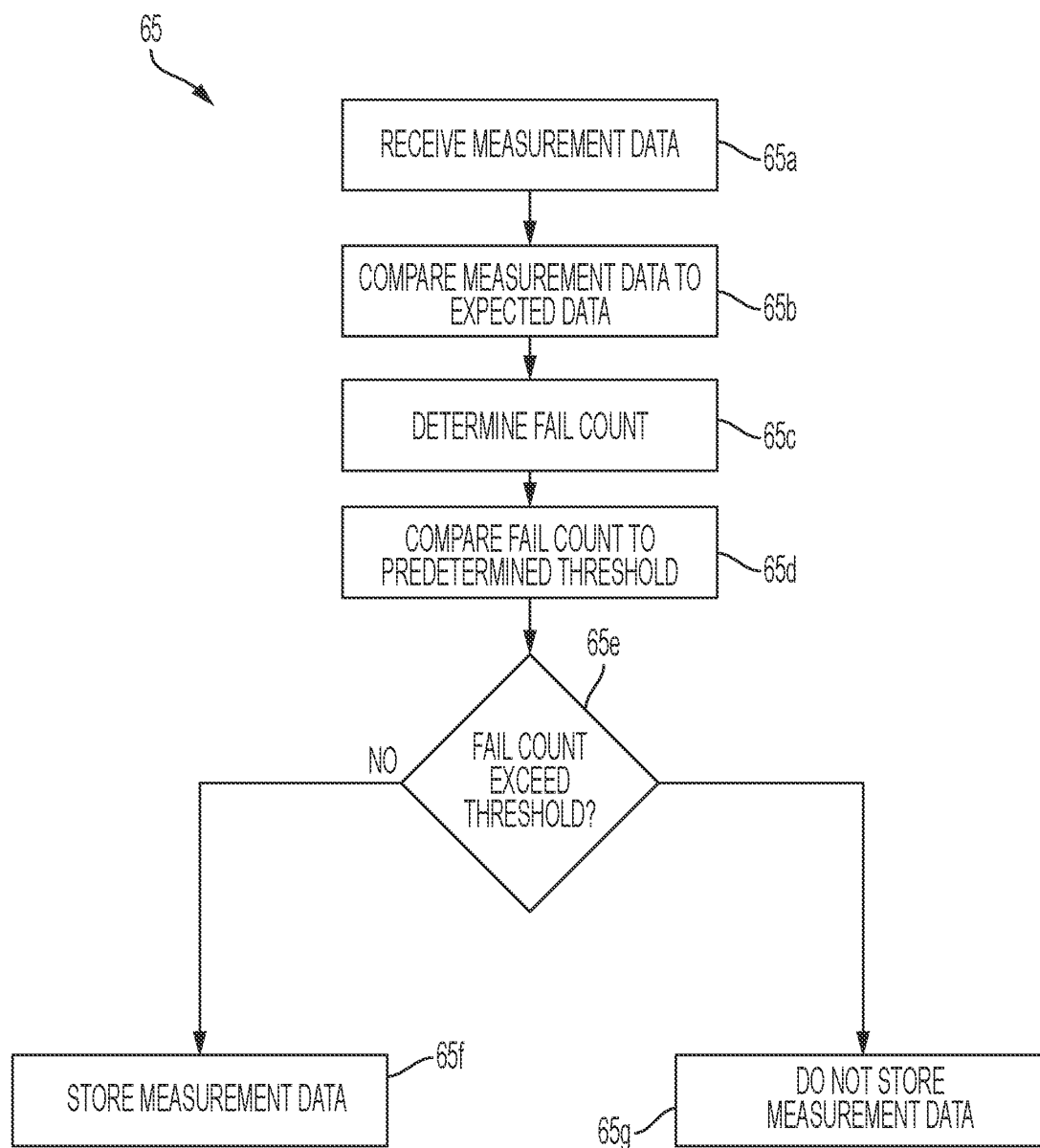


FIG. 6

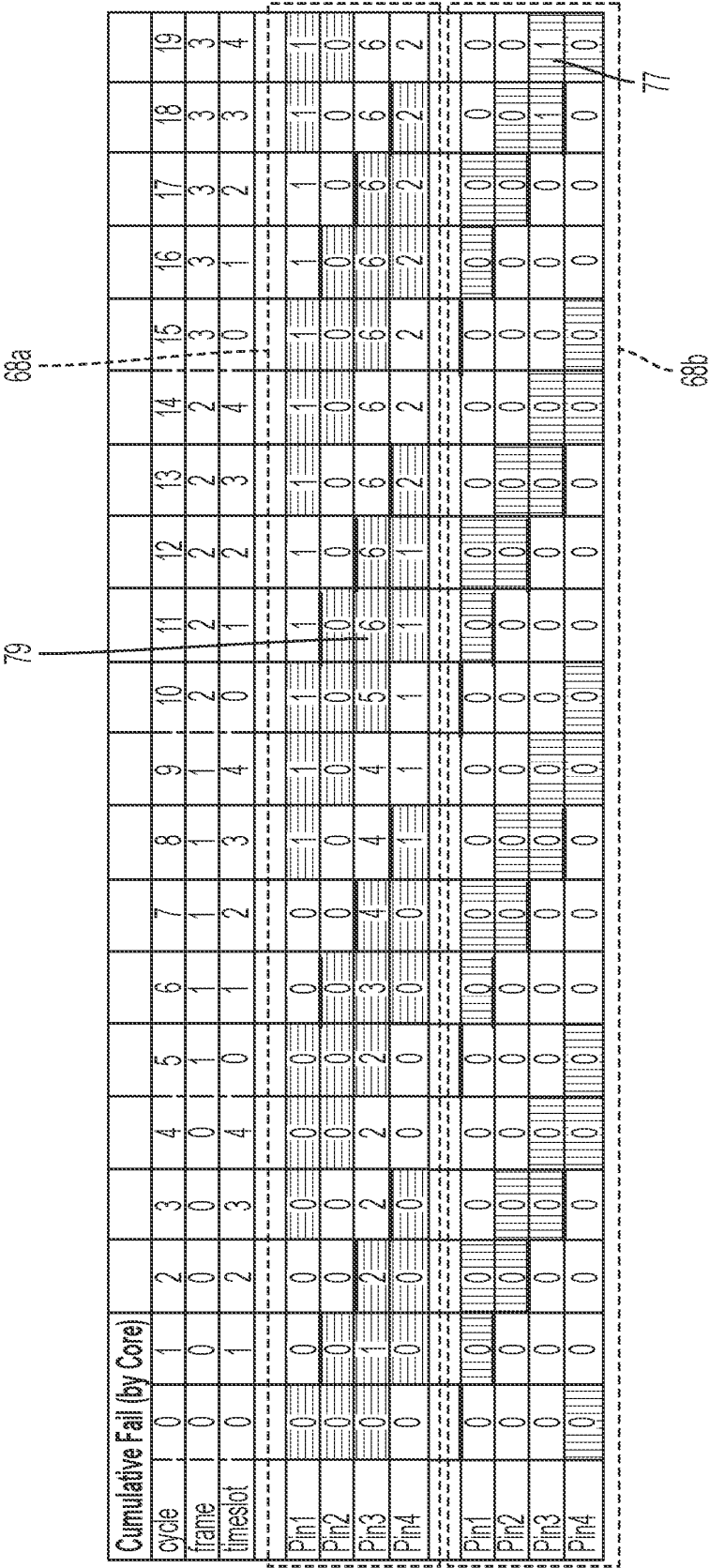


FIG. 7

Stored Result (by Core)		Fail limit: 5																				
cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19		
frame	0	0	0	0	0	1	1	1	1	1	2	2	2	2	2	3	3	3	3	3		
timeslot	0	1	2	3	4	0	1	2	3	4	0	1	2	3	4	0	1	2	3	4		
Pin1		H	H				L	L	H		L		L	L					L			
Pin2		L	H				L	L	L		H		L	L					H			
Pin3		H	L				L	L	L		L		L	H					L			
Pin4		L	H				H	L	L		L		L	L					L			

79

77

FIG. 8

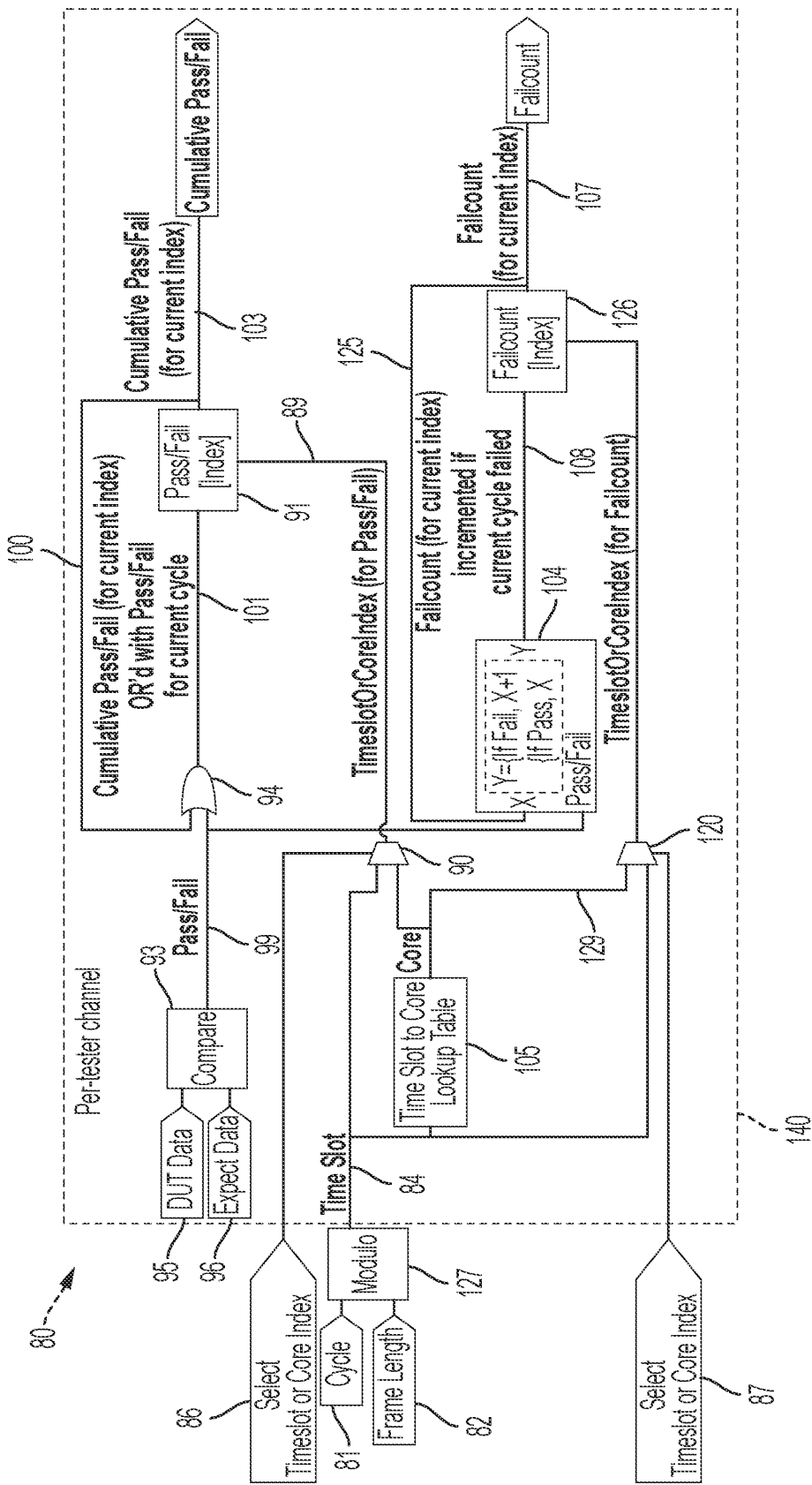


FIG. 9

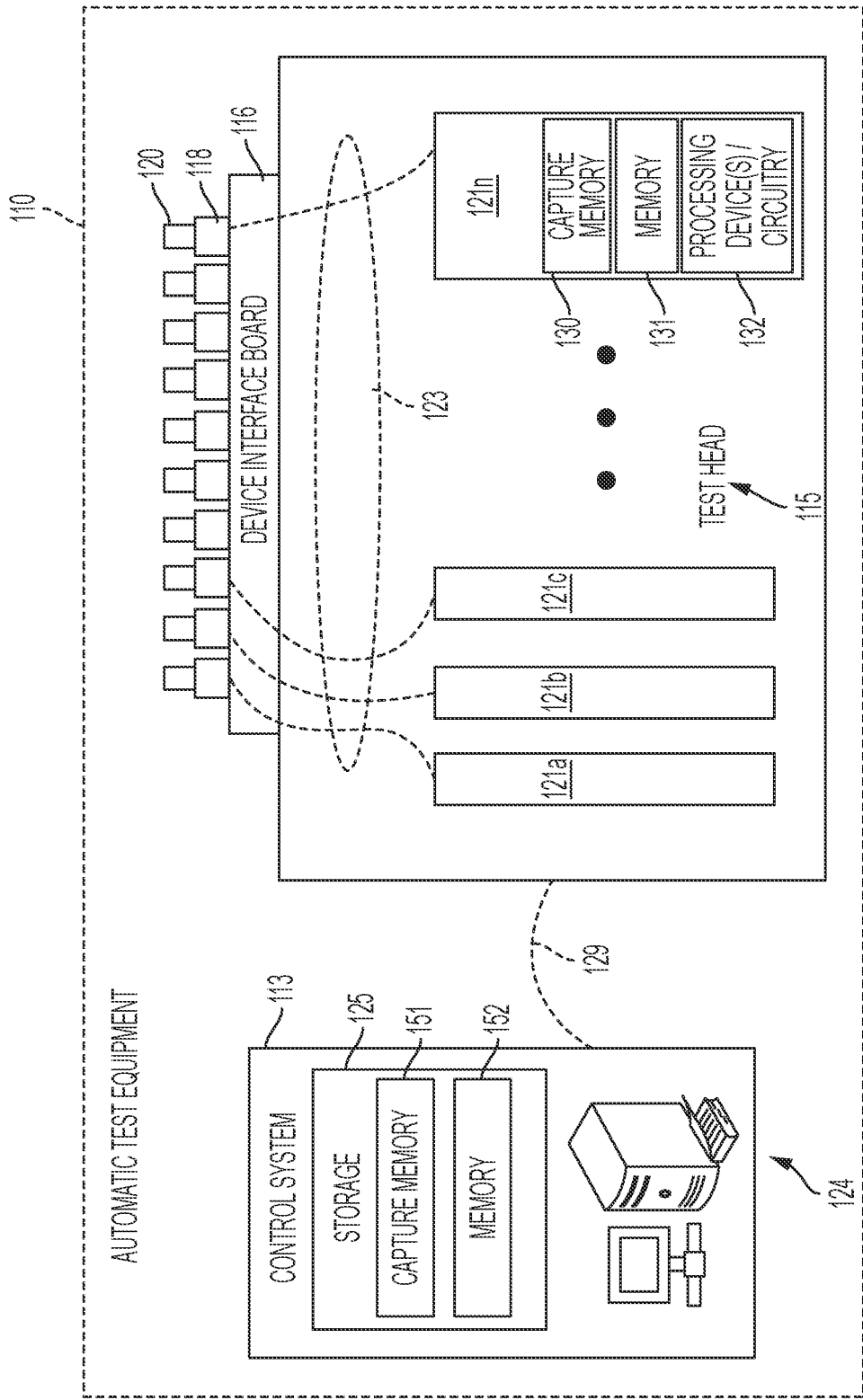


FIG. 10