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LARGE ANGLE TILT IMPLANT (LATI) METHOD FOR FORMING A LIGHTLY DOPED DRAIN (LDD)

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) within integrated circuits. More particularly, the present invention relates to methods for forming Lightly Doped Drain (LDD) low dose ion implant structures within Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) within integrated circuits.

2. Description of the Related Art

As integrated circuit technology has advanced, and integrated circuit device and conductor element dimensions have decreased, several novel effects have developed within advanced integrated circuits. Within advanced integrated circuits within which there are formed Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), one group of such novel effects is the Short Channel Effects (SCEs). Short Channel Effects (SCEs) derive from the narrowing of gate electrode widths upon semiconductor substrates within Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) within advanced integrated circuits, in conjunction with the thinning of gate oxide layers which reside beneath those gate electrodes.

A particularly common Short Channel Effect (SCE) is the Hot Carrier Effect (HCE). The Hot Carrier Effect (HCE) derives from increases in electric fields within semiconductor

substrates beneath gate electrode edges of advanced Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) due to thinning of those gate oxide layers under constant Metal Oxide Semiconductor Field Effect Transistor (MOSFET) operating voltage. The Hot Carrier Effect (HCE) is manifested as increases in sub-threshold currents within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) as charge carriers are injected from the semiconductor substrate upon which is formed the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) into the gate oxide layer or gate electrode of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), where the charge carriers are trapped within the material from which is formed the gate oxide layer or gate electrode.

In order to minimize Hot Carrier Effects (HCEs) within Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) within advanced integrated circuits, it has become common in the art to employ Lightly Doped Drain (LDD) low dose ion implant structures within the semiconductor substrate region beneath the gate electrode edges within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) of dimensions and operating voltage which make the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) susceptible to the Hot Carrier Effect (HCE). As illustrated specifically in Fig. 1, the Lightly Doped Drain (LDD) low dose ion implant structures 18a and 18b may be formed in a self-aligned fashion within a semiconductor substrate 10 having an active region defined by the isolation regions 12a and 12b by employing a gate oxide layer 14 and a gate electrode 16 as a mask through which is implanted a dose of substantially orthogonal low dose implanting ions 20. As further illustrated in Fig. 2, the source/drain electrode high dose ion implant structures 24a and 24b are typically subsequently formed partially overlapping the Lightly Doped Drain (LDD) low dose ion implant structures 18a and 18b in an analogous self-aligned fashion within the integrated circuit whose structure is illustrated in Fig. 1 through implanting a dose of substantially orthogonal high dose implanting ions 26 into the active region of the semiconductor substrate 10

employing the gate oxide layer 14, the gate electrode 16 and a pair of insulator spacers 22a and 22b as a mask. Subsequent to forming either the Lightly Doped Drain (LDD) low dose ion implant structures 18a and 18b or the source/drain electrode high dose ion implant structures 24a and 24b, the semiconductor substrate 10 is typically annealed to repair any semiconductor substrate 30 damage due to the ion implanting and/or to further drive in the Lightly Doped Drain (LDD) low dose ion implant structures 18a and 18b beneath the gate electrode 16 edges.

More recently, several novel and non-traditional methods have also been disclosed in the art for forming graded Lightly Doped Drain (LDD) low dose ion implant structures which partially overlap source/drain electrode high dose ion implant structures within advanced Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) within integrated circuits. The graded Lightly Doped Drain (LDD) low dose ion implant structures formed through the methods typically exhibit reduced series resistance, thus providing Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) with increased saturation currents. The disclosed methods employ a non-orthogonal Large Angle Tilt Implant (LATI) method for implanting dopants when forming the graded Lightly Doped Drain (LDD) low dose ion implant structures.

For example, Shimizu et al. in U.S. Patent No. 5,217,910 disclose a triple ion implant method for forming a graded Lightly Doped Drain (LDD) low dose ion implant structure and a partially overlapping adjoining source/drain electrode high dose ion implant structure within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The first two ion implants of the triple ion implant method are Large Angle Tilt Implants (LATIs) formed before and after forming an insulator spacer adjoining the edge of the gate electrode within the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Analogously, Okabe et al. in U.S. Patent 5,292,674 also disclose a triple ion implant method for forming a graded Lightly Doped Drain (LDD) low dose ion implant structure and

a partially overlapping adjoining source/drain electrode high dose ion implant structure within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Within the disclosed method, the intermediate ion implant of the triple ion implant method is a Large Angle Tilt Implant (LATI) implant. Finally, there is disclosed by Liang et al. in U.S. Patent No. 5,372,957 yet another method for forming a graded Lightly Doped Drain (LDD) low dose ion implant structure and a partially overlapping adjoining source/drain electrode high dose ion implant structure within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The method employs forming through a Large Angle Tilt Implant (LATI) method a minimum of three successively more heavily doped regions at a minimum of three separate angles within a semiconductor substrate adjoining the gate electrode edges of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). There is then formed an insulator spacer adjoining the gate electrode and a source/drain electrode high dose ion implant structure adjoining the insulator spacer.

Although each of the preceding methods provides value in forming low series resistance Lightly Doped Drain (LDD) low dose ion implant structures partially overlapping source/drain electrode high dose ion implant structures within Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) within integrated circuits, each of the preceding methods relies upon forming adjoining a gate electrode within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) an insulator spacer either integral to the method through which is formed the Lightly Doped Drain (LDD) low dose ion implant structure or subsequent to forming the Lightly Doped Drain (LDD) low dose ion implant structure. The insulator spacer is employed, at least in part, in defining the location of the Lightly Doped Drain (LDD) low dose ion implant structure with respect to the source/drain electrode high dose ion implant structure.

Desirable in the art are additional novel methods through which a Large Angle Tilt

Implant (LATI) method may be employed in forming within advanced Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) Lightly Doped Drain (LDD) low dose ion implant structures which partially overlap source/drain electrode high dose ion implant structures. Particularly desirable are methods through which may be formed Lightly Doped Drain (LDD) low dose ion implant structures and subsequently be formed source/drain electrode high dose ion implant structures partially overlapping those Lightly Doped Drain (LDD) low dose ion implant structures without the need for forming an intervening insulator spacer to define the location of the source/drain electrode high dose ion implant structure with respect to the Lightly Doped Drain (LDD) low dose ion implant structure. Such methods are desirable since they would provide for manufacturing efficiency.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a novel method through which a Large Angle Tilt Implant (LATI) implant may be employed in forming within a semiconductor substrate adjoining a gate electrode edge of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) a Lightly Doped Drain (LDD) low dose ion implant structure which partially overlaps a source/drain electrode high dose ion implant structure.

A second object of the present invention is to provide a method in accord with the first object of the present invention, which method also does not require forming an insulator spacer adjoining the gate electrode edge of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) to define the location of the Lightly Doped Drain (LDD) low dose ion implant structure with respect to the source/drain electrode high dose ion implant structure.

In accord with the objects of the present invention, there is provided a method for forming within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) within an integrated circuit a Lightly Doped Drain (LDD) low dose ion implant structure which partially overlaps a source/drain electrode high dose ion implant structure. To form the Lightly Doped Drain (LDD) low dose ion implant structure there is formed upon a semiconductor substrate a gate dielectric layer having formed thereupon a gate electrode. Formed then upon the exposed portions of the semiconductor substrate, the gate dielectric layer and the gate electrode is an insulator layer. Finally, there is implanted through a Large Angle Tilt Implant (LATI) method a minimum of one low dose ion implant through the insulator layer and into the semiconductor substrate to form a Lightly Doped Drain (LDD) low dose ion implant structure within the semiconductor substrate. The Lightly Doped Drain (LDD) low dose ion implant structure includes a portion of the semiconductor substrate beneath the gate electrode edges.

As an extension of the method of the present invention, there may additionally be implanted substantially orthogonally to the semiconductor substrate a minimum of one high dose ion implant also through the insulator layer and into the semiconductor substrate. The high dose ion implant is employed in forming a source/drain electrode high dose ion implant structure partially overlapping the Lightly Doped Drain (LDD) low dose ion implant structure. The source/drain electrode high dose ion implant structure is formed adjoining but not beneath the gate electrode edges.

As a further extension of the present invention there may be formed a polysilicon layer upon the insulator layer either before forming the low dose ion implant structure and the high dose ion implant structure, interposed between forming the low dose ion implant structure and the high dose ion implant structure or after forming the low dose ion implant structure and the high dose ion

implant structure. The polysilicon layer, if present, and/or the insulator layer, may optionally be anisotropically etched to form a polysilicon spacer and/or an insulator spacer. When the polysilicon layer is formed before the low dose ion implant or the high dose ion implant, there is formed a corresponding a low dose ion implant structure or high dose ion implant structure with a comparatively shallow junction which assists in reducing Short Channel Effects (SCEs).

Through the method of the present invention, a dose of Large Angle Tilt Implant (LATI) low dose implanting ions may be employed in forming within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) within an integrated circuit a Lightly Doped Drain (LDD) low dose ion implant structure which partially overlaps a source/drain electrode high dose ion implant structure. Analogously with methods conventional to the art, the method of the present invention provides a minimum of one Large Angle Tilt Implant (LATI) implant which is employed in forming a Lightly Doped Drain (LDD) low dose ion implant structure which partially overlaps a source/drain electrode high dose ion implant structure within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Contrary to methods known in the art, the present invention provides a method whereby the need for forming an insulator spacer to define the location of the Lightly Doped Drain (LDD) low dose ion implant structure with respect to the source/drain electrode high dose ion implant structure may be avoided.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiments, as set forth below. The Description of the Preferred Embodiments is understood within the context of the accompanying drawings, which

form a material part of this disclosure, wherein:

Fig. 1 and Fig. 2 show a pair of schematic cross-sectional diagrams illustrating the results of progressive process stages in forming within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) a Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure through a method conventional to the art.

Fig. 3 to Fig. 5 show a series of schematic cross-sectional diagrams illustrating the results of progressive process stages in forming within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) a Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure through the first preferred embodiment of the method of the present invention.

Fig. 6 to Fig. 9 show a series of schematic cross-sectional diagrams illustrating the results of progressive process stages in forming within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) a Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure through the second preferred embodiment of the method of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method for forming within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) within an integrated circuit a Lightly Doped Drain

(LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure. Through the method of the present invention, the Lightly Doped Drain (LDD) low dose ion implant structure may be formed partially overlapping the source/drain electrode high dose ion implant structure without forming an insulator spacer adjoining the gate electrode edge of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Such an insulator spacer is conventionally employed in defining within the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) the location of the Lightly Doped Drain (LDD) low dose ion implant structure with respect to the source/drain electrode high dose ion implant structure.

The method of the present invention may be employed in forming Lightly Doped Drain (LDD) low dose ion implant structures partially overlapping source/drain electrode high dose ion implant structures within Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) within integrated circuits including but not limited to Dynamic Random Access Memory (DRAM) integrated circuits, Static Random Access Memory (SRAM) integrated circuits and Application Specific Integrated Circuits (ASICs). The method of the present invention has broad applicability in forming within Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) within integrated circuits Lightly Doped Drain (LDD) low dose ion implant structures partially overlapping source/drain electrode high dose ion implant structures.

Referring now to Fig. 3 to Fig. 5, there is shown a series of schematic cross-sectional diagrams illustrating the results of progressive process steps in forming within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) a Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure in accord with the first preferred embodiment of the method of the present invention. Shown in Fig. 3 is a schematic cross-sectional diagram of the Metal Oxide Semiconductor Field Effect Transistor

(MOSFET) at its early stages of fabrication.

Shown in Fig. 3 is a semiconductor substrate 30 within and upon whose surface is formed isolation regions 32a and 32b which define the active region of the semiconductor substrate 30. Although the semiconductor substrate 30 upon which may be practiced the first preferred embodiment of the method of the present invention may have either dopant polarity and any crystallographic orientation, the semiconductor substrate 30 upon which is practiced the first preferred embodiment of the method of the present invention is preferably a (100) silicon semiconductor substrate having either an N- or P- doping.

Methods and materials through which isolation regions may be formed to define active regions within and/or upon semiconductor substrates are known in the art of integrated circuit manufacture. Isolation regions may be formed to define active regions of semiconductor substrates through methods including but not limited to thermal oxidation methods whereby portions of a semiconductor substrate exposed through a suitable oxidation mask are oxidized to form isolation regions within and upon the semiconductor substrate, and insulator layer deposition methods whereby an insulator layer is independently formed upon the surface of a semiconductor substrate and subsequently patterned to form isolation regions upon the semiconductor substrate. For the first preferred embodiment of the method of the present invention, the isolation regions 32a and 32b are preferably formed through a thermal oxidation method whereby portions of the semiconductor substrate 30 exposed through a suitable oxidation mask are oxidized at a temperature of from about 850 to about 1200 degrees centigrade to form isolation regions 32a and 32b of silicon oxide within and upon the semiconductor substrate 30.

Also shown in Fig. 3 is a gate oxide layer 34 upon which resides a gate electrode 36,

both of which reside upon the active region of the semiconductor substrate 30. Methods and materials through which both gate oxide layers and gate electrodes may be formed upon active regions of semiconductor substrates are known in the art of integrated circuit manufacture. Gate oxide layers are typically formed through patterning through methods as are conventional in the art of blanket gate oxide layers which are formed upon the surfaces of active regions of semiconductor substrates. The blanket gate oxide layers may be formed through methods including but not limited to thermal oxidation methods whereby blanket gate oxide layers are grown through thermal oxidation of active regions of semiconductor substrates and oxide layer deposition methods whereby blanket gate oxide layers are deposited upon the active regions of semiconductor substrates.

Analogously with gate oxide layers, gate electrodes may also be patterned through methods as are conventional in the art of blanket layers of gate electrode materials formed upon blanket gate oxide layers. The blanket layers of gate electrode materials may be formed through methods including but not limited to Chemical Vapor Deposition (CVD) methods, Plasma Enhanced Chemical Vapor Deposition (PECVD) methods and Physical Vapor Deposition (PVD) sputtering methods through which may be formed gate electrode materials including but not limited to metals, metal alloys, highly doped polysilicon and polycides (highly doped polysilicon/metal silicide stacks).

For the first preferred embodiment of the method of the present invention, the gate oxide layer 34 is preferably formed through patterning through methods as are conventional in the art of a blanket gate oxide layer formed through thermal oxidation of the active region of the semiconductor substrate at a temperature of about 800 to about 1000 degrees centigrade to yield a blanket gate oxide layer of thickness about 40 to about 150 angstroms. For the first preferred embodiment of the method of the present invention, the gate electrode 36 is preferably formed through patterning through methods as are conventional in the art of a blanket layer of gate electrode

material formed of a highly doped polysilicon or a tungsten silicide polycide at a thickness of from about 2000 to about 4000 angstroms. Once the blanket layer of gate electrode material has been patterned to yield the gate electrode 36, the gate electrode 36 may be employed in patterning the gate oxide layer 34 from the blanket gate oxide layer.

Finally, there is shown in Fig. 3 the presence of a blanket insulator layer 38 formed upon the exposed portions of the isolation regions 32a and 32b, the active region of the semiconductor substrate 30, the gate oxide layer 34 and the gate electrode 36. Methods and materials through which blanket insulator layers may be formed within integrated circuits are known within the art of integrated circuit manufacture. Blanket insulator layers may be formed within integrated circuits through methods including but not limited to Chemical Vapor Deposition (CVD) methods, Plasma Enhanced Chemical Vapor Deposition (PECVD) methods and Physical Vapor Deposition (PVD) sputtering methods through which may be formed blanket insulator layers of insulator materials including but not limited to silicon oxide insulator materials, silicon nitride insulator materials and silicon oxynitride insulator materials. Although other insulator materials may be employed, for the first preferred embodiment of the method of the present invention the blanket insulator layer 38 is preferably formed of a silicon oxide insulator material deposited through a Low Pressure Chemical Vapor Deposition (LPCVD) method. Preferably, the blanket insulator layer 38 is a conformal insulator layer formed to a thickness of from about 400 to about 1000 angstroms.

Referring now to Fig. 4, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) whose schematic cross-sectional diagram is illustrated in Fig. 3. Shown in Fig. 4 is the presence of the Lightly Doped Drain (LDD) low dose ion implant structures 40a and 40b formed into the active region of the semiconductor substrate 30 through a dose of Large Angle Tilt Implant

(LATI) low dose implanting ions 42. Novel to the present invention is the implanting of the dose of Large Angle Tilt Implant (LATI) low dose implanting ions 42 through the insulator layer 38 and into the active region of the semiconductor substrate. Conventionally, Large Angle Tilt Implant (LATI) implanting ions are not implanted through an insulator layer. For the first preferred embodiment of the method of the present invention, the implanting of the dose of Large Angle Tilt Implant (LATI) low dose implanting ion 42 through the insulator layer 38 provides value in forming the Lightly Doped Drain (LDD) low dose ion implant structures 40a and 40b into the active region of the semiconductor substrate 30 when the width of the gate oxide layer 34 and the gate electrode is from about 1500 to about 5000 angstroms. Under such circumstances, the first preferred embodiment of the method of the present invention provides Lightly Doped Drain (LDD) low dose ion implant structures 40a and 40b which penetrate sufficiently laterally within the semiconductor substrate 30 beneath the gate electrode 36 edges to effectively limit the Hot Carrier Effect (HCE) within the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) within which is formed the Lightly Doped Drain (LDD) low dose ion implant structures 40a and 40b.

As discussed within the foregoing Description of the Related Art, methods and materials through which Lightly Doped Drain (LDD) low dose ion implant structures may in general be formed within semiconductor substrates beneath gate electrode edges of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are known in the art of integrated circuit manufacture. By analogy, methods and materials through which Lightly Doped Drain (LDD) low dose ion implant structures may be formed within semiconductor substrates beneath gate electrode edges of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) via implanting through an insulator layer should be readily accessible given appropriate adjustment of the energy and dose of the implanting species. Further, as is known in the art, arsenic dopant species, boron dopant species and phosphorus dopant species are common in the art of forming Lightly Doped Drain (LDD)

low dose ion implant structures within Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

Thus, for the first preferred embodiment of the method of the present invention, the dose of Large Angle Tilt Implant (LATI) low dose implanting ions 42 is preferably provided through implanting either arsenic dopant species, boron dopant species or phosphorus dopant species through the blanket insulator layer 38 and into the active region of the semiconductor substrate 30 at an ion implantation dose of from about 1E13 to about 1E14 ions per square centimeter and an ion implantation energy of from about 50 to about 150 keV. Preferably, the dose of Large Angle Tilt Implant (LATI) low dose implanting ions 42 is provided through the insulator layer 38 and into the semiconductor substrate 30 at a tilt angle of from about 15 to about 45 degrees with respect to the orthogonal to the semiconductor substrate 30.

Referring now to Fig. 5, there is shown a schematic cross sectional diagram illustrating the results of further processing of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) whose schematic cross-sectional diagram is illustrated in Fig. 4. Shown in Fig. 5 is the presence of source/drain electrode high dose ion implant structures 44a and 44b formed into the active region of the semiconductor substrate 30 partially overlapping the Lightly Doped Drain (LDD) low dose ion implant structures 40a and 40b. The source/drain electrode high dose ion implant structures 44a and 44b are formed through implanting a dose of substantially orthogonal high dose implanting ions 46 into the active region of the semiconductor substrate 30.

Analogously with the methods and materials through which the Lightly Doped Drain (LDD) low dose ion implant structures 40a and 40b are formed within the semiconductor substrate 30, the source/drain electrode high dose ion implant structures 44a and 44b are also formed through

implanting dopant species through the insulator layer 38. Analogously with the dopant species through which is provided the dose of Large Angle Tilt Implant (LATI) low dose implanting ions 42, the dopant species through which is provided the dose of substantially orthogonal high dose implanting ions 46 may also be chosen from the group of dopant species consisting of arsenic dopant species, boron dopant species and phosphorus dopant species. Preferably, the polarity of the dopant species employed in providing the dose of substantially orthogonal high dose implanting ions 46 is equivalent to the polarity of the dopant species employed in providing the dose of Large Angle Tilt Implant (LATI) low dose implanting ions 42. Preferably the dose of substantially orthogonal high dose implanting ions 46 is provided at an ion implantation dose of from about 1E15 to about 1E16 ions per square centimeter and an ion implantation energy of from about 50 to about 150 keV. In practice, it is typical within the first preferred embodiment of the method of the present invention that the dose of substantially orthogonal high dose implanting ions 46 be provided at an angle of from about zero to about 7 degrees from the orthogonal to the semiconductor substrate 30.

Upon forming the source/drain electrode high dose ion implant structures 44a and 44b within the semiconductor substrate 30 through the dose of substantially orthogonal high dose implanting ions 46, there is formed a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) through the first preferred embodiment of the method of the present invention. The Metal Oxide Semiconductor Field Effect Transistor Field Effect Transistor (MOSFET) formed through the first preferred embodiment of the method of the present invention has formed therein a Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure. The Lightly Doped Drain (LDD) low dose ion implant structure and the source/drain electrode high dose ion implant structure are formed sequentially in-situ without sequentially forming therebetween an insulator spacer adjoining the edge of the gate electrode within the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which insulator spacer would

otherwise be employed in defining the location of the Lightly Doped Drain (LDD) low dose ion implant structure with respect to the source/drain electrode high dose ion implant structure.

In addition to the first preferred embodiment of the method of the present invention, there also exists a second preferred embodiment of the method of the present invention. A series of schematic cross-sectional diagrams illustrating the results of progressive process stages in forming within an integrated circuit a Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) through the second preferred embodiment of the method of the present invention is shown by reference to Fig. 6 to Fig. 9. With noted exceptions, the methods, materials, structures and dimensions through which is formed the Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping the source/drain electrode high dose ion implant structure within the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) formed through the second preferred embodiment of the method of the present invention are equivalent to the methods, materials, structures and dimensions through which is formed the Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping the source/drain electrode high dose ion implant structure within the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) formed through the first preferred embodiment of the method of the present invention. Shown in Fig. 6 is the results of early stages of processing of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

Shown in Fig. 6 is a schematic cross-sectional diagram of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) otherwise equivalent to the schematic cross-sectional diagram of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) shown in Fig. 3, with the exception that there is added within the Metal Oxide Semiconductor Field Effect

Transistor (MOSFET) whose schematic cross-sectional diagram is illustrated in Fig. 6 a blanket polysilicon layer 39. The blanket polysilicon layer 39 is preferably an undoped blanket polysilicon layer. Methods and materials through which undoped blanket polysilicon layers may be formed within integrated circuits are known in the art. Undoped blanket polysilicon layers may be formed through methods including but not limited to Chemical Vapor Deposition (CVD) methods, Low Pressure Chemical Vapor Deposition (LPCVD) methods and Physical Vapor Deposition (PVD) sputtering methods through which may be deposited undoped blanket polysilicon layers from suitable silicon source materials. For the second preferred embodiment of the method of the present invention, the blanket polysilicon layer 39 is preferably formed through a Low Pressure Chemical Vapor Deposition (LPCVD) method employing a suitable silicon source material. Preferably, the blanket polysilicon layer 39 is from about 500 to about 1500 angstroms thick.

Referring now to Fig. 7 there is show a schematic cross-sectional diagram illustrating the results of further processing of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) whose schematic cross-sectional diagram is illustrated in Fig. 6. Analogously with the first preferred embodiment of the method of the present invention, the schematic cross-sectional diagram of Fig. 7 illustrates within the second preferred embodiment of the method of the present invention the formation of the Lightly Doped Drain (LDD) low dose ion implant structures 40a' and 40b' within the semiconductor substrate 30. The methods and materials through which are formed the Lightly Doped Drain (LDD) low dose ion implant structures 40a' and 40b' within the second preferred embodiment of the method of the present invention are analogous to the methods and materials employed in forming the Lightly Doped Drain (LDD) low dose ion implant structures 40a and 40b within the first preferred embodiment of the method of the present invention with the exception that the ion implantation energy may be increased somewhat in order to assure adequate penetration of the dose of Large Angle Tilt Implant (LATI) low dose implanting ions 42' through

both the blanket polysilicon layer 39 and the blanket insulator layer 38. Thus, for the second preferred embodiment of the method of the present invention, the dose of Large Angle Tilt Implant (LATI) low dose implanting ions 42' is preferably provided at a tilt angle of from about 15 to about 45 degrees from the orthogonal to the semiconductor substrate 30, at an ion implantation dose of from about 1E13 to about 1E14 ions per square centimeter and at an ion implantation energy of from about 50 to about 150 keV.

Referring now to Fig. 8, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) whose schematic cross-sectional diagram is illustrated in Fig. 7. Analogously with the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) whose schematic cross-sectional diagram is illustrated within Fig. 5 within the first preferred embodiment of the method of the present invention, there is shown within Fig. 8 the formation within the semiconductor substrate 30 of source/drain electrode high dose ion implant structures 44a' and 44b' through means of a dose of substantially orthogonal high dose implanting ions 46'. Analogously with the dose of Large Tilt Angle Implant (LATI) low dose implanting ions 42' within the second preferred embodiment of the method of the present invention, the dose of substantially orthogonal high dose implanting ions 46' within the second preferred embodiment of the method of the present invention may also be provided at an ion implantation energy somewhat higher than the ion implantation energy employed in forming the source/drain electrode high dose ion implant structures 44a and 44b within the first preferred embodiment of the method of the present invention. Thus, for the second preferred embodiment of the method of the present invention, the dose of substantially orthogonal high dose implanting ions 46' is preferably provided at an ion implantation dose of from about 1E15 to about 1E16 ions per square centimeter and an ion implantation energy of from about 50 to about 150 keV.

Referring now to Fig. 9, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the integrated circuit whose schematic cross-sectional diagram is illustrated in Fig. 8. Shown in Fig. 9 is the presence of the polysilicon spacers 39a and 39b which reside upon the insulator spacers 38a and 38b. The polysilicon spacers 39a and 39b, and the insulator spacers 38a and 38b, are formed from the corresponding blanket polysilicon layer 39 and blanket insulator layer 38. Methods and materials through which spacers may in general be formed from corresponding blanket layers within integrated circuits are known within the art of integrated circuit manufacture. Spacers are typically formed from corresponding blanket layers within integrated circuits through anisotropic Reactive Ion Etch (RIE) etching of those corresponding blanket layers employing a Reactive Ion Etch (RIE) etchant gas appropriate to the material from which is formed the corresponding blanket layer. For the second preferred embodiment of the method of the present invention, the polysilicon spacers 39a and 39b, and the insulator spacers 38a and 38b are preferably formed through such a Reactive Ion Etch (RIE) anisotropic etch method as applied to the blanket polysilicon layer 39 and the blanket insulator layer 38. In general, spacers within advanced integrated circuits assist in forming void free insulator layer upon integrated circuit structures adjoining which are formed those spacers. In particular, polysilicon spacers, such as polysilicon spacers 39a and 39b, additionally provide within advanced integrated circuits a structure through which charge carriers may be induced into a semiconductor substrate region adjoining but not immediately beneath a gate electrode within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

Upon forming the polysilicon spacers 39a and 39b, and the insulator spacers 38a and 38b, there is formed a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) through the second preferred embodiment of the method of the present invention. Analogously with the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) formed through the first preferred embodiment of the method of the present invention, the Metal Oxide Semiconductor Field Effect

Transistor (MOSFET) formed through the second preferred embodiment of the method of the present invention has formed therein a Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure. The Lightly Doped Drain (LDD) low dose ion implant structure and the source/drain electrode high dose ion implant structure may be formed in-situ without the need for forming through a sequential intermediate process step an insulator spacer adjoining the gate electrode edge of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which insulator spacer would otherwise conventionally be employed in defining the location of the Lightly Doped Drain (LDD) low dose ion implant structure with respect to the source/drain electrode high dose ion implant structure.

As is understood by a person skilled in the art, the preferred embodiments of the method of the present invention are illustrative of the method of the present invention rather than limiting of the method of the present invention. Revisions may be made to methods, materials, structures and dimensions through which is formed the Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping the source/drain electrode high dose ion implant structure within the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) formed through the preferred embodiments of the method of the present invention while still forming Lightly Doped Drain (LDD) low dose ion implant structures partially overlapping source/drain electrode high dose ion implant structures which are within the spirit and scope of the present invention as defined by the appended Claims. In particular, as is understood by a person skilled in the art, such revisions include but are not limited to the order in which the Lightly Doped Drain (LDD) low dose ion implant structure and the source/drain electrode high dose ion implant structure are provided in forming a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) through the method of the present invention. As is additionally understood by a person skilled in the art, such revisions also include but are not limited to the ordering with which the optional polysilicon layer is formed upon the Metal

Oxide Semiconductor Field Effect Transistor (MOSFET) with respect the formation of the Lightly Doped Drain (LDD) low dose ion implant structures and the source/drain electrode high dose ion implant structures within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) formed through the method of the present invention.

What is claimed is:

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1. A method for forming a Lightly Doped Drain (LDD) low dose ion implant structure within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) comprising:

forming upon a semiconductor substrate a gate dielectric layer upon which gate dielectric layer resides a gate electrode;

forming upon the exposed portions of the semiconductor substrate, the gate dielectric layer and the gate electrode an insulator layer; and

implanting through a Large Angle Tilt Implant (LATI) method a minimum of one low dose ion implant through the insulator layer and into the semiconductor substrate to form a Lightly Doped Drain (LDD) low dose ion implant structure within the semiconductor substrate including a portion of the semiconductor substrate beneath the gate electrode edges.

2. The method of Claim 1 wherein the width of the gate electrode is from about 1500 to about 5000 angstroms.

3. The method of Claim 1 wherein the insulator layer is a conformal insulator layer.

4. The method of Claim 1 wherein the insulator layer is from about 400 to about 1000 angstroms thick.

5. The method of Claim 1 wherein the low dose ion implant is provided at a tilt angle of from about 15 to about 45 degrees with respect to the orthogonal to the semiconductor substrate.

6. The method of Claim 1 wherein the low dose ion implant employs a dopant species

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chosen from the group of dopant species consisting of arsenic dopant species, boron dopant species and phosphorus dopant species.

7. The method of Claim 1 wherein the low dose ion implant is undertaken at an ion implant dose of from about 1E13 to about 1E14 ions per square centimeter and an ion implantation energy of from about 50 to about 150 keV.

8. A method for forming a Lightly Doped Drain (LDD) low dose ion implant structure partially overlapping a source/drain electrode high dose ion implant structure within a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) comprising:

forming upon a semiconductor substrate a gate dielectric layer upon which resides a gate electrode;

forming upon the exposed portions of the semiconductor substrate, the gate dielectric layer and the gate electrode an insulator layer;

implanting through a Large Angle Tilt Implant (LATI) method a minimum of one low dose ion implant through the insulator layer and into the semiconductor substrate to form a Lightly Doped Drain (LDD) low dose ion implant structure within the semiconductor substrate including a portion of the semiconductor substrate beneath the gate electrode edges; and

implanting substantially orthogonally to the semiconductor substrate a minimum of one high dose ion implant through the insulator layer and into the semiconductor substrate to form a source/drain electrode high dose ion implant structure adjoining but not beneath the gate electrode edges.

9. The method of Claim 8 wherein the width of the gate electrode is from about 1500

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to about 5000 angstroms.

10. The method of Claim 8 wherein the insulator layer is a conformal insulator layer.

11. The method of Claim 8 wherein the insulator layer is from about 400 to about 1000 angstroms thick.

12. The method of Claim 8 wherein the low dose ion implant is provided at a tilt angle of from about 15 to about 45 degrees with respect to the orthogonal to the semiconductor substrate.

13. The method of Claim 8 wherein the low dose ion implant employs a dopant species chosen from the group of dopant species consisting of arsenic dopant species, boron dopant species and phosphorus dopant species.

14. The method of Claim 8 wherein the low dose ion implant is undertaken at an ion implant dose of from about 1E13 to about 1E14 ions per square centimeter and an ion implantation energy of from about 50 to about 150 keV.

15. The method of Claim 8 wherein the high dose ion implant employs a dopant species of polarity equivalent to the polarity of the dopant species employed in the low dose ion implant, and the high dose ion implant employs a dopant species chosen from the group of dopant species consisting of arsenic dopant species, boron dopant species and phosphorus dopant species.

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16. The method of Claim 8 wherein the high dose ion implant is undertaken at an ion implant dose of from about 1E15 to about 1E16 ions per square centimeter and an ion implantation energy of from about 50 to about 150 keV.

17. The method of Claim 8 wherein the low dose ion implant is provided prior to the high dose ion implant.

18. The method of Claim 8 wherein the high dose ion implant is provided prior to the low dose ion implant.

19. The method of Claim 8 further comprising forming a polysilicon layer upon the insulator layer.

20. The method of Claim 19 wherein the polysilicon layer is from about 500 to about 1500 angstroms thick.

21. The method of Claim 8 further comprising anisotropically etching the insulator layer to form an insulator spacer after providing the low dose ion implant and the high dose ion implant through the insulator layer.

22. The method of Claim 19 further comprising sequentially anisotropically etching the polysilicon layer to form a polysilicon spacer and the insulator layer to form an insulator spacer after providing the low dose ion implant and the high dose ion implant through the insulator layer.

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