

METHOD OF CONTROLLING A SeOI DRAM MEMORY CELL HAVING A
SECOND CONTROL GATE BURIED UNDER THE INSULATING LAYER

ABSTRACT

The invention relates to a method of controlling a DRAM memory cell consisting of an FET transistor on a semiconductor-on-insulator substrate comprising a thin film (3) of semiconductor material separated from a base substrate (1) by an insulating layer (2, BOX), the transistor having a channel (4) and two control gates, a front control gate (8, 11) being arranged on top of the channel (4) and separated from the latter by a gate dielectric (7, 10) and a back control gate (9, 12, 13, 17, 18) being arranged in the base substrate and separated from the channel (4) by the insulating layer (BOX), characterized in that, in a cell programming operation, the front control gate and the back control gate are used jointly by applying a first voltage to the front control gate and a second voltage to the back control gate, said first voltage being lower in amplitude than the voltage needed to program the cell when no voltage is applied to the back control gate.

FIGURE 2