CLAIMS

1. An integrated circuit, comprising:

at least one photodetection region configured to generate charge carriers in response to receiving incident photons; and

at least one charge storage region configured to receive the charge carriers from the photodetection region,

wherein:

charge carriers stored in the at least one charge storage region indicate timing information and spectral information of the incident photons; and

the at least one charge storage region comprises first and second charge storage regions, charge carriers stored in the first charge storage region indicate the timing information, and charge carriers stored in the second charge storage region indicate the spectral information.

2. The integrated circuit of claim 1, wherein the timing information comprises luminescence lifetime information.

3. The integrated circuit of claim 1, wherein the spectral information comprises wavelength information.

4. The integrated circuit of claim 3, wherein the at least one photodetection region is configured to receive a first plurality of incident photons having first spectral characteristics and a second plurality of incident photons having second spectral characteristics, and the spectral information indicates a difference between the first and second spectral characteristics.

5. The integrated circuit of claim 4, wherein the spectral information indicates a difference between a wavelength of the first plurality of incident photons and a wavelength of the second plurality of incident photons.

6. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 600 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 600nm.

7. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 600 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 700nm.

8. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 700 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 700nm.

9. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 550 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 600nm.

10. The integrated circuit of claim 5, wherein the wavelength of the first plurality of incident photons is less than 550 nanometers (nm) and the wavelength of the second plurality of incident photons is greater than 550nm.

~~11. The integrated circuit of claim 1, wherein the at least one charge storage region comprises first and second charge storage regions, charge carriers stored in the first charge storage region indicate the timing information, and charge carriers stored in the second charge storage region indicate the spectral information.~~

~~12~~11. The integrated circuit of claim 1~~1~~, wherein the first and second charge storage regions have different depths in a first direction in which the at least one photodetection region is configured to receive the incident photons.

~~13~~12. The integrated circuit of claim ~~12~~11, wherein the at least one photodetection region comprises a photodetection region configured to generate and transfer the charge carriers to the first and second charge storage regions.

~~14~~13. The integrated circuit of claim ~~12~~11, wherein the at least one photodetection region comprises first and second photodetection regions configured to generate first and second charge carriers, respectively, and the first charge storage region is configured to receive the first charge carriers and the second charge storage region is configured to receive the second charge carriers.

~~15~~14. The integrated circuit of claim ~~12~~11, further comprising:

a first charge transfer region disposed between the at least one photodetection region and the first charge storage region; and

a second charge transfer region disposed between the at least one photodetection region and the second charge storage region,

wherein the first charge transfer region is positioned, at least in part, in the first direction, before or after the second charge transfer region.

~~16~~15. The integrated circuit of claim ~~15~~14, further comprising:

a third charge transfer region configured to receive the charge carriers from the at least one photodetection region,

wherein the third charge transfer region is positioned, at least in part, in the first direction, before or after the first and/or second charge transfer region(s).

~~17~~16. The integrated circuit of claim 1, further comprising a pixel comprising the at least one photodetection region and the at least one charge storage region, wherein the pixel is 10 microns by 10 microns or smaller.

~~18. An integrated circuit, comprising:~~

~~a first photodetection region configured to generate first charge carriers in response to receiving incident photons in a first direction, the first photodetection region having a first depth in the first direction;~~

~~a second photodetection region having a second depth in the first direction that is different from the first depth, the second photodetection region configured to generate second charge carriers in response to receiving incident photons in the first direction; and~~

~~a charge storage region configured to receive the first and/or second charge carriers from the first and/or second photodetection region.~~

~~19. The integrated circuit of claim 18, further comprising a transfer gate configured to control a transfer of the first and/or second charge carriers from the first photodetection region to the charge storage region.~~

~~20. The integrated circuit of claim 18, further comprising a second charge storage region configured to receive the second charge carriers from the second photodetection region, wherein the charge storage region is a first charge storage region~~

21. The integrated circuit of claim 20, further comprising a first transfer gate configured to control a transfer of the first charge carriers to the first charge storage region and a second transfer gate configured to control a transfer of the second charge carriers to the second charge storage region.

22. The integrated circuit of any one of claims 18 to 21, wherein the first charge carriers indicate lifetime information of the incident photons, and the second charge carriers indicate spectral information of the incident photons.

23. The integrated circuit of claim 22, wherein the spectral information comprises wavelength information.

24. A system comprising the integrated circuit of claim 23 and at least one processor, the at least one processor configured to:

detect a first number of charge carriers stored in the first charge storage region;

detect a second number of charge carriers stored in the second charge storage region; and

combine the first number and second numbers to determine the lifetime information and/or the spectral information.

25. The system of claim 24, wherein the at least one processor is configured to add and/or subtract the first and/or second numbers to determine the lifetime information and/or the spectral information.

26. An integrated circuit, comprising:

a photodetection region configured to generate first charge carriers in response to receiving incident photons in a first direction;

a first charge storage region having a first depth in the first direction and configured to receive the first charge carriers; and

a second charge storage region having a second depth in the first direction that is different from the first depth, the second charge storage region configured to generate second charge carriers in response to receiving incident photons in the first direction.

27. The integrated circuit of claim 26, further comprising a transfer gate configured to control a transfer of the first charge carriers from the photodetection region to the first charge storage region.

~~28. The integrated circuit of claim 27, wherein the first charge carriers indicate lifetime information of the incident photons, and the second charge carriers indicate spectral information of the incident photons.~~

~~29. The integrated circuit of claim 28, wherein the spectral information comprises wavelength information.~~

~~30. A system comprising the integrated circuit of claim 29 and at least one processor, the at least one processor configured to:~~

~~detect a first number of charge carriers stored in the first charge storage region;~~

~~detect a second number of charge carriers stored in the second charge storage region; and~~

~~combine the first number and second numbers to determine the lifetime information and/or the spectral information.~~

~~31. The system of claim 30, wherein the at least one processor is configured to add and/or subtract the first and/or second numbers to determine the lifetime information and/or the spectral information.~~

~~32~~17. An integrated circuit, comprising:

at least one photodetection region configured to generate first charge carriers in response to receiving incident photons in a first direction;

at least one charge storage region configured to receive the first charge carriers from the at least one photodetection region and positioned at a first depth in the first direction; and

a region positioned at a second depth in the first direction and configured to generate second charge carriers responsive to the incident photons,

wherein the first charge carriers indicate lifetime information of the incident photons, and the second charge carriers indicate spectral information of the incident photons.

~~33~~18. The integrated circuit of claim ~~32~~17, wherein the at least one photodetection region comprises:

a first photodetection region configured to transfer the first charge carriers to a first charge storage region of the at least one charge storage region; and

a second photodetection region comprising the region positioned at the second depth in the first direction, wherein the second photodetection region is configured to transfer the second charge carriers to a second charge storage region of the at least one charge storage region.

~~34~~19. The integrated circuit of claim ~~33~~18, further comprising:

a first transfer gate configured to bias a first transfer channel between the first photodetection region and the first charge storage region; and

a second transfer gate configured to bias a second transfer channel between the second photodetection region and the second charge storage region.

~~35~~20. The integrated circuit of claim ~~32~~17, wherein the at least one charge storage region comprises:

a first charge storage region configured to receive the first charge carriers from the at least one photodetection region and positioned at the first depth in the first direction; and

a second charge storage region comprising the region positioned at the second depth in the first direction, wherein the second charge storage region is configured to generate and store the second charge carriers responsive to the incident photons.

~~36~~21. The integrated circuit of claim ~~35~~20, wherein:

the second depth is positioned after the first depth in the first direction; and

the second charge storage region is configured to receive the incident photons.

~~37~~22. The integrated circuit of claim ~~32~~17, wherein the integrated circuit further comprises a first transfer gate configured to bias a first transfer channel electrically coupling the at least one photodetection region to the first charge storage region.

~~38~~23. The integrated circuit of claim ~~37~~22, further comprising:

a third charge storage region configured to receive the charge carriers and positioned at a third depth that is before the second depth in the first direction; and

a second transfer gate configured to bias a second transfer channel electrically coupling the at least one photodetection region.

~~39~~24. The integrated circuit of claim ~~38~~23, wherein the second charge storage region is disposed, at least in part, between the at least one photodetection region and the third charge storage region.

~~40. The integrated circuit of claim 32, wherein the first charge carriers indicate lifetime information of the incident photons, and the second charge carriers indicate spectral information of the incident photons.~~

~~41~~25. The integrated circuit of claim ~~40~~32, wherein the spectral information comprises wavelength information.

~~42~~26. A method of operating the integrated circuit of any one of claim~~s 40~~ 1 to 25, the method comprising:

detecting, using at least one processor, a first number of charge carriers stored in the first charge storage region;

detecting, using the at least one processor, a second number of charge carriers stored in the second charge storage region; and

combining, using the at least one processor, the first number and second numbers to determine the lifetime or timing information and/or the spectral information.

~~43~~27. The method of claim ~~42~~26, wherein the act of combining includes adding and/or subtracting by the at least one processor.

~~44. An integrated circuit, comprising:~~

~~first and second charge storage regions; and~~

~~an optical sorting element configured to direct at least a first plurality of incident photons toward the first charge storage region and at least a second plurality of incident photons toward the second charge storage region,~~

~~wherein charge carriers generated in the first and/or second charge storage regions indicate timing information and spectral information.~~

~~45. The integrated circuit of claim 44, wherein the optical sorting element comprises an at least partially refractive element.~~

~~46. The integrated circuit of claim 45, wherein the at least partially refractive element comprises at least one member of a group comprising:~~

~~a micro-disk;~~

~~a micro-lens; and~~

~~a prism;~~

~~47. The integrated circuit of claim 44, wherein the optical sorting element comprises an at least partially diffractive element.~~

~~48. The integrated circuit of claim 47, wherein the at least partially diffractive element comprises at least one member from a group comprising:~~

~~a linear grating element;~~

~~a curved grating element;~~

~~a zone plate; and~~

~~a photonic crystal.~~

~~49. The integrated circuit of claim 44, wherein the optical sorting element comprises at least partially scattering element.~~

~~50. The integrated circuit of claim 49, wherein the at least partially scattering element comprises a plurality of elements having different refractive indices.~~

~~51. The integrated circuit of claim 44, wherein the first and second pluralities of incident photons are incident in a first direction, and wherein the optical sorting element comprises a plurality of openings at a surface that faces a second direction opposite the first direction.~~

~~52. The integrated circuit of claim 44, wherein the optical sorting element comprises a plasmonic element.~~

~~53. The integrated circuit of claim 52, wherein the plasmonic element comprises at least one member of a group comprising:~~

~~a plurality of nano-holes; and~~

~~an extraordinary optical transmission element.~~

~~54. The integrated circuit of claim 44, wherein the first charge carrier storage region is configured to generate and store first charge carriers responsive to the first plurality of the incident photons, and the second charge carrier storage region is configured to generate and store second charge carriers responsive to the second plurality of the incident photons.~~

~~55. The integrated circuit of claim 54, wherein the first charge carriers indicate lifetime information of the first plurality of the incident photons, and the second charge carriers indicate spectral information of the second plurality of the incident photons.~~

~~56. The integrated circuit of claim 55, wherein the spectral information comprises wavelength information.~~

~~57. The integrated circuit of claim 44, further comprising:~~

~~at least one photodetection region;~~

~~a first transfer gate configured to bias a first transfer channel between the at least one photodetection region and the first charge storage region; and~~

~~a second transfer gate configured to bias a second transfer channel between the at least one photodetection region and the second charge storage region.~~

~~58. The integrated circuit of claim 57, wherein the at least one photodetection region comprises:~~

~~a first photodetection region configured to transfer the charge carriers to the first charge storage region; and~~

~~a second photodetection region configured to transfer the charge carriers to the second charge storage region,~~

~~wherein the optical sorting element is configured to direct the first plurality of the incident photons towards the first photodetection region and direct the second plurality of the incident photons towards the second photodetection region.~~

28. A system, comprising:

the integrated circuit of any one of claims 1 to 25; and

a control circuit configured to provide control signals to transfer gates of the integrated circuit to control time-gating of charge carriers from the at least one photodetection region to the at least one charge storage region.