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TITLE



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**STRAINED-CHANNEL TRANSISTOR STRUCTURE WITH LATTICE-
MISMATCHED ZONE AND FABRICATION METHOD THEREOF**

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor device with lattice-mismatched zone and fabrication method thereof, and more specifically to a strained-channel transistor structure and fabrication method thereof.

Description of the Related Art

Size reduction of the metal-oxide-semiconductor field-effect transistor (MOSFET), including reduction of gate length and gate oxide thickness, has enabled a continuous improvement in speed performance, density, and cost per unit function of integrated circuits during the past few decades.

In order to further enhance performance of the transistor, strain may be introduced in the transistor channel to improve carrier mobility to enhance performance of the transistor in addition to device scaling. There are several existing approaches to introducing strain in a channel region of the transistor.

In one conventional approach, as described in a paper titled "NMOS and PMOS transistors fabricated in strained silicon/relaxed silicon-germanium structures", disclosed by J. Welser *et al.*, published at the December 1992 International Electron Devices Meeting held in San Francisco, CA, pp. 1000-1002, a relaxed silicon germanium (SiGe) buffer layer 110 is provided beneath channel region 126, as shown in Fig. 1A. In Fig. 1B and Fig. 1C, a simple model of different lattice constants is used to show the intersection between relaxed SiGe layer 114 of buffer layer 110 and strained-Si layer 130. In Fig. 1B, model 135 shows the natural lattice constant of Si, smaller than that of SiGe shown by model 115. In Fig. 1C, when a thin layer of epitaxial Si (model 135) is grown on relaxed SiGe layer 114 (model 115), unit cell 136 of Si shown in model 135 is stretched laterally so as to be under a biaxial tensile strain. The thin layer of epitaxial Si becomes strain-Si layer 130 shown in Fig. 1A. In Fig. 1A, a transistor formed on the epitaxial strained-Si layer 130 is therefore with a channel region 126 under the biaxial tensile strain. In this approach, relaxed SiGe layer 114 is a stressor that introduces strain in channel region 126. The stressor, in this case, is placed below channel region 126. Significant mobility enhancement has been reported for both electrons and holes in bulk transistors using a silicon channel under biaxial tensile strain. In the aforementioned approach, the epitaxial silicon layer 130 is strained before forming the transistor. Therefore, there are some concerns about possible strain relaxation in the subsequent high

temperature CMOS processes. Further, the approach is very expensive since SiGe buffer layer 110 with thickness in the order of micrometers has to be grown. Numerous dislocations exist in relaxed SiGe layer 114, some of which propagate to strained-Si layer 130, resulting in high defect density, thereby negatively affecting transistor performance.

In another approach, strain in a channel region is introduced after a transistor is formed. In this approach, a high stress film 220 is formed over a completed transistor structure 250, as shown in Fig. 2. High stress film 220, being a stressor, exerts significant influence on channel region 206, modifying silicon lattice spacing in channel region 206, and thus introducing strain in channel region 206. In this case, the stressor is placed above completed transistor structure 250, described in detail in a paper disclosed by A. Shimizu et al., entitled "Local mechanical stress control (LMC): a new technique for CMOS performance enhancement", published in pp. 433-436 of the *Digest of Technical Papers* of the 2001 International Electron Device Meeting. The strain contributed by high stress film 220 is believed to be uniaxial in nature with a direction parallel to a source-to-drain direction. However, uniaxial tensile strain in the source-to-drain degrades hole mobility while uniaxial compressive strain degrades electron mobility. Ion implantation of germanium can be used to selectively relax the strain so that the hole or electron mobility is not degraded, but can be difficult to implement due to the close proximity of the N and P-channel transistors.

SUMMARY OF THE INVENTION

Thus, the main object of the present invention is to provide a transistor structure with a strained channel region.

Another object of the present invention is to provide a strained-channel transistor structure where portions of one or both of a source region and drain region adjacent to a strained channel region are lattice mismatched with respect to the channel region.

Another object of the present invention is to provide a fabrication method of a strained-channel transistor structure.

In order to achieve the above objects, the present invention provides a strained-channel transistor structure comprising a strained channel region, a gate dielectric layer, a gate electrode, and a source region and drain region. The substrate comprises a first semiconductor material with a first natural lattice constant. The gate dielectric layer is on the strained channel region. The gate electrode is on the gate dielectric layer. The source region and drain region are oppositely adjacent to the strained channel region. One or both of the source region

and drain region comprise a lattice-mismatched zone comprising a second semiconductor material with a second natural lattice constant different from the first natural lattice constant.

5 The present invention further provides a fabrication method of a strained-channel transistor structure. First, a substrate having a channel region, comprising a first semiconductor material with a first natural lattice constant, in a surface, a gate dielectric on the channel
10 region, and a gate electrode on the gate dielectric layer is provided. Then, a first source region and drain region are formed oppositely adjacent to the channel region. Next, a spacer is formed on a sidewall of the gate electrode, covering a part of the surface of the substrate.
15 Next, the surface of the substrate not covered by the spacer and gate electrode is recessed. Further, the recess is filled with a second semiconductor material with a second natural lattice constant different from the first natural lattice constant as a lattice-mismatched zone
20 straining the channel region. Finally, a second source region is formed adjacent to the first source region and a second drain region is formed adjacent to the first drain region, one or both of the second source region and second drain region comprising the lattice-mismatched zone.

25 The present invention further provides a fabrication method of a strained-channel transistor structure. First, a substrate having a channel region, comprising a first semiconductor material with a first natural lattice constant, in a surface, a gate dielectric on the channel
30 region, a gate electrode on the gate dielectric layer, a source region and drain region oppositely adjacent to the channel region, and a spacer on a sidewall of the gate electrode, covering a part of the surface of the substrate, is provided. Then, one or both of the source region and
35 drain region is recessed. Finally, the recess is filled with a second semiconductor material with a second natural lattice constant different from the first natural lattice constant as a lattice-mismatched zone straining the channel region.

40 The present invention further provides a fabrication method of a strained-channel transistor structure. First, a substrate having a channel region, comprising a first semiconductor material with a first natural lattice constant, in a surface, a gate dielectric on the channel
45 region, a gate electrode on the gate dielectric layer, and a spacer on a sidewall of the gate electrode, covering a part of the surface of the substrate, is provided. Then, the surface of the substrate not covered by the spacer and gate dielectric layer is recessed to form a recess.
50 Finally, a source region and drain region are formed oppositely adjacent to the channel region, one or both of the source region and drain region comprising the lattice-mismatched zone.

The present invention further provides a fabrication method of a strained-channel transistor structure. First, a substrate having a channel region, comprising a semiconductor material, in a surface, a gate dielectric on the channel region, a gate electrode on the gate dielectric layer, a source region and drain region oppositely adjacent to the channel region, and a spacer on a sidewall of the gate electrode, covering a part of the surface of the substrate, is provided. Finally, an element with an atomic size different from that of the semiconductor material is implanted to form a lattice-mismatched zone in one or both of the source region and drain region straining the channel region.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description in conjunction with the examples with references made to the accompanying drawings, wherein:

Figs. 1A through 1C are cross sections illustrating a conventional strained silicon transistor with a relaxed SiGe layer as a stressor to induce strain in the top epitaxial strained silicon layer.

Fig. 2 is a cross section illustrating another conventional strained silicon transistor introducing strain in the channel using a high stress film as a stressor.

Fig. 3A and Fig. 3B are cross sections illustrating strained-channel transistor structures in accordance with the first embodiment of the present invention.

Figs. 4A through 4B are cross sections illustrating strained-channel transistor structures in accordance with the second embodiment of the present invention.

Fig. 5 is a flowchart illustrating, in detail, the fabrication method of a strained-channel transistor structure in accordance with the third embodiment of the present invention.

Figs. 6A through 6F are cross sections illustrating steps of the fabrication method of a strained-channel transistor structure in accordance with the third embodiment of the present invention.

Fig. 7 is a flowchart illustrating, in detail, the fabrication method of a strained-channel transistor structure in accordance with the fourth embodiment of the present invention.

Figs. 8A through 8D are cross sections illustrating steps of the fabrication method of a strained-channel transistor structure in accordance with the fourth embodiment of the present invention.

Fig. 9 is a flowchart illustrating, in detail, the fabrication method of a strained-channel transistor structure in accordance with the fifth embodiment of the present invention.

Figs. 10A through 10G are cross sections illustrating steps of the fabrication method of a strained-channel transistor structure in accordance with the fifth embodiment of the present invention.

Figs. 11A through 11D are cross sections illustrating steps of the fabrication method of a strained-channel transistor structure in accordance with the sixth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The following embodiments are intended to illustrate the invention more fully without limiting their scope, since numerous modifications and variations will be apparent to those skilled in this art.

First Embodiment

In the first embodiment of the present invention, two kinds of stress modes exerted on the strained-channel region according to the present invention are discussed.

In Fig. 3A, a cross section of a strained-channel transistor structure 3a in accordance with the first embodiment of the present invention is shown. Substrate 300a, having a strained channel region 306a in a surface, comprises a semiconductor material. Gate dielectric layer 312a, preferably with a thickness between about 3 and 100 Å, is on the strained channel region 306a. Gate electrode 314a is on the gate dielectric layer 312a. Spacer 316a is on a sidewall of gate electrode 314a and covers a part of the surface of substrate 300a. Drain region 307a, comprising drain extension region 301a and deeper drain region 302a, and source region 308a, comprising source extension region 303a and deeper source region 304a, are oppositely adjacent to strained channel region 306a. Lattice-mismatched zone 305a, comprising another semiconductor material with a natural lattice constant different from that of substrate 300a, may be in one or both of the deeper drain region 302a and deeper source region 304a. Strained channel region 306a is therefore strained by the different lattice constants of strained channel region 306a and lattice-mismatched zone 305a.

In strained-channel transistor structure 3a in accordance with the first embodiment of the present invention, substrate 300a preferably comprises silicon, with a natural lattice constant of approximately 5.431 Å, and lattice-mismatched zone 305a preferably comprises an alloy semiconductor material such as a silicon-germanium alloy, with a natural lattice constant between about 5.431 Å to 5.657 Å depending on concentration of germanium in the silicon-germanium alloy, larger than that of substrate 300a. Molar fraction of germanium in the silicon-germanium alloy of lattice-mismatched zone 305a in accordance with the first embodiment of the present invention is preferably between about 0.1 and 0.9. Therefore, lattice-mismatched zone 305a as a stressor exerts a compressive stress C_1 in a

source-to-drain direction and tensile stress T_1 in a vertical direction on the strained channel region 306a, resulting in strained channel region 306a under a compressive strain in the source-to-drain direction and tensile strain in the vertical direction. Hole mobility in the strained channel region 306a is significantly enhanced, enhancing drive current when strained-channel transistor structure 3a in accordance with the first embodiment of the present invention is a P-channel transistor structure.

In Fig. 3B, a cross section of a strained-channel transistor structure 3b in accordance with the first embodiment of the present invention is shown. Substrate 300b, having a strained channel region 306b in a surface, comprises a semiconductor material. Gate dielectric layer 312b, preferably with a thickness between about 3 and 100 Å, is on the strained channel region 306b. Gate electrode 314b is on the gate dielectric layer 312b. Spacer 316b is on a sidewall of gate electrode 314b and covers a part of the surface of substrate 300b. Drain region 307b, comprising drain extension region 301b and deeper drain region 302b, and source region 308b, comprising source extension region 303b and deeper source region 304b, are oppositely adjacent to strained channel region 306b. Lattice-mismatched zone 305b, comprising another semiconductor material with a natural lattice constant different from that of substrate 300b, may be in one or both of the deeper drain region 302b and deeper source region 304b. Strained channel region 306b is therefore strained by the difference lattice constants of strained channel region 306b and lattice-mismatched zone 305b.

In strained-channel transistor structure 3b in accordance with the first embodiment of the present invention, substrate 300b preferably comprises silicon and lattice-mismatched zone 305b preferably comprises an alloy semiconductor material such as a silicon-carbon alloy, with a natural lattice constant smaller than that of substrate 300a. Molar fraction of carbon in the silicon-carbon alloy of lattice-mismatched zone 305b in accordance with the first embodiment of the present invention is preferably between about 0.01 and 0.04. Therefore, lattice-mismatched zone 305b as a stressor exerts a tensile stress T_2 in a source-to-drain direction and compressive stress C_2 in a vertical direction on the strained channel region 306b, resulting in strained channel region 306b under a tensile strain in the source-to-drain direction and compressive strain in the vertical direction. Electron mobility in the strained channel region 306b is significantly enhanced, enhancing drive current when strained-channel transistor structure 3b in accordance with the first embodiment of the present invention is an N-channel transistor structure. Furthermore, lattice-mismatched zone 305b may further comprise germanium as a silicon-germanium-carbon alloy, in

which molar fraction of carbon is more than a tenth of that of germanium.

Further, compressive strain and tensile strain of strained channel region 306a in Fig. 3A and strained channel region 306b in Fig. 3B are about 0.1% to 4%, preferably about 1% to 4%. Both lattice-mismatched zone 305a in Fig. 3A and lattice-mismatched zone 305b in Fig. 3B are about 10 Å and 1000 Å thick. Compressive strain and tensile strain of strained channel region 306a in Fig. 3A and strained channel region 306b in Fig. 3B are dependent on lattice constants of lattice-mismatched zones 306a and 306b, thicknesses of lattice-mismatched zones 306a and 306b, and arrangement of lattice-mismatched zone 306a in drain region 307a and/or source region 308a, and lattice-mismatched zone 306b in drain region 307b and/or source region 308b.

Second Embodiment

In the second embodiment of the present invention, different kinds of arrangements of lattice-mismatched zone in drain region and/or source region according to the present invention are discussed. In strained-channel transistor structures 4a through 4d in Figs. 4A through 4D, relationships among substrate 400, drain extension region 401, deeper drain region 402, drain region 407, source extension region 403, deeper source region 404, source region 408, lattice-mismatched zone 405a/405b/405c/405d, strained channel region 406a/406b/406c/406d, gate dielectric layer 412, gate electrode 414, and spacer 416, the same as those described in the first embodiment of the present invention, are omitted.

In Fig. 4A, lattice-mismatched zone 405a is arranged near the surface of drain region 407 and/or source region 408, and does not extend into drain extension region 401 and/or source extension region 403. In Fig. 4B, lattice-mismatched zone 405b may protrude from the surface of drain region 407 and/or source region 408, forming a raised drain region 407b and raised source region 408b. In Fig. 4C, lattice-mismatched zone 405c is arranged near the surface of drain region 407 and/or source region 408, and may further extend into drain extension region 401 and/or source extension region 403. In Fig. 4D, lattice-mismatched zone 405d is arranged more deeply from the surface of drain region 407 and/or source region 408, and may further extend into strained channel region 406d beneath drain extension region 401 and/or source extension region 403. Note that the arrangements of lattice-mismatched zone in drain region and/or source region in accordance with the first embodiment of the present invention are not meant to be restrictive. Those skilled in the art may further adjust the arrangement of lattice-mismatched zone according to the present invention when required.

In Figs. 4A through 4D, a conductive layer 420 such as silicon, metal, metal silicide, or combinations thereof is optionally formed on the surface of drain region 407 and/or source region 408 of strained-channel transistor structures 4a, 4c, and 4d, and raised drain region 407b and/or raised source region 408b of strained-channel transistor structure 4b.

Moreover, enhancement of either electron or hole mobility in strained-channel structure 4c in Fig. 4C is further improved because lattice-mismatched zone 405c is closer to strained channel region 406c, resulting in lattice-mismatched zone 405c exerting more strain on strained channel region 406c.

Third Embodiment

In the third embodiment of the present invention, a fabrication method of a strained-channel transistor structure according to the present invention is described. A flowchart of the fabrication method in accordance with the third embodiment of the present invention is shown in Fig. 5. The subsequent descriptions of the fabrication method in accordance with the third embodiment of the present invention follow the steps in Fig. 5.

In Fig. 6A, a semiconductor substrate such as a silicon substrate 500 is provided. Silicon substrate 500 comprises a previously formed plurality of isolation regions (not shown) and previously defined plurality of device regions (not shown). For example, the isolation regions may be shallow trench isolation regions. Figs. 6A through 6F provide a cross-sectional view of one single device region for easy description. Silicon substrate 500 comprises a channel region 506 in an active surface. Silicon substrate 500 is N-type doped when strained-channel transistor structure 5 in Fig. 6E is a P-channel transistor structure, or P-type doped when strained-channel transistor structure 5 in Fig. 6E is an N-channel transistor structure.

In Fig. 6B, a gate dielectric layer 512 is formed on the channel region 506, and then a gate electrode 514 is formed on the gate dielectric layer 512. Gate dielectric layer 512 is formed by thermal oxidation, thermal oxidation followed by nitridation, chemical vapor deposition, physical vapor deposition such as sputtering, or other known techniques to form a gate dielectric layer. Gate dielectric layer 512 can be silicon dioxide, silicon oxynitride, or combinations thereof with a thickness between about 3 Å to 100 Å, preferably approximately 10 Å or less. Gate dielectric layer 512 may be a high permittivity (high-k) material such as aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), hafnium oxynitride (HfON), hafnium silicate (HfSiO_4), zirconium silicate (ZrSiO_4), lanthanum oxide (La_2O_3), or combinations thereof with an equivalent oxide thickness between about 3 Å to 100 Å. Gate electrode 514 is

polycrystalline-silicon (poly-Si), poly-crystalline silicon-germanium (poly-SiGe), refractory metal such as molybdenum or tungsten, compounds such as titanium nitride, combinations thereof or other conductive material(s).
5 Implants known as workfunction implants may be introduced in gate electrode 514 to alter the workfunction thereof. Gate electrode 514 is formed by depositing a gate electrode material layer (not shown) over substrate 500, depositing a gate mask (not shown) over the gate electrode material layer,
10 patterning the gate mask to define gate electrode 514, etching the gate electrode material layer to form gate electrode 514, and removing the gate mask. Gate electrode 514 is electrically isolated from channel region 506 by gate dielectric layer 512. Gate dielectric layer 512 is preferably silicon oxynitride and gate electrode 514 is preferably poly-silicon etched using chlorine and bromine chemistry with a high etch selectivity with respect to gate dielectric later 514 in accordance with the third embodiment of the present invention.

20 In Fig. 6C, a drain extension region 501 and source extension region 503 are formed oppositely adjacent to channel region 506 in the active surface of substrate 500, and spacer 516 is formed on a sidewall of gate electrode 514, covering a part of drain extension region 501 and
25 source extension region 503. The drain extension region 501 and source extension region 503 are formed by ion implantation, plasma immersion ion implantation (PIII), or other known techniques. Spacer 516 is preferably formed by depositing a spacer material layer (not shown) such as silicon nitride or silicon dioxide, and selectively etching the spacer material layer. Spacer 516 is silicon nitride in accordance with the third embodiment of the present invention.

35 In Fig. 6D, a part or all of the active surface of substrate 500 not covered by gate dielectric layer 512 and spacer 516 is recessed to form at least one recess 509 with a depth d by plasma etching using chlorine and bromine chemistry. The depth d of recess 509 is about 50 Å to 1000 Å. An optional anneal may be performed to facilitate
40 silicon migration to repair etch damage caused by etching recess 509 to smooth the surface of recess 509 for a subsequent epitaxy process.

50 In Fig. 6E, recess 509 is filled with a semiconductor material such as silicon-germanium alloy or silicon-carbon alloy to form a lattice-mismatched zone 505, and then a deeper drain region 502 is formed adjacent to the drain extension region 501 and a deeper source region 503 is formed adjacent to the source extension region 502. Deeper drain region 502 combines with drain extension region 501 to form a drain region 507, and deeper source region 504 combines with source extension region 503 to form a source region 508. One or both of the drain region 507 and source region 508 comprise the lattice-mismatched zone 505.

Channel region 506 is strained to be a strained channel region 506' when lattice-mismatched zone 505 is formed. Thus, strained-channel transistor structure 5 in accordance with the third embodiment of the present invention is basically formed. Lattice-mismatched zone 505 is formed using an epitaxy process such as chemical vapor deposition, ultra-high vacuum chemical vapor deposition, or molecular beam epitaxy. Lattice-mismatched zone 505 comprises silicon-germanium alloy where molar fraction of germanium is about 0.1 to 0.9 when strained-channel transistor structure 5 is a P-channel transistor structure. When strained-channel transistor structure 5 is an N-channel transistor structure, lattice-mismatched zone 505 comprises silicon-carbon alloy where molar fraction of carbon is between about 0.01 and 0.04, and may further comprise germanium to be silicon-carbon-germanium alloy where molar fraction of germanium is less than ten times that of carbon. A silicon cap 522 is optionally formed on lattice-mismatched zone 505 using an epitaxy process such as chemical vapor deposition, ultra-high vacuum chemical vapor deposition, or molecular beam epitaxy. Lattice-mismatched zone 505 and optional silicon cap 522 may be in-situ doped or undoped during the epitaxy process. When lattice-mismatched zone 505 and optional silicon cap 522 are undoped during the epitaxy process, they will be subsequently doped, with dopants activated using a rapid thermal annealing process. Deeper drain region 502 and deeper source region 504 are formed using ion implantation, PIII, gas or solid source diffusion, or other known techniques. An annealing step is further added to recover implant damage or amorphization during formation of lattice-mismatched zone 505, silicon cap 522, deeper drain region 502, and deeper source region 504.

In Fig. 6F, a conductive layer 520 is optionally formed on lattice-mismatched zone 505 and/or drain region 507/source region 508 to reduce resistances of drain region 507 and source region 508. Conductive layer 520 is formed using self-aligned silicide, or other metal deposition process. Passivation layers and device contacts are subsequently formed so as to finish a device comprising strained-channel transistor structure 5 in accordance with the third embodiment of the present invention.

Fourth Embodiment

In the fourth embodiment of the present invention, a fabrication method of a strained-channel transistor structure where lattice-mismatched zone does not extend into drain extension region and/or source extension region according to the present invention is described. A flowchart of the fabrication method in accordance with the third embodiment of the present invention is shown in Fig. 7. The subsequent descriptions of the fabrication method in accordance with the third embodiment of the present invention follow the steps in Fig. 7.

In Fig. 8A, a semiconductor substrate such as a silicon substrate 600 is provided. Silicon substrate 600 comprises a previously formed plurality of isolation regions (not shown) and previously defined plurality of device regions (not shown). For example, the isolation regions may be shallow trench isolation regions. Figs. 8A through 8D provide a cross-sectional view of one single device region for easy description. Silicon substrate 600 comprises a conventional transistor structure comprising a channel region 606 in an active surface of substrate 600, a gate dielectric layer 612 on channel region 606, a gate electrode 614 on gate dielectric layer 612, a source region 608 and drain region 607 oppositely adjacent to channel region 606, and a spacer 616 on a sidewall of gate electrode 614, covering a part of the active surface of substrate 600. Drain region 607 comprises a drain extension region 601 and a deeper drain region 602, and source region 608 comprises a source extension region 603 and a deeper source region 604. Silicon substrate 600 is N-type doped when strained-channel transistor structure 6 in Fig. 8C is a P-channel transistor structure, or P-type doped when strained-channel transistor structure 6 in Fig. 8C is an N-channel transistor structure.

In Fig. 8B, a part or all of the active surface of substrate 600 not covered by gate dielectric layer 612 and spacer 616 is recessed to form at least one recess 609 with a depth d by plasma etching using chlorine and bromine chemistry. The depth d of recess 609 is about 50 Å to 1000 Å. An optional anneal may be performed to facilitate silicon migration to repair etch damage caused by etching recess 606 to smooth the surface of recess 609 for a subsequent epitaxy process.

In Fig. 8C, recess 609 is filled with a semiconductor material such as silicon-germanium alloy or silicon-carbon alloy to form a lattice-mismatched zone 605. One or both of the drain region 607 and source region 608 comprise the lattice-mismatched zone 605. Channel region 606 is strained to be a strained channel region 606' when lattice-mismatched zone 605 is formed. Thus, strained-channel transistor structure 6 in accordance with the fourth embodiment of the present invention is basically formed. Lattice-mismatched zone 605 may protrude from the surface of drain region 607 and/or source region 608, forming a raised drain region and raised source region. Lattice-mismatched zone 605 is formed using an epitaxy process such as chemical vapor deposition, ultra-high vacuum chemical vapor deposition, or molecular beam epitaxy. Lattice-mismatched zone 605 comprises silicon-germanium alloy where molar fraction of germanium is about 0.1 to 0.9 when strained-channel transistor structure 6 is a P-channel transistor structure. When strained-channel transistor structure 6 is an N-channel transistor structure, lattice-mismatched zone 605 comprises silicon-carbon alloy where

molar fraction of carbon is between about 0.01 and 0.04, and may further comprise germanium to be silicon-carbon-germanium alloy where molar fraction of germanium is less than ten times that of carbon. A silicon cap 622 is optionally formed on lattice-mismatched zone 605 using an epitaxy process such as chemical vapor deposition, ultra-high vacuum chemical vapor deposition, or molecular beam epitaxy. Lattice-mismatched zone 605 and optional silicon cap 622 are in-situ doped during the epitaxy process.

In Fig. 8D, a conductive layer 620 is optionally formed on lattice-mismatched zone 605 and/or drain region 607/source region 608 to reduce resistances of drain region 607 and source region 608. Conductive layer 620 is formed using self-aligned silicide, or other metal deposition process. Passivation layers and device contacts are subsequently formed so as to finish a device comprising strained-channel transistor structure 6 in accordance with the third embodiment of the present invention.

Fifth Embodiment

In the fifth embodiment of the present invention, a fabrication method of a strained-channel transistor structure where lattice-mismatched zone extends into drain extension region and/or source extension region according to the present invention is described. A flowchart of the fabrication method in accordance with the third embodiment of the present invention is shown in Fig. 9. The subsequent descriptions of the fabrication method in accordance with the third embodiment of the present invention follow the steps in Fig. 9.

In Fig. 10A, a semiconductor substrate such as a silicon substrate 700 is provided. Silicon substrate 700 comprises a previously formed plurality of isolation regions (not shown) and previously defined plurality of device regions (not shown). For example, the isolation regions may be shallow trench isolation regions. Figs. 10A through 10G provide a cross-sectional view of one single device region for easy description. Silicon substrate 700 comprises a channel region 706 in an active surface. Silicon substrate 700 is N-type doped when strained-channel transistor structure 7 in Fig. 10D is a P-channel transistor structure, or P-type doped when strained-channel transistor structure 7 in Fig. 10D is an N-channel transistor structure.

In Fig. 10B, first, a gate dielectric layer 712 is formed on the channel region 706, and a gate electrode 714 is formed on the gate dielectric layer 712. Finally, spacer 715 is formed on a sidewall of gate electrode 714, covering a part of the active surface of substrate 700. Gate dielectric layer 712 is formed by thermal oxidation, thermal oxidation followed by nitridation, chemical vapor deposition, physical vapor deposition such as sputtering, or other known techniques to form a gate dielectric layer. Gate dielectric layer 712 is preferably silicon dioxide,

silicon oxynitride, or combinations thereof with a thickness between about 3 Å to 100 Å, preferably approximately 10 Å or less. Gate dielectric layer 712 may be a high permittivity (high-k) material such as aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), hafnium oxynitride (HfON), hafnium silicate (HfSiO_4), zirconium silicate (ZrSiO_4), lanthanum oxide (La_2O_3), or combinations thereof with an equivalent oxide thickness between about 3 Å to 100 Å. Gate electrode 714 is polycrystalline-silicon (poly-Si), poly-crystalline silicon-germanium (poly-SiGe), refractory metal such as molybdenum or tungsten, compounds such as titanium nitride, combinations thereof or other conductive material(s). Implants known as workfunction implants may be introduced in gate electrode 714 to alter the workfunction thereof. Gate electrode 714 is formed by depositing a gate electrode material layer (not shown) over substrate 700, depositing a gate mask (not shown) over the gate electrode material layer, patterning the gate mask to define gate electrode 714, etching the gate electrode material layer to form gate electrode 714, and removing the gate mask. Gate electrode 714 is electrically isolated from channel region 706 by gate dielectric layer 712. Gate dielectric layer 712 is preferably silicon oxynitride and gate electrode 714 is poly-silicon etched using chlorine and bromine chemistry with a high etch selectivity with respect to gate dielectric layer 712 in accordance with the third embodiment of the present invention. Spacer 715 is formed using a deposition and anisotropic etching technique for protecting the sidewall of gate electrode 714 during a subsequent epitaxy step.

In Fig. 10C, a part or all of the active surface of substrate 700 not covered by gate dielectric layer 712 and spacer 715 is recessed to form at least one recess 709 with a depth d by plasma etching using chlorine and bromine chemistry. The depth d of recess 709 is about 50 Å to 1000 Å. An optional anneal may be performed to facilitate silicon migration to repair etch damage caused by etching recess 706 to smooth the surface of recess 709 for a subsequent epitaxy process.

In Fig. 10D, recess 709 is filled with a semiconductor material such as silicon-germanium alloy or silicon-carbon alloy to form a lattice-mismatched zone 705, and then a drain extension region 701 and source extension region 702 are formed oppositely adjacent to the strained channel region 706'. Thus, strained-channel transistor structure 7 in accordance with the fifth embodiment of the present invention is basically formed. Lattice-mismatched zone 705 is formed using an epitaxy process such as chemical vapor deposition, ultra-high vacuum chemical vapor deposition, or molecular beam epitaxy. Channel region 706 is strained to be a strained channel region 706' when lattice-mismatched zone 705 is formed. Lattice-mismatched zone 705 comprises

silicon-germanium alloy where molar fraction of germanium is about 0.1 to 0.9 when strained-channel transistor structure 7 is a P-channel transistor structure. When strained-channel transistor structure 7 is an N-channel transistor structure, lattice-mismatched zone 705 comprises silicon-carbon alloy where molar fraction of carbon is between about 0.01 and 0.04, and may further comprise germanium to be silicon-carbon-germanium alloy where molar fraction of germanium is less than ten times that of carbon. A silicon cap 722 is optionally formed on lattice-mismatched zone 705 using an epitaxy process such as chemical vapor deposition, ultra-high vacuum chemical vapor deposition, or molecular beam epitaxy. Lattice-mismatched zone 705 and optional silicon cap 722 may be in-situ doped or undoped during the epitaxy process. When lattice-mismatched zone 705 and optional silicon cap 722 are undoped during the epitaxy process, but will be doped subsequently, at which time dopants will be activated using a rapid thermal annealing process. Drain extension region 701 and source extension region 703 are formed by dopant diffusion from lattice-mismatched zone 705 and optional silicon cap 722. One or both of the drain extension region 701 and source extension region 703 comprise the lattice-mismatched zone 705 and optional silicon cap 722.

In Fig. 10E, a spacer 716 is formed overlying the spacer 715. Spacer 716 is formed using deposition and selectively etching a spacer material (not shown) such as silicon nitride or silicon dioxide. Spacer 716 is silicon nitride in accordance with the third embodiment of the present invention.

In Fig. 10F, a deeper drain region 702 is formed adjacent to drain extension region 701, and deeper source region 704 is formed adjacent to source extension region 703. Deeper drain region 702 combines with drain extension region 701, lattice-mismatched zone 705 when available, and optional silicon cap 722 when available to be a drain region 707, and deeper source region 704 combines with source extension region 703, lattice-mismatched zone 705 when available, and optional silicon cap 722 when available to be a source region 708. Deeper drain region 702 and deeper source region 704 are formed using ion implantation, PIII, gas or solid source diffusion, or other known techniques.

In Fig. 10G, a conductive layer 720 is optionally formed on drain region 707 and source region 708 to reduce resistances of drain region 707 and source region 708. Conductive layer 720 is formed using self-aligned silicide, or other metal deposition. Passivation layers and device contacts are subsequently formed so as to finish a device comprising strained-channel transistor structure 7 in accordance with the fifth embodiment of the present invention.

Sixth Embodiment

In the sixth embodiment of the present invention, a fabrication method of a strained-channel transistor structure where lattice-mismatched zone is formed using an ion implantation process according to the present invention is described.

In Fig. 11A, a semiconductor substrate such as a silicon substrate 800 is provided. Silicon substrate 800 comprises a previously formed plurality of isolation regions (not shown) and previously defined plurality of device regions (not shown). For example, the isolation regions may be shallow trench isolation regions. Figs. 11A through 11D provide a cross-sectional view of one single device region for easy description. Silicon substrate 800 comprises a conventional transistor structure comprising a channel region 806 in an active surface of substrate 800, a gate dielectric layer 812 on channel region 806, a gate electrode 814 on gate dielectric layer 812, a source region 808 and drain region 807 oppositely adjacent to channel region 806, and a spacer 816 on a sidewall of gate electrode 814, covering a part of the active surface of substrate 800. Drain region 807 comprises a drain extension region 801 and a deeper drain region 802, and source region 808 comprises a source extension region 803 and a deeper source region 804. Silicon substrate 800 is N-type doped when strained-channel transistor structure 8 in Fig. 11C is a P-channel transistor structure, or P-type doped when strained-channel transistor structure 8 in Fig. 11C is an N-channel transistor structure.

In Fig. 11B, an ion implantation process is performed to introduce ions 830 of one or more atomic species with a different atomic size from that of substrate 800 into drain region 807 and/or source region 808. Gate electrode 814 and spacer 816 act as a implantation mask during the ion implantation process. Thickness of spacer 816 is adjustable depending on lattice-mismatched zone 805 in Fig. 11C either extending into drain extension region 801 and/or source extension region 803, or not extending into drain extension region 801 and/or source extension region 803, as required.

In Fig. 11C, an annealing step is performed on the substrate 800 to form a lattice-mismatched zone in one or both of drain region 807 and source region 808. Thus, one or both of the drain region 807 and source region 808 comprise the lattice-mismatched zone 805. Channel region 806 is strained to be a strained channel region 806' when lattice-mismatched zone 805 is formed. Thus, strained-channel transistor structure 8 in accordance with the sixth embodiment of the present invention is basically formed. Lattice-mismatched zone 805 comprises silicon-germanium alloy where molar fraction of germanium is about 0.1 to 0.9 when strained-channel transistor structure 8 is a P-channel transistor structure. When strained-channel transistor

structure 8 is an N-channel transistor structure, lattice-mismatched zone 805 comprises silicon-carbon alloy where molar fraction of carbon is between about 0.01 and 0.04, and may further comprise germanium to be silicon-carbon-germanium alloy where molar fraction of germanium is less than ten times that of carbon.

In Fig. 11D, a conductive layer 820 is optionally formed on drain region 807 and source region 808 to reduce resistances of drain region 807 and source region 808. Conductive layer 820 is formed using self-aligned silicide, or other metal deposition process. Passivation layers and device contacts are subsequently formed so as to finish a device comprising strained-channel transistor structure 8 in accordance with the sixth embodiment of the present invention.

Although the present invention has been particularly shown and described above with reference to six specific embodiments, it is anticipated that alterations and modifications thereof will no doubt become apparent to those skilled in the art. It is therefore intended that the following claims be interpreted as covering all such alteration and modifications as fall within the true spirit and scope of the present invention.

What is claimed is:

1 1. A strained-channel transistor structure with
2 improved transport properties, comprising:
3 a strained channel region comprising a first
4 semiconductor material with a first natural
5 lattice constant;
6 a gate dielectric layer overlying the strained channel
7 region;
8 a gate electrode overlying the gate dielectric layer;
9 and
10 a source region and drain region oppositely adjacent
11 to the strained channel region, one or both of
12 the source region and drain region comprising a
13 lattice-mismatched zone comprising a second
14 semiconductor material with a second natural
15 lattice constant different from the first natural
16 lattice constant.

1 2. The transistor structure as claimed in claim 1,
2 wherein the lattice-mismatched zone is about 10 to 1000 Å
3 thick.

1 3. The transistor structure as claimed in claim 1,
2 wherein the lattice-mismatched zone is about 300 to 1000 Å
3 thick.

1 4. The transistor structure as claimed in claim 1,
2 wherein the first semiconductor material comprises silicon.

1 5. The transistor structure as claimed in claim 1,
2 wherein the second semiconductor comprises silicon and
3 germanium.

1 6. The transistor structure as claimed in claim 1,
2 wherein the second semiconductor comprises silicon and
3 carbon.

1 7. The transistor structure as claimed in claim 5,
2 wherein molar fraction of germanium in the second
3 semiconductor material is about 0.1 to 0.9.

1 8. The transistor structure as claimed in claim 6,
2 wherein molar fraction of carbon in the second
3 semiconductor material is about 0.01 to 0.04.

1 9. The transistor structure as claimed in claim 6,
2 wherein the second semiconductor material further comprises
3 germanium whose molar fraction in the second semiconductor
4 material is less than ten times that of carbon in the
5 second semiconductor material.

- 1 10. The transistor structure as claimed in claim 1,
2 wherein the strained channel region is under a tensile
3 strain in a source-to-drain direction.
- 1 11. The transistor structure as claimed in claim 1,
2 wherein the strained channel region is under a compressive
3 strain in a vertical direction.
- 1 12. The transistor structure as claimed in claim 10,
2 wherein the tensile strain is about 0.1% to 4%.
- 1 13. The transistor structure as claimed in claim 11,
2 wherein the compressive strain is about 0.1% to 4%.
- 1 14. The transistor structure as claimed in claim 1,
2 wherein the strained channel region is under a compressive
3 strain in a source-to-drain direction.
- 1 15. The transistor structure as claimed in claim 1,
2 wherein the strained channel region is under a tensile
3 strain in a vertical direction.
- 1 16. The transistor structure as claimed in claim 14,
2 wherein the compressive strain is about 0.1% to 4%.
- 1 17. The transistor structure as claimed in claim 15,
2 wherein the tensile strain is about 0.1% to 4%.
- 1 18. The transistor structure as claimed in claim 1,
2 further comprising a cap layer on the lattice-mismatched
3 zone.
- 1 19. The transistor structure as claimed in claim 18,
2 wherein the cap layer comprises the first semiconductor
3 material.
- 1 20. The transistor structure as claimed in claim 1,
2 wherein the source region comprises a source extension
3 region and a deep source region, and the drain region
4 comprises a drain extension region and a deep drain region.
- 1 21. The transistor structure as claimed in claim 20,
2 wherein the lattice-mismatched zone laterally extends into
3 the source extension region and/or drain extension region.
- 1 22. The transistor structure as claimed in claim 1,
2 wherein the lattice-mismatched zone further extends beyond
3 the source region and/or drain region.
- 1 23. The transistor structure as claimed in claim 1,
2 wherein the gate dielectric layer is silicon oxide or
3 silicon oxynitride.

1 24. The transistor structure as claimed in claim 1,
2 wherein the gate dielectric layer is Al₂O₃, HfO₂, ZrO₂, HfON,
3 HfSiO₄, ZrSiO₄, La₂O₃, or combinations thereof.

1 25. The transistor structure as claimed in claim 24,
2 wherein the relative permittivity of the gate dielectric
3 layer is larger than 5.

1 26. The transistor structure as claimed in claim 1,
2 wherein the gate dielectric layer is about 3 to 100 Å
3 thick.

1 27. The transistor structure as claimed in claim 1,
2 wherein the gate electrode comprises poly-crystalline
3 silicon.

1 28. The transistor structure as claimed in claim 1,
2 wherein the gate electrode comprises poly-crystalline
3 silicon germanium.

1 29. The transistor structure as claimed in claim 1,
2 wherein the gate electrode comprises a metal.

1 30. The transistor structure as claimed in claim 1,
2 wherein the gate electrode comprises a metal silicide.

1 31. The transistor structure as claimed in claim 1,
2 further comprising a conductive material on the source
3 region and drain region.

1 32. The transistor structure as claimed in claim 31,
2 wherein the conductive material comprises a metal.

1 33. The transistor structure as claimed in claim 31,
2 wherein the conductive material comprises a metal silicide.

1 34. A method of fabrication a strained-channel
2 transistor structure with improved transport properties,
3 comprising:

4 providing a substrate comprising a first semiconductor
5 material with a first natural lattice constant, a
6 gate dielectric layer on the substrate, and a
7 gate electrode on the gate dielectric layer;

8 forming a first source region and first drain region
9 oppositely adjacent to the gate dielectric layer;

10 forming a spacer on a sidewall of the gate electrode;
11 recessing the surface of the substrate not covered by
12 the spacer and gate dielectric layer to form a
13 recess;

14 filling the recess with a second semiconductor
15 material with a second natural lattice constant

16 different from the first natural lattice constant
17 as a lattice-mismatched zone; and
18 forming a second source region adjacent to the first
19 source region and second drain region adjacent to
20 the first drain region, one or both of the second
21 source region and second drain region comprising
22 the lattice-mismatched zone.

1 35. The method as claimed in claim 34, wherein the
2 first semiconductor material comprises silicon.

1 36. The method as claimed in claim 34, wherein the
2 second semiconductor comprises silicon and germanium.

1 37. The method as claimed in claim 34, wherein the
2 second semiconductor comprises silicon and carbon.

1 38. The method as claimed in claim 36, wherein molar
2 fraction of germanium in the second semiconductor material
3 is about 0.1 to 0.9.

1 39. The method as claimed in claim 37, wherein molar
2 fraction of carbon in the second semiconductor material is
3 about 0.01 to 0.04.

1 40. The method as claimed in claim 37, wherein the
2 second semiconductor material further comprises germanium
3 whose molar fraction in the second semiconductor material
4 is less than ten times that of carbon in the second
5 semiconductor material.

1 41. The method as claimed in claim 34, wherein the
2 recess is formed by plasma etching.

1 42. The method as claimed in claim 34, wherein the
2 recess is about 50 to 1000 Å deep.

1 43. The method as claimed in claim 34, further
2 comprising annealing the substrate in an inert ambient
3 after forming the recess.

1 44. The method as claimed in claim 34, wherein the
2 second semiconductor material is filled in the recess by an
3 epitaxy process using chemical vapor deposition, ultra-high
4 vacuum chemical vapor deposition, or molecular beam
5 epitaxy.

1 45. The method as claimed in claim 34, wherein the
2 second semiconductor material is in-situ doped when filling
3 the recess.

1 46. The method as claimed in claim 34, wherein the
2 second semiconductor material is undoped when filling the
3 recess.

1 47. The method as claimed in claim 34, further
2 comprising forming a cap layer on the second semiconductor
3 material.

1 48. The method as claimed in claim 47, wherein the
2 cap layer comprises the first semiconductor material.

1 49. The method as claimed in claim 34, wherein the
2 gate dielectric layer comprises silicon oxide or silicon
3 oxynitride.

1 50. The method as claimed in claim 34, wherein the
2 gate dielectric layer is Al_2O_3 , HfO_2 , ZrO_2 , HfON , HfSiO_4 ,
3 ZrSiO_4 , La_2O_3 , or combinations thereof.

1 51. The method as claimed in claim 50, wherein the
2 relative permittivity of the gate dielectric layer is
3 larger than 5.

1 52. The method as claimed in claim 34, wherein the
2 gate dielectric layer is about 3 to 100 Å thick.

1 53. The method as claimed in claim 34, wherein the
2 gate electrode comprises poly-crystalline silicon.

1 54. The method as claimed in claim 34, wherein the
2 gate electrode comprises poly-crystalline silicon
3 germanium.

1 55. The method as claimed in claim 34, wherein the
2 gate electrode comprises a metal.

1 56. The method as claimed in claim 34, wherein the
2 gate electrode comprises a metal silicide.

1 57. The method as claimed in claim 34, wherein the
2 first source region and first drain region are formed by
3 ion implantation or plasma immersion ion implantation.

1 58. The method as claimed in claim 34, wherein the
2 second source region and second drain region are formed by
3 ion implantation or plasma immersion ion implantation.

1 59. The method as claimed in claim 34, further
2 comprising forming a conductive material on the second
3 source region and second drain region.

1 60. The method as claimed in claim 59, wherein the
2 conductive material comprises a metal.

1 61. The method as claimed in claim 59, wherein the
2 conductive material comprises a metal silicide.

1 62. A method of fabrication a strained-channel
2 transistor structure with improved transport properties,
3 comprising:

4 providing a substrate comprising a first semiconductor
5 material with a first natural lattice constant, a
6 gate dielectric layer on the substrate, a gate
7 electrode on the gate dielectric layer, a source
8 region and drain region oppositely adjacent to
9 the gate dielectric layer, and a spacer on a
10 sidewall of the gate electrode;

11 recessing one or both of the source region and drain
12 region to form a recess; and

13 filling the recess with a second semiconductor
14 material with a second natural lattice constant
15 different from the first natural lattice constant
16 as a lattice-mismatched zone.

1 63. The method as claimed in claim 62, wherein the
2 first semiconductor material comprises silicon.

1 64. The method as claimed in claim 62, wherein the
2 second semiconductor comprises silicon and germanium.

1 65. The method as claimed in claim 62, wherein the
2 second semiconductor comprises silicon and carbon.

1 66. The method as claimed in claim 64, wherein molar
2 fraction of germanium in the second semiconductor material
3 is about 0.1 to 0.9.

1 67. The method as claimed in claim 65, wherein molar
2 fraction of carbon in the second semiconductor material is
3 about 0.01 to 0.04.

1 68. The method as claimed in claim 65, wherein the
2 second semiconductor material further comprises germanium
3 whose molar fraction in the second semiconductor material
4 is less than ten times that of carbon in the second
5 semiconductor material.

1 69. The method as claimed in claim 62, wherein the
2 recess is formed by plasma etching.

1 70. The method as claimed in claim 62, wherein the
2 recess is about 50 to 1000 Å deep.

1 71. The method as claimed in claim 62, further
2 comprising annealing the substrate in an inert ambient
3 after forming the recess.

1 72. The method as claimed in claim 62, wherein the
2 second semiconductor material is filled in the recess by an
3 epitaxy process using chemical vapor deposition, ultra-high
4 vacuum chemical vapor deposition, or molecular beam
5 epitaxy.

1 73. The method as claimed in claim 62, wherein the
2 second semiconductor material is in-situ doped when filling
3 the recess.

1 74. The method as claimed in claim 62, further
2 comprising forming a cap layer on the second semiconductor
3 material.

1 75. The method as claimed in claim 74, wherein the
2 cap layer comprises the first semiconductor material.

1 76. The method as claimed in claim 62, wherein the
2 gate dielectric layer comprises silicon oxide or silicon
3 oxynitride.

1 77. The method as claimed in claim 62, wherein the
2 gate dielectric layer comprises Al_2O_3 , HfO_2 , ZrO_2 , HfON ,
3 HfSiO_4 , ZrSiO_4 , La_2O_3 , or combinations thereof.

1 78. The method as claimed in claim 77, wherein the
2 relative permittivity of the gate dielectric layer is
3 larger than 5.

1 79. The method as claimed in claim 62, wherein the
2 gate dielectric layer is about 3 to 100 Å thick.

1 80. The method as claimed in claim 62, wherein the
2 gate electrode comprises poly-crystalline silicon.

1 81. The method as claimed in claim 62, wherein the
2 gate electrode comprises poly-crystalline silicon
3 germanium.

1 82. The method as claimed in claim 62, wherein the
2 gate electrode comprises a metal.

1 83. The method as claimed in claim 62, wherein the
2 gate electrode comprises a metal silicide.

1 84. The method as claimed in claim 62, further
2 comprising forming a conductive material on the source
3 region and drain region.

1 85. The method as claimed in claim 84, wherein the
2 conductive material comprises a metal.

1 86. The method as claimed in claim 84, wherein the
2 conductive material comprises a metal silicide.

1 87. A method of fabrication a strained-channel
2 transistor structure with improved transport properties,
3 comprising:

4 providing a substrate comprising a first semiconductor
5 material with a first natural lattice constant, a
6 gate dielectric layer on the substrate, a gate
7 electrode on the gate dielectric layer, and a
8 first spacer on a sidewall of the gate electrode;
9 recessing the surface of the substrate not covered by
10 the spacer and gate dielectric layer to form a
11 recess;

12 filling the recess with a second semiconductor
13 material with a second natural lattice constant
14 different from the first natural lattice constant
15 as a lattice-mismatched zone; and

16 forming a first source region and second drain region
17 oppositely adjacent to the gate dielectric layer,
18 one or both of the first source region and second
19 drain region comprising the lattice-mismatched
20 zone.

1 88. The method as claimed in claim 87, further
2 comprising:

3 forming a second spacer overlying the first spacer;
4 and

5 forming a second source region adjacent to the first
6 source region and second drain region adjacent to
7 the first drain region.

1 89. The method as claimed in claim 87, wherein the
2 second semiconductor material is in-situ doped when filling
3 the recess.

1 90. The method as claimed in claim 87, wherein the
2 second semiconductor material is undoped when filling the
3 recess.

1 91. The method as claimed in claim 87, wherein the
2 first source region and first drain region are formed by
3 ion implantation or plasma immersion ion implantation.

1 92. The method as claimed in claim 87, wherein the
2 first semiconductor material comprises silicon.

1 93. The method as claimed in claim 87, wherein the
2 second semiconductor comprises silicon and germanium.

1 94. The method as claimed in claim 87, wherein the
2 second semiconductor comprises silicon and carbon.

1 95. The method as claimed in claim 93, wherein molar
2 fraction of germanium in the second semiconductor material
3 is about 0.1 to 0.9.

1 96. The method as claimed in claim 94, wherein molar
2 fraction of carbon in the second semiconductor material is
3 about 0.01 to 0.04.

1 97. The method as claimed in claim 94, wherein the
2 second semiconductor material further comprises germanium
3 whose molar fraction in the second semiconductor material
4 is less than ten times that of carbon in the second
5 semiconductor material.

1 98. The method as claimed in claim 87, wherein the
2 recess is formed by plasma etching.

1 99. The method as claimed in claim 87, wherein the
2 recess is about 50 to 1000 Å deep.

1 100. The method as claimed in claim 87, further
2 comprising annealing the substrate in an inert ambient
3 after forming the recess.

1 101. The method as claimed in claim 87, wherein the
2 second semiconductor material is filled in the recess by an
3 epitaxy process using chemical vapor deposition, ultra-high
4 vacuum chemical vapor deposition, or molecular beam
5 epitaxy.

1 102. The method as claimed in claim 87, further
2 comprising forming a cap layer on the second semiconductor
3 material.

1 103. The method as claimed in claim 102, wherein the
2 cap layer comprises the first semiconductor material.

1 104. The method as claimed in claim 87, wherein the
2 gate dielectric layer comprises silicon oxide or silicon
3 oxynitride.

1 105. The method as claimed in claim 87, wherein the
2 gate dielectric layer comprises Al_2O_3 , HfO_2 , ZrO_2 , HfON ,
3 HfSiO_4 , ZrSiO_4 , La_2O_3 , or combinations thereof.

1 106. The method as claimed in claim 87, wherein the
2 relative permittivity of the gate dielectric layer is
3 larger than 5.

1 107. The method as claimed in claim 87, wherein the
2 gate dielectric layer is about 3 to 100 Å thick.

1 108. The method as claimed in claim 87, wherein the
2 gate electrode comprises poly-crystalline silicon.

1 109. The method as claimed in claim 87, wherein the
2 gate electrode comprises poly-crystalline silicon
3 germanium.

1 110. The method as claimed in claim 87, wherein the
2 gate electrode comprises a metal.

1 111. The method as claimed in claim 87, wherein the
2 gate electrode comprises a metal silicide.

1 112. The method as claimed in claim 88, wherein the
2 second source region and second drain region are formed by
3 ion implantation or plasma immersion ion implantation.

1 113. The method as claimed in claim 87, further
2 comprising forming a conductive material on the first
3 source region and first drain region.

1 114. The method as claimed in claim 113, wherein the
2 conductive material comprises a metal.

1 115. The method as claimed in claim 113, wherein the
2 conductive material comprises a metal silicide.

1 116. A method of fabrication a strained-channel
2 transistor structure with improved transport properties,
3 comprising:

4 providing a substrate comprising a semiconductor
5 material, a gate dielectric layer on the
6 substrate, a gate electrode on the gate
7 dielectric layer, and a source region and drain
8 region oppositely adjacent to the gate dielectric
9 layer; and

10 implanting an element with an atomic size different
11 from that of the semiconductor material to form a
12 lattice-mismatched zone in one or both of the
13 source region and drain region.

1 117. The method as claimed in claim 116, further
2 comprising annealing the substrate after implanting the
3 element.

1 118. The method as claimed in claim 116, wherein the
2 first semiconductor comprises silicon.

- 1 119. The method as claimed in claim 116, wherein the
2 element is germanium.
- 1 120. The method as claimed in claim 116, wherein the
2 element is carbon.
- 1 121. The method as claimed in claim 119, wherein molar
2 fraction of germanium in the lattice-mismatched zone is
3 about 0.1 to 0.9.
- 1 122. The method as claimed in claim 120, wherein molar
2 fraction of carbon in the lattice-mismatched zone is about
3 0.01 to 0.04.
- 1 123. The method as claimed in claim 116, wherein the
2 gate dielectric layer comprises silicon oxide or silicon
3 oxynitride.
- 1 124. The method as claimed in claim 124, wherein the
2 gate dielectric layer comprises Al_2O_3 , HfO_2 , ZrO_2 , HfON ,
3 HfSiO_4 , ZrSiO_4 , La_2O_3 , or combinations thereof.
- 1 125. The method as claimed in claim 124, wherein the
2 relative permittivity of the gate dielectric layer is
3 larger than 5.
- 1 126. The method as claimed in claim 116, wherein the
2 gate dielectric layer is about 3 to 100 Å thick.
- 1 127. The method as claimed in claim 116, wherein the
2 gate electrode comprises poly-crystalline silicon.
- 1 128. The method as claimed in claim 116, wherein the
2 gate electrode comprises poly-crystalline silicon
3 germanium.
- 1 129. The method as claimed in claim 116, wherein the
2 gate electrode comprises a metal.
- 1 130. The method as claimed in claim 116, wherein the
2 gate electrode comprises a metal silicide.
- 1 131. The method as claimed in claim 116, further
2 comprising forming a conductive material on the source
3 region and drain region.
- 1 132. The method as claimed in claim 116, wherein the
2 conductive material comprises a metal.
- 1 133. The method as claimed in claim 116, wherein the
2 conductive material comprises a metal silicide.