

CLAIMS:

1. A method of manufacturing a LED precursor comprising:
forming a monolithic growth stack having a growth surface; and
5 forming a monolithic LED stack on the growth surface of the monolithic growth stack,
wherein:
 - a) forming the monolithic growth stack comprises:
10 forming a first semiconducting layer comprising a Group III-nitride;
forming a second semiconducting layer on the first semiconducting layer, the second semiconducting layer comprising a first Group III-nitride including a donor dopant such that the second semiconducting layer has a donor density of at least $5 \times 10^{18} \text{ cm}^{-3}$;
forming a third semiconducting layer on an opposite side of the second
15 semiconducting layer to the first semiconducting layer, wherein the third semiconducting layer provides the growth surface of the monolithic growth stack, the third semiconducting layer comprising a second Group III-nitride different to the first Group-III-nitride such that the third semiconducting layer is formed on the second semiconducting layer under compressive strain; and
20 selectively removing a portion of the third semiconducting layer from the growth surface through a thickness of the third semiconducting layer such that the growth surface of the monolithic growth stack comprises a mesa surface of third semiconducting layer and a sidewall surface of the third semiconducting layer encircling the mesa surface,
wherein following formation of the third semiconducting layer:
25 the second semiconducting layer is subjected to a porosity treatment to increase an areal porosity of the second semiconducting layer to at least 15%; and
the third semiconducting layer is heated to a strain relaxing temperature such that the third semiconducting layer relaxes such that an in-plane lattice constant of the mesa surface increases; and
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 - b) forming the monolithic LED stack comprises:
forming a fourth semiconducting layer comprising a Group III-nitride on the growth surface of the monolithic growth stack, such that the fourth semiconducting layer covers the mesa surface of the third semiconducting layer;

forming an active layer on the fourth semiconducting layer, the active layer comprising a plurality of quantum well layers, each quantum well layer comprising a Group III-nitride;

5 forming a p-type semiconducting layer comprising a Group III-nitride on the active layer.

2. A method according to claim 1, wherein
the second semiconducting layer comprises GaN; and/or
the third semiconducting layer comprises $\text{In}_x\text{Ga}_{1-x}\text{N}$, where $0 < X \leq 1$.
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3. A method according to claim 1 or claim 2, wherein
each quantum well layer of the active layer comprises $\text{In}_z\text{Ga}_{1-z}\text{N}$, where $0.2 < Z \leq 0.5$.
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4. A method according to any preceding claim, wherein
the second semiconducting layer is subjected to the porosity treatment prior to selectively removing a portion of the third semiconducting layer from the growth surface.
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5. A method according to any preceding claim, wherein
the third semiconducting layer is selectively removed such that the growth surface of the monolithic growth stack comprises a surface of the second semiconducting layer.
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6. A method according to any preceding claim, wherein forming the monolithic growth stack further comprises:
selectively removing a portion of the second semiconducting layer aligned with the portion of the third semiconducting layer which is selectively removed such that the growth surface of the monolithic growth stack comprises a sidewall surface of the second semiconducting layer.
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7. A method according to claim 6, wherein
the second semiconducting layer is selectively removed such that the sidewall surface of the second semiconducting layer is aligned with the sidewall surface of the third semiconducting layer.
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8. A method according to claim 6 or 7, wherein

the second semiconducting layer is selectively removed such that the growth surface comprises a portion of a surface of the first semiconducting layer.

9. A method according to any preceding claim, wherein the fourth semiconducting layer comprises GaN.
10. A method according to any preceding claim, wherein the fourth semiconducting layer is formed on the growth surface to provide an inclined sidewall portion extending from a mesa portion of the fourth semiconducting layer on the mesa surface of the third semiconducting layer towards the second semiconducting layer.
11. A method according to any one of claims 4 to 8, wherein forming the monolithic growth stack further comprises:
selectively forming a masking layer on the growth surface of the monolithic growth stack, the masking layer comprising an aperture aligned with the mesa surface of the monolithic growth stack.
12. A method according to claim 11, wherein the monolithic LED stack is selectively formed on the mesa surface of the monolithic growth stack and not on the growth surface covered by the masking layer.
13. A LED precursor comprising:
a monolithic growth stack having a growth surface; and
a monolithic LED stack provided on the growth surface of the monolithic growth stack,
wherein:
a) the monolithic growth stack comprises:
a first semiconducting layer comprising a Group III-nitride;
a second semiconducting layer provided on the first semiconducting layer, the second semiconducting layer comprising a first Group III-nitride including a donor dopant such that the second semiconducting layer has a donor density of at least $5 \times 10^{18} \text{ cm}^{-3}$, wherein the second semiconducting layer has an areal porosity of at least 15 % and a first in-plane lattice constant; and

a third semiconducting layer provided on an opposite side of the second semiconducting layer to the first semiconducting layer, the third semiconducting layer comprising a second Group III-nitride different to the first Group-III-nitride,

wherein the monolithic growth stack comprises a mesa structure comprising the
5 third semiconducting layer such that the growth surface comprises a mesa surface of third semiconducting layer and a sidewall surface of the third semiconducting layer encircling the mesa surface, the sidewall surface of the third semiconducting layer inclined relative to the mesa surface,

wherein the mesa surface of the third semiconducting layer has a second in-plane
10 lattice constant which is greater than the first in-plane lattice constant; and

b) the monolithic LED stack comprises:

a fourth semiconducting layer provided on the growth surface of the monolithic growth stack, such that the fourth semiconducting layer covers the mesa surface of the third semiconducting layer and the sidewall surface of the third semiconducting layer;

15 an active layer provided on the fourth semiconducting layer, the active layer comprising a plurality of quantum well layers, each quantum well layer comprising a Group III-nitride; and

a p-type semiconducting layer comprising a Group III-nitride provided on the active layer.

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14. A LED precursor according to claim 13, wherein
the second semiconducting layer comprises GaN; and/or
the third semiconducting layer comprises $\text{In}_x\text{Ga}_{1-x}\text{N}$, where $0 < x \leq 1$.

25 15. A LED precursor according to claim 13 or claim 14, wherein
each quantum well layer of the active layer comprises $\text{In}_z\text{Ga}_{1-z}\text{N}$, where $0.2 < z \leq 0.5$.

16. A LED precursor according to any of claims 13 to 15, wherein the sidewall surface
30 of the third semiconducting layer is inclined in a direction transverse to the mesa surface.

17. A LED precursor according to any of claims 13 to 16, wherein
the mesa structure extends from the porous semiconducting layer such that growth surface comprises the porous semiconducting layer.

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18. A LED precursor according to any of claims 13 to 17, wherein
the growth surface of the monolithic growth stack comprises a sidewall surface of
the porous semiconducting layer aligned with the sidewall surface of the third
semiconducting layer.
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19. A LED precursor according to claim 18, wherein
the mesa structure extends from the first semiconducting layer such that the growth
surface comprises a portion of a surface of the first semiconducting layer.
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20. A LED precursor according to any of claims 13 to 19, wherein the fourth
semiconducting layer comprises GaN.
21. A LED precursor according to any of claims 13 to 20, wherein
the fourth semiconducting layer is provided on the growth surface to provide an
15 inclined sidewall portion extending from a mesa portion of the fourth semiconducting layer
on the mesa surface of the third semiconducting layer towards the second semiconducting
layer.
22. A LED precursor according to any of claims 16 to 21, wherein the monolithic growth
20 stack further comprises:
a masking layer provided on the growth surface of the monolithic growth stack, the
masking layer comprising an aperture aligned with the mesa surface of the monolithic
growth stack.
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23. A LED precursor according to claim 22, wherein
the monolithic LED stack is selectively provided only on the mesa surface of the
monolithic growth stack.
24. A LED precursor according to any of claims 13 to 23, wherein
30 the LED precursor is a micro LED precursor wherein the monolithic LED stack has a
surface area dimension in a plane aligned with the first semiconducting layer of less than
100 μm x 100 μm .
25. A LED array precursor comprising:

a plurality of LED precursors according to any of claims 13 to 24, the plurality of LED precursor arranged in a two-dimensional array.