

PATENT SPECIFICATION (11)

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(54) IMPROVEMENT IN INPUT CIRCUITS

(71) We, HITACHI LIMITED, of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to an input circuit of a semiconductor integrated circuit device composed of insulated gate field-effect transistors (hereinafter referred to as "FETs").

In general, the input impedance of the gate of a FET is highly capacitive. In a FET, therefore, even very small stray charges can induce a high voltage and cause dielectric breakdown of the gate.

In a semiconductor integrated circuit composed of FETs, the capacitance of an externally-mounted terminal, such as a power supply line or an earth line, is usually large since the parasitic capacitances of the component FETs are connected in parallel. For this reason, a high voltage is not induced by a very small amount of charge, and the problem of dielectric breakdown does not arise.

However, the problem still occurs in a circuit, such as an input gate circuit, whose capacitance as viewed from an input terminal is very small. Various circuits have therefore been hitherto provided as protection against static electricity for semiconductor integrated circuits composed of FETs, as stated in "Denshi Zairyo" (Electronic Material), July 1971, page 112, published in Japan.

In the case where an input signal is a signal from a mechanical switch, as in an electronic desk top calculator, it is inadvisable to transmit binary levels by means of the switch. An expedient which has been commonly adopted is illustrated in Figure 1 of the accompanying drawing, which shows a prior-art input circuit of an integrated circuit composed of FETs. Two possible input levels are provided at the input IN, depending on whether switch SW between the input and earth is open or closed. An open-

ing-preventing FET Q3 for the input is provided in the integrated circuit 1, which FET ensures that the logical state at the input when the switch SW is open is positively determined. Thus, various disadvantages, such as susceptibility to noise, are lessened. A resistor R is also connected, as shown, for the protection of the FETs.

Where the resistor R is incorporated as shown in Figure 1, the input signal level at a point A is determined by the ratio between the resistance of the resistor R and the conductance of the FET Q3. Accordingly, in order to reduce the loss of input level at the point A and to ensure that the FET Q2 is not affected by noise, the value of resistance of the resistor R should desirably be as small as possible. In contrast, the value of resistance of the resistor R should desirably be as large as possible for the protection of the gate of the FET Q2. Previously, it has been necessary to reach a compromise between these requirements when setting the value of resistance of the resistor R. Because of that compromise, it is possible that either malfunction of the FET Q2 due to noise or breakdown of the gate of the FET Q2 due to stray charges will arise.

As mentioned in the above cited "Denshi Zairyo", the problem can be solved by interposing the resistor R between the point A and a point B, as in the alternative prior-art input circuit shown in Figure 2 of the accompanying drawing. It has been shown, however, that the gate insulation of the input FET is destroyed when such a circuit is used. The cause for the destruction of the gate insulation is thought to be that, since the gate-source capacitance C₁ of the FET Q3 is extremely small, a high voltage is induced thereacross by a very small amount of stray charge.

According to the present invention there is provided an input circuit for a semiconductor integrated circuit composed of insulated gate field-effect transistors, including driving transistor with its source connected to a reference potential, its drain connected to an output terminal and its gate connected through a first resistor to an input ter-

SPECIFIC INSTRUCTIONS - SEE ATTACHED SLIP

5 minal, a load connected between a first power supply terminal and the output terminal, an opening-preventing input transistor connected between the input terminal and the first power supply terminal, there being a second resistor between the input terminal and the said input transistor, and an input switching means operable to connect the input-terminal to or disconnect it from the reference potential.

10 One preferred embodiment of the invention will now be described by way of example, with reference to Figure 3 of the accompanying drawing, which is a circuit diagram of an input gate circuit.

15 Referring to Figure 3, in an inverter comprising FETs Q1 and Q2, the gate of the driving FET Q2 is connected to an input terminal IN through a protective resistor R1. The input terminal IN is connected to the source of an opening-preventing input FET Q3 through a protective resistor R2. The drain of the FET Q3 is connected directly to first power supply terminal VDD, and the gate is connected to a second power supply terminal VGG, optionally through a protective resistor R3. The FET Q2 has a gate capacitance C between its gate and earth (to which its source is connected), while there is a gate capacitance C¹ between the gate and source of the FET Q3. The drain of the FET Q2 is connected to an output terminal OUT to which is connected the load for Q2 namely FET Q1 of which the drain is connected to the first power supply terminal VDD and the gate to the second power supply terminal VGG.

20 The protective resistor R1 and the gate capacitance C form an integration circuit between the gate of the driving FET Q2 of the inverter and the input terminal IN. Accordingly, an abruptly rising voltage, ascribable to, for example, noise from the input is suppressed by the integration circuit, i.e. the output voltage of the integration circuit cannot rise suddenly. The larger the resistance of the protective resistor R1, the greater can be the suppression of voltage exerted on the gate of FET Q2 and dielectric breakdown of the FET Q2 can be prevented. However, because no resistor (such as R, Fig. 1) is present between the switch SW and the point A, the input signal level at point A becomes equal to the reference potential level, in this case earth potential. In the situation seen in Figure 1, the input signal level at point A is determined by the ratio between the resistance of R and the conductance of Q3. Accordingly, the embodiment avoids the loss of signal level experienced in that prior art while having no less noise tolerance.

25 At the source of the FET Q3, the protective resistor R2 and the parasitic gate cap-

65 acitance C¹ of the FET Q3 form an integration circuit. The FET Q3 can accordingly be protected in the same manner as described above.

70 Further, by inserting the protective resistor R3 between the gate of the FET Q3 and the second power source VGG, the breakdown of the gate can be prevented, since if a breakdown current begins to flow, the voltage between the gate and the source of the FET Q3 is reduced small by the resistor R3.

75 The values of resistance of the resistors R1 to R3 are preferably large, but these values, particularly of the resistors R1 and R2, cannot be made very large. The reason for this is that, when the values of resistance of the resistors R1 and R2 are made large, the charging and discharging time of the capacitor C is lengthened, and this renders the switching time of the FET Q2 long. The values of resistance of the resistors R1 and R2 must, therefore, be appropriately selected.

80 The operation of the circuit can be enhanced, if desired, by connecting a clamp diode in parallel with each of the resistors R1 to R3.

WHAT WE CLAIM IS:—

95 1. An input circuit for a semiconductor integrated circuit composed of insulated gate field-effect transistors, including driving transistor with its source connected to a reference potential, its drain connected to an output terminal and its gate connected through a first resistor to an input terminal, a load connected between a first power supply terminal and the output terminal, an opening-preventing input transistor connected between the input terminal and the first power supply terminal, there being a second resistor between the input terminal and the said input transistor, and an input switching means operable to connect the input-terminal to or disconnect it from the reference potential.

100 2. An input circuit according to Claim 1, wherein a third resistor is connected between the gate of said input transistor and a second power supply terminal.

105 3. An input circuit according to Claim 1 or Claim 2 wherein the load is a load transistor with its gate connected to a or the second power supply terminal, its source to the output terminal and its drain to the first power supply terminal.

110 4. An input circuit according to Claim 1, Claim 2 or Claim 3, wherein a clamp diode is connected in parallel with each of said resistors.

115 5. An input circuit for a semiconductor integrated circuit, constructed and arranged to operate substantially as herein described

5 minal, a load connected between a first power supply terminal and the output terminal, an opening-preventing input transistor connected between the input terminal and the first power supply terminal, there being a second resistor between the input terminal and the said input transistor, and an input switching means operable to connect the input-terminal to or disconnect it from the reference potential.

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20 The protective resistor R1 and the gate capacitance C form an integration circuit between the gate of the driving FET Q2 of the inverter and the input terminal IN. Accordingly, an abruptly rising voltage, ascribable to, for example, noise from the input is suppressed by the integration circuit, i.e. the output voltage of the integration circuit cannot rise suddenly. The larger the resistance of the protective resistor R1, the greater can be the suppression of voltage exerted on the gate of FET Q2 and dielectric breakdown of the FET Q2 can be prevented. However, because no resistor (such as R, Fig. 1) is present between the switch SW and the point A, the input signal level at point A becomes equal to the reference potential level, in this case earth potential. In the situation seen in Figure 1, the input signal level at point A is determined by the ratio between the resistance of R and the conductance of Q3. Accordingly, the embodiment avoids the loss of signal level experienced in that prior art while having no less noise tolerance.

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105 3. An input circuit according to Claim 1 or Claim 2 wherein the load is a load transistor with its gate connected to a or the second power supply terminal, its source to the output terminal and its drain to the first power supply terminal.

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with reference to and as illustrated in Figure 3 of the accompanying drawing.

6. A semiconductor integrated circuit incorporating an input circuit according to
5 any one of the preceding claims.

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The following amendments were allowed under Section 29 on 3 December 1979:

Page 1, line 79, *delete* mentioned in *insert* suggested by

Page 1, lines 82 and 83, *delete* prior art

Sheet 1 of drawings, figure 2, *delete* PRIOR ART