ABSTRACT

A METHOD TO FORM SHALLOW TRENCH ISOLATION STRUCTURES WITH IMPROVED ISOLATION FILL AND SURFACE PLANARITY

A method to form shallow trench isolation structures with improved isolation fill and surface planarity is described. A pad oxide layer is provided over the surface of a semiconductor substrate. A silicon nitride layer is deposited overlying the pad oxide layer. A thin oxide layer is deposited overlying the silicon nitride layer. An isolation trench is etched through the thin oxide layer, the nitride layer, and the pad oxide layer and into the substrate. The silicon nitride layer exposed within the trench is etched to form a lateral undercut leaving a projection of the thin oxide layer and exposing a portion of the underlying pad oxide layer. The thin oxide layer and the exposed portion of the pad oxide layer are etched away thereby exposing portions of the surface of the substrate. A liner oxide is grown on the exposed portions of the semiconductor substrate within the isolation trench and on the surface of the substrate. A layer of isolation dielectric is deposited overlying the liner oxide and the silicon nitride and filling the isolation trench. The isolation dielectric is polished away stopping at the silicon nitride layer. The remaining silicon nitride etched away. The isolation dielectric and the pad oxide are etched away from the surface of the semiconductor substrate. The fabrication of the integrated circuit device is completed.

(FIGURE 3 IS SUGGESTED FOR PUBLICATION)