

ABSTRACT

A memory device according to some embodiments of the present disclosure may comprise a substrate including a cell region and a peripheral region, a first transistor disposed in the peripheral region of the substrate, the first transistor comprising a first gate insulating layer, a first gate electrode, and a first gate capping layer and a second transistor disposed in the peripheral region of the substrate, the second transistor comprising a semiconductor layer, a second gate insulating layer having a lower surface positioned higher than a lower surface of the first gate insulating layer, a second gate electrode, and a second gate capping layer having an upper surface positioned at the same height as an upper surface of the first gate capping layer.

FIG. 2

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