CLAIMS

1. A semiconductor device comprising:

a plurality of first fin-shaped patterns in a first region of a substrate and spaced apart from each other in a first direction;

a plurality of second fin-shaped patterns in a second region of the substrate and spaced apart from each other in a second direction;

a first field insulating film on the substrate and covering sidewalls of the first fin-shaped patterns;

a second field insulating film on the substrate and covering sidewalls of the second fin-shaped patterns;

a first source/drain pattern on the first field insulating film, connected to the first fin-shaped patterns, and including a first silicon-germanium pattern; and

a second source/drain pattern on the second field insulating film, connected to the second fin-shaped patterns, and including a second silicon-germanium pattern, the second source/drain pattern and the second field insulating film defining one or more first air gaps therebetween;

wherein the first source/drain pattern includes first bottom surfaces connected to respective ones of the first fin-shaped patterns and one or more first connection surfaces each connecting a corresponding adjacent pair of the first bottom surfaces with each other,

the second source/drain pattern includes second bottom surfaces connected to respective ones of the second fin-shaped patterns and one or more second connection surfaces each connecting a corresponding adjacent pair of the second bottom surfaces to each other,

a number of first air gaps is same as a number of second connection surfaces, and

at least one of the first connection surfaces is in entire contact with an upper surface of the first field insulating film.

2. The semiconductor device of claim 1, wherein the first connection surfaces are in entire contact with the upper surface of the first field insulating film.

3. The semiconductor device of claim 1 or claim 2, wherein

the first source/drain pattern and the first field insulating film define one or more second air gaps therebetween, and

a number of second air gaps is less than a number of first connection surfaces.

4. The semiconductor device of claim 3, wherein a size of the first air gap is greater than a size of the second air gap.

5. The semiconductor device of any one of claims 1 to 4, wherein a number of first fin-shaped patterns is more than a number of second fin-shaped patterns.

6. The semiconductor device of claim 5, wherein the number of first fin-shaped patterns is four or more.

7. The semiconductor device of any one of claims 1 to 6, wherein

the first source/drain pattern includes connection semiconductor regions extending along the upper surface of the first field insulating film, and

the connection semiconductor regions include silicon-germanium.

8. The semiconductor device of any one of claims 1 to 7, wherein

the first field insulating film includes first, second, and third regions, the first, second, and third regions each being between an adjacent pair of the first fin-shaped patterns,

the second region of the first field insulating film is between the first region of the first field insulating film and the third region of the first field insulating film, and

a height of an upper surface of the second region of the first field insulating film is different from a height of an upper surface of the third region of the first field insulating film.

9. The semiconductor device of claim 8, wherein a height of an upper surface of the first region of the first field insulating film is same as the height of the upper surface of the second region of the first field insulating film.

10. The semiconductor device of claim 8, wherein the height of the upper surface of the second region of the first field insulating film is greater than a height of an upper surface of the first region of the first field insulating film, and is smaller than the height of the upper surface of the third region of the first field insulating film.

11. The semiconductor device of claim 8, wherein a height of an upper surface of the first region of the first field insulating film and the height of the upper surface of the third

region of the first field insulating film are smaller than the height of the upper surface of the second region of the first field insulating film.

12. The semiconductor device of claim 8, wherein a height of an upper surface of the first region of the first field insulating film and the height of the upper surface of the third region of the first field insulating film are greater than the height of the upper surface of the second region of the first field insulating film.

13. A semiconductor device comprising:

a plurality of first fin-shaped patterns in a first region of a substrate and spaced apart from each other;

a first field insulating film on the substrate and covering sidewalls of the first fin-shaped patterns; and

a first source/drain pattern on the first field insulating film and connected to the first fin-shaped patterns,

wherein the first source/drain pattern includes a plurality of first epitaxial regions, connection semiconductor regions, and a second epitaxial region, the first epitaxial regions on respective ones of the first fin-shaped patterns, the connection semiconductor regions extending along an upper surface of the first field insulating film and in contact with the first field insulating film, the second epitaxial region being on the first epitaxial regions and the connection semiconductor regions, the second epitaxial region connecting the first epitaxial regions and the connection semiconductor regions to each other,

the first epitaxial regions, the connection semiconductor regions, and the second epitaxial region include silicon-germanium, and

a fraction of germanium in the connection semiconductor regions is smaller than a fraction of germanium in the second epitaxial region,

wherein the first source/drain pattern includes first bottom surfaces connected to respective ones of the first fin-shaped patterns and one or more first connection surfaces each connecting a corresponding adjacent pair of the first bottom surfaces with each other, and

at least one of the first connection surfaces is in entire contact with the upper surface of the first field insulating film,

wherein the semiconductor device further comprises:

a plurality of second fin-shaped patterns in a second region of the substrate and spaced apart from each other;

a second field insulating film on the substrate and covering sidewalls of the second fin-shaped patterns; and

a second source/drain pattern on the second field insulating film, connected to the second fin-shaped patterns, and including a second silicon-germanium pattern, and

wherein the second source/drain pattern and the second field insulating film define one or more air gaps therebetween.

14. The semiconductor device of claim 13, wherein

the first connection surfaces are in entire contact with the upper surface of the first field insulating film.

15. The semiconductor device of claim 13 or claim 14, wherein

the first source/drain pattern and the first field insulating film define an air gap therebetween,

the first field insulating film includes a first region and a second region, the first region and the second region between respective adjacent pairs of the first fin-shaped patterns,

an entirety of an upper surface of the first region of the first field insulating film is in contact with the first source/drain pattern, and

the air gap is between the second region of the first field insulating film and the first source/drain pattern.

16. The semiconductor device of any one of claims 13 to 15, wherein the connection semiconductor regions include a facet.

17. The semiconductor device of any one of claims 13 to 16,

wherein a number of air gaps is one less than a number of second fin-shaped patterns.

18. The semiconductor device of any one of claims 13 to 16, further comprising:

a lower pattern in the second region of the substrate;

a sheet pattern spaced apart from the lower pattern; and

a gate electrode surrounding a circumference of the sheet pattern.

19. A semiconductor device comprising:

a plurality of first fin-shaped patterns in an I/O region of a substrate, the first fin-shaped patterns spaced apart from each other in a first direction;

a plurality of second fin-shaped patterns in a logic region of the substrate, the second fin-shaped patterns spaced apart from each other in a second direction;

a first field insulating film on the substrate and covering sidewalls of the first fin-shaped patterns;

a second field insulating film on the substrate and covering sidewalls of the second fin-shaped patterns;

a first source/drain pattern on the first field insulating film, connected to the first fin-shaped patterns, and including a first silicon-germanium pattern on the first fin-shaped patterns; and

a second source/drain pattern on the second field insulating film, connected to the second fin-shaped patterns, and including a second silicon-germanium pattern, the second source/drain pattern and the second field insulating film defining one or more air gaps,

wherein the first source/drain pattern includes bottom surfaces connected to respective ones of the first fin-shaped patterns and one or more connection surfaces each connecting a corresponding adjacent pair of the bottom surfaces to each other,

a number of first fin-shaped patterns is more than a number of second fin-shaped patterns,

a number of air gaps is one less than the number of second fin-shaped patterns, and

the one or more connection surfaces are in entire contact with upper surface of the first field insulating film.

20. The semiconductor device of claim 19, wherein

the first source/drain pattern includes a connection semiconductor region extending along the upper surface of the first field insulating film, and

a fraction of germanium in the connection semiconductor region is smaller than a fraction of germanium in the first silicon-germanium pattern.