DESCRIPTION

Title of Invention: PLASMA PROCESSING DEVICE, BIAS POWER SUPPLY SYSTEM, AND PLASMA PROCESSING METHOD

Technical Field

[0001] Example embodiments of the present disclosure relate to a plasma processing apparatus, a bias power supply system, and a plasma processing method.

Background Art

[0002] A plasma processing apparatus that processes a substrate using plasma is known. The plasma processing apparatus described in Patent Literature 1 includes a substrate holding electrode and a counter electrode disposed in a chamber, a radio frequency generator, a DC negative pulse generator, and a controller. The radio frequency generator applies a radio frequency power of 50 MHz or higher to the substrate holding electrode. The DC negative pulse generator applies a DC negative pulse voltage to the substrate holding electrode so as to be superimposed on the radio frequency power. The controller controls the radio frequency generator so that the application of the radio frequency power is performed intermittently, and controls the DC negative pulse generator so that the application of the DC negative pulse is performed intermittently in accordance with the on/off timing of the radio frequency power.

Citation List

Patent Literature

[0003] [Patent Literature 1] Japanese Unexamined Patent Application

Summary of Invention

Technical Problem

[0004] The present disclosure provides a technique for suppressing a decrease in energy of ions supplied from plasma to a substrate during application of a voltage pulse.

Solution to Problem

[0005] In one example embodiment, a plasma processing apparatus is provided. The plasma processing apparatus includes a chamber, a substrate support, a plasma generator, and a bias power supply system. The substrate support has a bias electrode. The substrate support is disposed in the chamber. The plasma generator is configured to generate plasma in the chamber. The bias power supply system is electrically coupled to the bias electrode. The bias power supply system is configured to intermittently apply a voltage pulse to the bias electrode to draw ions from the plasma into a substrate on the substrate support. The bias power supply system includes at least one DC power supply, a switching circuit, and a pulse controller. The switching circuit is electrically connected between the bias electrode and the at least one DC power supply. The pulse controller is configured to control the switching circuit. The pulse controller is configured to control the switching circuit to cause the voltage level of the voltage pulse to stepwise reach a target voltage level thereof having a maximum potential difference in the negative direction with respect to a reference potential.

Advantageous Effects of Invention

[0006] According to one example embodiment, a technique for suppressing a decrease in energy of ions supplied from plasma to a substrate during application of a voltage pulse is provided.

Brief Description of Drawings

[0007] [FIG. 1] FIG. 1 is a diagram for explaining an example configuration of a plasma processing system.

[FIG. 2] FIG. 2 is a diagram for explaining an example configuration of a capacitively coupled plasma processing apparatus.

[FIG. 3] FIG. 3 is a diagram schematically illustrating a plasma processing apparatus according to one example embodiment.

[FIG. 4] FIG. 4 is a diagram schematically illustrating a bias power supply system according to one example embodiment.

[FIG. 5] FIG. 5 is an example timing chart related to the bias power supply system according to one example embodiment.

[FIG. 6] FIG. 6 is a diagram schematically illustrating a bias power supply system according to another example embodiment.

[FIG. 7] FIG. 7 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment.

[FIG. 8] FIG. 8 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment.

[FIG. 9] FIG. 9(a) is an example timing chart related to a bias power supply system according to yet another example embodiment, and FIG. 9(b) is a diagram showing an enlarged view of a portion S of the timing chart of FIG. 9(a).

[FIG. 10] FIG. 10 is a diagram schematically illustrating a plasma processing apparatus according to another example embodiment.

[FIG. 11] FIG. 11 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment.

[FIG. 12] FIG. 12 is an example timing chart related to a bias power supply system according to yet another example embodiment.

[FIG. 13] FIG. 13 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment.

[FIG. 14] FIG. 14 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment.

[FIG. 15] FIG. 15 is a diagram schematically illustrating a bias power supply system according to still yet another example embodiment.

[FIG. 16] FIG. 16(a) is an example timing chart related to a bias power supply system according to yet another example embodiment, and FIG. 16(b) is a diagram showing an enlarged view of a portion S of the timing chart of FIG. 16(a).

[FIG. 17] FIG. 17 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment.

[FIG. 18] FIG. 18 is a flowchart of a plasma processing method according to one example embodiment.

[FIG. 19] FIG. 19 is a block diagram of a processing circuit that implements the operations described in the present specification on a computer.

Description of Embodiments

[0008] Hereinafter, various example embodiments will be described in detail with reference to the drawings. In the drawings, the same or equivalent portions are denoted by the same reference signs.

[0009] FIG. 1 is a diagram for explaining an example configuration of a

plasma processing system. In one embodiment, the plasma processing system includes a plasma processing apparatus 1 and a controller 2. The plasma processing system is an example of a substrate processing system, and the plasma processing apparatus 1 is an example of a substrate processing apparatus. The plasma processing apparatus 1 includes a chamber 10, a substrate support 11, and a plasma generator 12. The chamber 10 has an interior space (plasma processing space). The chamber 10 also has at least one gas inlet for supplying at least one process gas into the interior space and at least one gas outlet for discharging gas from the interior space. The gas inlet is connected to a gas supply 20 described later, and the gas outlet is connected to an exhaust system 40 described later. The substrate support 11 is disposed in the interior space and has a substrate support surface for supporting a substrate.

[0010] The plasma generator 12 is configured to generate plasma from at least one process gas supplied into the interior space. The plasma formed in the interior space may be capacitively coupled plasma (CCP), inductively coupled plasma (ICP), electron-cyclotron-resonance plasma (ECR plasma), helicon wave plasma (HWP), surface wave plasma (SWP), or the like. Various types of plasma generators may be used, including an AC (Alternating Current) plasma generator and a DC (Direct Current) plasma generator. In one embodiment, an AC signal (AC power) used in the AC plasma generator has a frequency within a range of 100 kHz to 10 GHz. Accordingly, the AC signal includes an RF (Radio Frequency) signal and a microwave signal. In one embodiment, the RF signal has a frequency within a range of 100 kHz to 150 MHz.

[0011] The controller 2 processes computer-executable instructions that cause the plasma processing apparatus 1 to perform various steps described in the present disclosure. The controller 2 may be configured to control each component of the plasma processing apparatus 1 so as to perform the various steps described herein. In one embodiment, a part or all of the controller 2 may be included in the plasma processing apparatus 1. The controller 2 may include a processor 2a1, a storage 2a2, and a communication interface 2a3. The controller 2 is implemented by, for example, a computer 2a. The processor 2a1 may be configured to perform various control operations by loading a program from the storage 2a2 and executing the loaded program. The program may be prestored in the storage 2a2, or may be obtained through a medium as needed. The obtained program is stored in the storage 2a2, and is loaded from the storage 2a2 by the processor 2a1 and executed. The medium may be any of various storage media readable by the computer 2a, or may be a communication line connected to the communication interface 2a3. The processor 2a1 may be a CPU (Central Processing Unit). The storage 2a2 may include a RAM (Random Access Memory), a ROM (Read Only Memory), an HDD (Hard Disk Drive), an SSD (Solid State Drive), or a combination thereof. The communication interface 2a3 may communicate with the plasma processing apparatus 1 through a communication line such as a LAN (Local Area Network).

[0012] An example configuration of a capacitively coupled plasma processing apparatus as an example of the plasma processing apparatus 1 will now be described. FIG. 2 is a diagram for explaining an example

configuration of the capacitively coupled plasma processing apparatus.

[0013] The capacitively coupled plasma processing apparatus 1 includes the chamber 10, the gas supply 20, a power supply 30, and the exhaust system 40. The plasma processing apparatus 1 also includes the substrate support 11 and a gas introduction unit. The gas introduction unit is configured to introduce at least one process gas into the chamber 10. The gas introduction unit includes a shower head 13. The substrate support 11 is disposed in the chamber 10. The shower head 13 is disposed above the substrate support 11. In one embodiment, the shower head 13 defines at least a part of the ceiling of the chamber 10. The chamber 10 has an interior space 10s defined by the shower head 13, a side wall 10a of the chamber 10, and the substrate support 11. The chamber 10 is grounded. The shower head 13 and the substrate support 11 are electrically insulated from the housing of the chamber 10.

[0014] The substrate support 11 includes a main body 111 and a ring assembly 112. The main body 111 has a substrate support surface 111a (central region) for supporting a substrate W and a ring support surface 111b (annular region) for supporting the ring assembly 112. The ring support surface 111b of the main body 111 surrounds the substrate support surface 111a of the main body 111 in a plan view. The substrate W is disposed on the substrate support surface 111a of the main body 111, and the ring assembly 112 is disposed on the ring support surface 111b of the main body 111 so as to surround the substrate W on the substrate support surface 111a of the main body 111.

[0015] In one embodiment, the main body 111 includes a base 1110 and an electrostatic chuck 1111. The base 1110 includes a conductive

member. The conductive member of the base 1110 can function as a bias electrode. The electrostatic chuck 1111 is disposed on the base 1110. The electrostatic chuck 1111 includes a ceramic member 1111a and an electrostatic electrode 1111b disposed inside the ceramic member 1111a. The ceramic member 1111a has the substrate support surface 111a. In one embodiment, the ceramic member 1111a also has the ring support surface 111b. Note that another member surrounding the electrostatic chuck 1111, such as an annular electrostatic chuck or an annular insulating member, may have the ring support surface 111b. In this case, the ring assembly 112 may be disposed on the annular electrostatic chuck or the annular insulating member, or may be disposed on both the electrostatic chuck 1111 and the annular insulating member. Also, at least one RF/DC electrode coupled to an RF power supply 31 and/or a DC power supply 32 described later may be disposed inside the ceramic member 1111a. In this case, the at least one RF/DC electrode functions as a bias electrode. When a bias RF signal and/or a DC signal described later is supplied to the at least one RF/DC electrode, the RF/DC electrode is also referred to as a bias electrode. Note that the conductive member of the base 1110 and the at least one RF/DC electrode may function as a plurality of bias electrodes. Also, the electrostatic electrode 1111b may function as a bias electrode. Accordingly, the substrate support 11 includes at least one bias electrode.

[0016] The ring assembly 112 includes one or more annular members. In one embodiment, the one or more annular members include one or more edge rings and at least one cover ring. The one or more edge rings are formed from a conductive material or an insulating material, and the

cover ring is formed from an insulating material.

[0017] The substrate support 11 may also include a temperature control module configured to adjust at least one of the electrostatic chuck 1111, the ring assembly 112, and the substrate to a target temperature. The temperature control module may include a heater, a heat transfer medium, a channel 1110a, or a combination thereof. A heat transfer fluid such as brine or gas flows through the channel 1110a. In one embodiment, the channel 1110a is formed in the base 1110, and one or more heaters are disposed in the ceramic member 1111a of the electrostatic chuck 1111. The substrate support 11 may also include a heat transfer gas supply configured to supply a heat transfer gas into a gap between the back surface of the substrate W and the substrate support surface 111a.

[0018] The shower head 13 is configured to introduce at least one process gas from the gas supply 20 into the interior space 10s. The shower head 13 has at least one gas inlet 13a, at least one gas diffusion chamber 13b, and a plurality of gas introduction ports 13c. The process gas supplied to the gas inlet 13a passes through the gas diffusion chamber 13b and is introduced into the interior space 10s through the plurality of gas introduction ports 13c. The shower head 13 also includes at least one upper electrode. Note that the gas introduction unit may include, in addition to the shower head 13, one or more side gas injectors (SGIs) attached to one or more openings formed in the side wall 10a.

[0019] The gas supply 20 may include at least one gas source 21 and at least one flow rate controller 22. In one embodiment, the gas supply 20

is configured to supply at least one process gas from the corresponding gas source 21 to the shower head 13 through the corresponding flow rate controller 22. Each flow rate controller 22 may include, for example, a mass flow controller or a pressure control type flow rate controller. Furthermore, the gas supply 20 may include at least one flow rate modulation device that modulates or pulses the flow rate of at least one process gas.

[0020] The power supply 30 includes an RF power supply 31 coupled to the chamber 10 through at least one impedance matching circuit. The RF power supply 31 is configured to supply at least one RF signal (RF power) to at least one bias electrode and/or at least one upper electrode. This causes plasma to be formed from at least one process gas supplied to the interior space 10s. Accordingly, the RF power supply 31 can function as at least a part of the plasma generator 12. Also, by supplying a bias RF signal to at least one bias electrode, a bias potential is generated in the substrate W, and ionic components in the formed plasma can be drawn into the substrate W.

[0021] In one embodiment, the RF power supply 31 includes a first RF generator 31a and a second RF generator 31b. The first RF generator 31a is coupled to at least one bias electrode and/or at least one upper electrode through at least one impedance matching circuit, and is configured to generate a source RF signal (source RF power) for plasma generation. In one embodiment, the source RF signal has a frequency within a range of 10 MHz to 150 MHz. In one embodiment, the first RF generator 31a may be configured to generate a plurality of source RF signals having different frequencies. The generated one or more source

RF signals are supplied to at least one bias electrode and/or at least one upper electrode.

[0022] The second RF generator 31b is coupled to at least one bias electrode through at least one impedance matching circuit, and is configured to generate a bias RF signal (bias RF power). The frequency of the bias RF signal may be the same as or different from the frequency of the source RF signal. In one embodiment, the bias RF signal has a frequency lower than the frequency of the source RF signal. In one embodiment, the bias RF signal has a frequency within a range of 100 kHz to 60 MHz. In one embodiment, the second RF generator 31b may be configured to generate a plurality of bias RF signals having different frequencies. The generated one or more bias RF signals are supplied to at least one bias electrode. Also, in various embodiments, at least one of the source RF signal and the bias RF signal may be pulsed.

[0023] The power supply 30 may also include a DC power supply 32 coupled to the chamber 10. The DC power supply 32 includes a first DC generator 32a and a second DC generator 32b. In one embodiment, the first DC generator 32a is connected to at least one bias electrode and is configured to generate a first DC signal. The generated first DC signal is applied to at least one bias electrode. In one embodiment, the second DC generator 32b is connected to at least one upper electrode and is configured to generate a second DC signal. The generated second DC signal is applied to at least one upper electrode.

[0024] In various embodiments, the first and second DC signals may be pulsed. In this case, a sequence of voltage pulses is applied to at least one bias electrode and/or at least one upper electrode. The voltage

pulses may have a pulse waveform that is rectangular, trapezoidal, triangular, or a combination thereof. In one embodiment, a waveform generator for generating a sequence of voltage pulses from a DC signal is connected between the first DC generator 32a and at least one bias electrode. Accordingly, the first DC generator 32a and the waveform generator constitute a voltage pulse generator. When the second DC generator 32b and the waveform generator constitute a voltage pulse generator, the voltage pulse generator is connected to at least one upper electrode. The voltage pulses may have a positive polarity or a negative polarity. Also, the sequence of voltage pulses may include one or more positive-polarity voltage pulses and one or more negative-polarity voltage pulses within one cycle. Note that the first DC generator 32a and the second DC generator 32b may be provided in addition to the RF power supply 31, or the first DC generator 32a may be provided in place of the second RF generator 31b.

[0025] The exhaust system 40 can be connected to, for example, a gas outlet 10e provided at the bottom of the chamber 10. The exhaust system 40 may include a pressure control valve and a vacuum pump. The pressure in the interior space 10s is adjusted by the pressure control valve. The vacuum pump may include a turbomolecular pump, a dry pump, or a combination thereof.

[0026] Reference is now made to FIG. 3. FIG. 3 is a diagram schematically illustrating a plasma processing apparatus according to one example embodiment. The substrate support 11, the power supply, and the configuration related to the power supply shown in FIG. 3 can be employed in the plasma processing apparatus 1.

[0027] The plasma processing apparatus 1 includes the substrate support 11. The substrate support 11 is disposed in the chamber 10. The substrate support 11 may include the base 1110 and the electrostatic chuck 1111. The base 1110 can function as a bias electrode BE.

[0028] The substrate support 11 may include a first region R1 and a second region R2. In FIG. 3, the boundary between the first region R1 and the second region R2 is indicated by a dashed line. The first region R1 is a region intersecting an axis AX and has a substantially disk shape. The axis AX is the central axis of the substrate support 11 and can coincide with the central axis of the chamber 10. The first region R1 includes, as an upper surface thereof, the above-described substrate support surface 111a. The second region R2 extends so as to surround the first region R1.

[0029] The substrate W is placed on the substrate support surface 111a and is supported on the first region R1. The second region R2 is an annular region around the axis AX. The second region R2 may include, as an upper surface thereof, the above-described ring support surface 111b. An edge ring ER included in the ring assembly 112 is placed on the ring support surface 111b and is supported on the second region R2. The substrate W is disposed in a region surrounded by the edge ring ER.

[0030] As shown in FIG. 3, the electrostatic chuck 1111 may include a dielectric portion 1111d. The dielectric portion 1111d may be the above-described ceramic member 1111a. The central portion of the dielectric portion 1111d may form the first region R1 and may have the substrate support surface 111a as an upper surface thereof. The peripheral portion of the dielectric portion 1111d may form the second

region R2 and may have the ring support surface 111b as an upper surface thereof.

[0031] The electrostatic chuck 1111 may include, as a part of the electrostatic electrode 1111b, a chuck electrode CE1. The chuck electrode CE1 is disposed inside the dielectric portion 1111d and within the first region R1. The chuck electrode CE1 may be a film formed from a conductive material. The chuck electrode CE1 may have a substantially circular planar shape. The chuck electrode CE1 may be disposed such that a center thereof is located on the axis AX. The chuck electrode CE1 can extend between the substrate support surface 111a and a first bias electrode BE1.

[0032] The electrostatic chuck 1111 may also include, as another part of the electrostatic electrode 1111b, chuck electrodes CE2 and CE3. Each of the chuck electrodes CE2 and CE3 is disposed inside the dielectric portion 1111d and within the second region R2. Each of the chuck electrodes CE2 and CE3 may be a film formed from a conductive material. Each of the chuck electrodes CE2 and CE3 may extend circumferentially around the axis AX and may have a substantially annular planar shape. The chuck electrode CE2 is disposed on the inner side with respect to the chuck electrode CE3. That is, the radial distance between the chuck electrode CE2 and the axis AX is smaller than the radial distance between the chuck electrode CE3 and the axis AX.

[0033] As described above, the plasma processing apparatus 1 further includes the first RF generator 31a. The first RF generator 31a may be electrically connected to the bias electrode BE through a matcher 31am and an electrical path 30p.

[0034] The plasma processing apparatus 1 may further include a DC power supply 41p. The DC power supply 41p is electrically connected to the chuck electrode CE1 through a switch 41s. A filter 41f may be further connected between the DC power supply 41p and the chuck electrode CE1. The filter 41f is a low-pass filter configured to block or attenuate an RF signal such as a source RF signal. When a voltage from the DC power supply 41p is applied to the chuck electrode CE1, an electrostatic attraction force is generated between the electrostatic chuck 1111 and the substrate W. The substrate W is attracted to the first region R1 by the generated electrostatic attraction force and is held by the first region R1.

[0035] The plasma processing apparatus 1 may further include DC power supplies 42p and 43p. The DC power supply 42p is electrically connected to the chuck electrode CE2 through a switch 42s. A filter 42f may be further connected between the DC power supply 42p and the chuck electrode CE2. The filter 42f is a low-pass filter configured to block or attenuate an RF signal such as a source RF signal.

[0036] The DC power supply 43p is electrically connected to the chuck electrode CE3 through a switch 43s. A filter 43f may be further connected between the DC power supply 43p and the chuck electrode CE3. The filter 43f is a low-pass filter configured to block or attenuate an RF signal such as a source RF signal.

[0037] When voltages from the DC power supplies 42p and 43p are applied to the chuck electrodes CE2 and CE3, an electrostatic attraction force is generated between the electrostatic chuck 1111 and the edge ring ER. The edge ring ER is attracted to the second region R2 by the

generated electrostatic attraction force and is held by the second region R2. Note that voltages may be applied to the chuck electrode CE2 and the chuck electrode CE3 such that a potential difference is generated between them. That is, the second region R2 may form a bipolar electrostatic chuck.

[0038] The plasma processing apparatus 1 includes a bias power supply system 50. The bias power supply system 50 is electrically coupled to the bias electrode BE through a filter 301f and an electrical path 30p. The filter 301f is a low-pass filter configured to block or attenuate an RF signal such as a source RF signal. In FIG. 3, the base 1110 forms the bias electrode BE, but the location of the bias electrode BE in the substrate support 11 is not limited. The bias electrode BE may be at least one conductive member of the base 1110. The bias electrode BE may be, for example, at least one electrode inside the electrostatic chuck 1111.

[0039] FIG. 4 is a diagram schematically illustrating a bias power supply system 50 according to one example embodiment. The bias power supply system 50 is configured to intermittently apply a voltage pulse VP (see FIG. 5) to the bias electrode BE in order to draw ions from the plasma into the substrate W on the substrate support 11. The voltage pulse VP may be periodically applied to the bias electrode BE. That is, the voltage pulse VP may be periodically applied at a time interval equal to the duration of the waveform cycle thereof. The bias frequency, which is the reciprocal of the duration of the waveform cycle of the voltage pulse VP, may be lower than the frequency of the source RF signal and may be a frequency within a range of 100 kHz or more and 50 MHz or less. The bias frequency is, for example, 400 kHz.

[0040] As shown in FIG. 4, the bias power supply system 50 includes at least one DC power supply 51, a switching circuit 53, and a pulse controller 54. The switching circuit 53 is electrically connected between the bias electrode BE and the at least one DC power supply 51. The pulse controller 54 is configured to control the switching circuit 53. The pulse controller 54 controls the switching circuit 53 so as to cause the voltage level of the voltage pulse VP to stepwise reach a target voltage level thereof having a maximum potential difference in the negative direction with respect to a reference potential. The reference potential is, for example, ground potential.

[0041] In one embodiment, the bias power supply system 50 may include, as the at least one DC power supply 51, a first DC power supply 511 and a second DC power supply 512, as shown in FIG. 4. The first DC power supply 511 is capable of outputting an output voltage having a potential difference smaller than the above-described target voltage level with respect to the reference potential. The second DC power supply 512 is capable of outputting an output voltage having the target voltage level. Each of the first DC power supply 511 and the second DC power supply 512 may be a variable DC power supply. The positive terminal of the first DC power supply 511 is connected to ground. The positive terminal of the second DC power supply 512 is connected to ground.

[0042] In one embodiment, the switching circuit 53 may include a first switching element SW1, a second switching element SW2, and a switching element SWG.

[0043] The first switching element SW1 is electrically connected between the negative terminal of the first DC power supply 511 and the

bias electrode BE. The first switching element SW1 is electrically connected to the bias electrode BE through an electrical path 53p. When the first switching element SW1 is closed, the first DC power supply 511 and the bias electrode BE are in a conductive state, and when the first switching element SW1 is open, the first DC power supply 511 and the bias electrode BE are in a non-conductive state.

[0044] The second switching element SW2 is electrically connected between the negative terminal of the second DC power supply 512 and the bias electrode BE. The second switching element SW2 is electrically connected to the bias electrode BE through the electrical path 53p. When the second switching element SW2 is closed, the second DC power supply 512 and the bias electrode BE are in a conductive state, and when the second switching element SW2 is open, the second DC power supply 512 and the bias electrode BE are in a non-conductive state.

[0045] The switching element SWG is electrically connected between ground and the bias electrode BE. The switching element SWG is electrically connected to the bias electrode BE through the electrical path 53p. When the switching element SWG is closed, ground and the bias electrode BE are in a conductive state, and when the switching element SWG is open, ground and the bias electrode BE are in a non-conductive state.

[0046] The pulse controller 54 is electrically connected to the first switching element SW1, the second switching element SW2, and the switching element SWG of the switching circuit 53. The pulse controller 54 can switch the open/closed states of the first switching

element SW1, the second switching element SW2, and the switching element SWG by providing pulse control signals to them. The pulse controller 54 may be implemented by a processing circuit described later.

[0047] The pulse controller 54 is configured to control the switching circuit 53 so as to, in the application of the voltage pulse VP to the bias electrode BE, set the first switching element SW1 to a closed state and set the second switching element SW2 to an open state, and then set the second switching element SW2 to a closed state and set the first switching element SW1 to an open state.

[0048] An example of the operation of the pulse controller 54 will now be described. FIG. 5 is an example timing chart related to the bias power supply system according to one example embodiment. In FIG. 5, the horizontal axis represents time. In FIG. 5, the vertical axis represents the state of each of the first switching element SW1, the second switching element SW2, and the switching element SWG, and the voltage level of the voltage pulse VP. In FIG. 5, the reference potential for the voltage level of the voltage pulse VP is ground potential.

[0049] Each of the first switching element SW1, the second switching element SW2, and the switching element SWG is in a closed state during the period corresponding to "On" shown in FIG. 5. Each of the first switching element SW1, the second switching element SW2, and the switching element SWG is in an open state during the period corresponding to "Off" shown in FIG. 5.

[0050] As shown in FIG. 5, the pulse controller 54 may be configured to periodically apply the voltage pulse VP to the bias electrode BE. The

waveform cycle of the voltage pulse VP includes a first period T1 and a second period T2. In the first period T1, the pulse controller 54 controls the switching circuit 53 so as to cause the voltage level of the voltage pulse VP to stepwise reach the target voltage level thereof having the maximum potential difference in the negative direction with respect to the reference potential. In the second period T2, the level of the output voltage of the bias power supply system 50 is set to the reference potential level (e.g., ground potential).

[0051] In one embodiment, the first period T1 includes a period T11 and a period T12. The period T12 is a period following the period T11. In the period T11, the pulse controller 54 sets the first switching element SW1 to a closed state and sets the second switching element SW2 to an open state. Also, in the period T11, the pulse controller 54 sets the switching element SWG to an open state. In the period T11, the bias electrode BE is connected to the negative terminal of the first DC power supply 511, and the output voltage of the first DC power supply 511 is applied to the bias electrode BE. As a result, in the period T11, the voltage level of the voltage pulse VP reaches a first voltage level V1, which is the voltage level of the output voltage of the first DC power supply 511.

[0052] Next, in the period T12, the pulse controller 54 sets the second switching element SW2 to a closed state and sets the first switching element SW1 to an open state. In the period T12, the pulse controller 54 sets the switching element SWG to an open state. In the period T12, the bias electrode BE is connected to the negative terminal of the second DC power supply 512, and the output voltage of the second DC power

supply 512 is applied to the bias electrode BE. As a result, in the period T12, the voltage level of the voltage pulse VP reaches a second voltage level V2, which is the voltage level of the output voltage of the second DC power supply 512, that is, the above-described target voltage level.

[0053] Accordingly, in the first period T1, the voltage level of the voltage pulse VP reaches the above-described target voltage level in two steps.

[0054] Next, in the second period T2, the pulse controller 54 sets the first switching element SW1 and the second switching element SW2 to an open state. The pulse controller 54 may set the switching element SWG to a closed state in the second period T2.

[0055] In the plasma processing apparatus 1 described above, the voltage level of the voltage pulse VP stepwise reaches the target voltage level. Accordingly, even if the substrate W is charged by ions from the plasma during the application of the voltage pulse VP to the bias electrode BE, a decrease in the potential difference between the potential of the substrate W and the plasma is suppressed. Therefore, according to the plasma processing apparatus 1, even if the substrate W is charged during the application of the voltage pulse VP to the bias electrode BE, a decrease in the energy of ions supplied from the plasma to the substrate W is suppressed.

[0056] Reference is now made to FIG. 6. FIG. 6 is a diagram schematically illustrating a bias power supply system according to another example embodiment. A bias power supply system 50A shown in FIG. 6 can be employed in the plasma processing apparatus 1 in place of the bias power supply system 50. In the bias power supply system

50A, the positive terminal of the second DC power supply 512 is floating from ground and is connected to the negative terminal of the first DC power supply 511. Other configurations of the bias power supply system 50A are the same as the corresponding configurations of the bias power supply system 50. Also, the control of the switching circuit 53 by the pulse controller 54 in the bias power supply system 50A is the same as the control of the switching circuit 53 by the pulse controller 54 in the bias power supply system 50.

[0057] In the bias power supply system 50A, the voltage level of the output voltage from the second DC power supply 512 is the sum of the voltage level of the output voltage of the first DC power supply 511 and the potential difference between the positive terminal and the negative terminal of the second DC power supply 512. Accordingly, it is possible to use a DC power supply having a relatively small maximum output voltage level as the second DC power supply 512.

[0058] Reference is now made to FIG. 7. FIG. 7 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment. A bias power supply system 50B shown in FIG. 7 can be employed in the plasma processing apparatus 1 in place of the bias power supply system 50. In the bias power supply system 50B, the first DC power supply 511 includes a plurality of DC power supplies connected in series. Also, in the bias power supply system 50B, the second DC power supply 512 is constituted by the plurality of DC power supplies of the first DC power supply 511 and a plurality of DC power supplies connected in series with the first DC power supply 511. Other configurations of the bias power supply system 50B are the same

as the corresponding configurations of the bias power supply system 50A. Also, the control of the switching circuit 53 by the pulse controller 54 in the bias power supply system 50B is the same as the control of the switching circuit 53 by the pulse controller 54 in the bias power supply system 50.

[0059] Reference is now made to FIG. 8. FIG. 8 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment. A bias power supply system 50C shown in FIG. 8 can be employed in the plasma processing apparatus 1 in place of the bias power supply system 50. The bias power supply system 50C will now be described focusing on differences from the bias power supply system 50.

[0060] The bias power supply system 50C includes a DC power supply 51C, a switching circuit 53C, and a pulse controller 54C. The DC power supply 51C may be a single DC power supply in the bias power supply system 50C. The DC power supply 51C is capable of outputting an output voltage having the target voltage level of the voltage pulse VP (see FIG. 9(a)). The DC power supply 51C may be a variable DC power supply. The positive terminal of the DC power supply 51C may be connected to ground. The negative terminal of the DC power supply 51C is connected to the switching circuit 53C.

[0061] The switching circuit 53C includes a switching element SWC and a switching element SWG.

[0062] The switching element SWC is electrically connected between the negative terminal of the DC power supply 51C and the bias electrode BE. When the switching element SWC is closed, the DC power supply

51C and the bias electrode BE are in a conductive state, and when the switching element SWC is open, the DC power supply 51C and the bias electrode BE are in a non-conductive state.

[0063] The switching element SWG is electrically connected between ground and the bias electrode BE. When the switching element SWG is closed, ground and the bias electrode BE are in a conductive state, and when the switching element SWG is open, ground and the bias electrode BE are in a non-conductive state.

[0064] The pulse controller 54C is configured to control the switching circuit 53C. The pulse controller 54C is configured to control the switching circuit 53C so as to cause the voltage level of the voltage pulse VP to stepwise reach the target voltage level thereof having a maximum potential difference in the negative direction with respect to the reference potential. The pulse controller 54C is configured to control the switching circuit 53C so as to alternately repeat opening and closing of the switching element SWC in the application of the voltage pulse VP to the bias electrode BE.

[0065] An example of the operation of the pulse controller 54C will now be described. FIG. 9(a) is an example timing chart related to a bias power supply system according to yet another example embodiment. FIG. 9(b) is a diagram showing an enlarged view of a portion S of the timing chart of FIG. 9(a). In FIG. 9(a) and FIG. 9(b), the horizontal axis represents time. In FIG. 9(a), the vertical axis represents the state of each of the switching element SWC and the switching element SWG and the voltage level of the voltage pulse VP. In FIG. 9, the reference potential of the voltage level of the voltage pulse VP is ground potential.

[0066] As shown in FIG. 9(a) and FIG. 9(b), the pulse controller 54C may be configured to periodically apply the voltage pulse VP to the bias electrode BE. The waveform cycle of the voltage pulse VP includes a first period T1C and a second period T2C. The second period T2C is a period following the first period T1C. In the first period T1C, the pulse controller 54C controls the switching circuit 53C so as to cause the voltage level of the voltage pulse VP to stepwise reach the above-described target voltage level. In the second period T2C, the level of the output voltage of the bias power supply system 50C is set to the reference potential level (e.g., ground potential).

[0067] In the first period T1C, the pulse controller 54C sets the switching element SWG to an open state. In the illustrated example, the first period T1C includes periods T11a to T14b. The duration of each of the periods T11a to T14b may be predetermined.

[0068] The period T11a is the first sub-period within the first period T1C. In the period T11a, the pulse controller 54C sets the switching element SWC to a closed state. In the period T11a, the voltage level of the voltage pulse VP reaches a first voltage level VC1. In the subsequent period T11b, the pulse controller 54C sets the switching element SWC to an open state. In the period T11b, the bias electrode BE is floating from ground.

[0069] In the subsequent period T12a, the pulse controller 54C sets the switching element SWC to a closed state. In the period T12a, the voltage level of the voltage pulse VP reaches a second voltage level VC2. The difference between the second voltage level VC2 and the reference potential is equal to or greater than the difference between the

first voltage level VC1 and the reference potential. In the subsequent period T12b, the pulse controller 54C sets the switching element SWC to an open state. In the period T12b, the bias electrode BE is floating from ground.

[0070] In the subsequent period T13a, the pulse controller 54C sets the switching element SWC to a closed state. In the period T13a, the voltage level of the voltage pulse VP reaches a third voltage level VC3. The difference between the third voltage level VC3 and the reference potential is equal to or greater than the difference between the second voltage level VC2 and the reference potential. In the period T13b, the pulse controller 54C sets the switching element SWC to an open state. In the period T13b, the bias electrode BE is floating from ground.

[0071] In the subsequent period T14a, the pulse controller 54C sets the switching element SWC to a closed state. In the period T14a, the voltage level of the voltage pulse VP reaches a fourth voltage level VC4. The difference between the fourth voltage level VC4 and the reference potential is equal to or greater than the difference between the third voltage level VC3 and the reference potential. In the example shown in FIG. 9(a), the fourth voltage level VC4 is the target voltage level having a maximum potential difference in the negative direction with respect to the reference potential in the voltage pulse VP. In the subsequent period T14b, the pulse controller 54C sets the switching element SWC to an open state. In the period T14b, the bias electrode BE is floating from ground.

[0072] As shown in FIG. 9(a), in the first period T1C, the voltage level of the voltage pulse VP reaches the above-described target voltage level

in four steps. Note that the number of steps for the voltage pulse VP to reach the target voltage level in the first period T1C is not limited to four steps.

[0073] In the second period T2C following the first period T1C, the pulse controller 54C sets the switching element SWC to an open state. In the second period T2C, the pulse controller 54C may set the switching element SWG to a closed state.

[0074] According to the bias power supply system 50C, a single DC power supply 51C can be used, and the number of switching elements in the switching circuit 53 is reduced. Accordingly, the bias power supply system 50C has a simpler structure.

[0075] Reference is now made to FIG. 10. FIG. 10 is a diagram schematically illustrating a plasma processing apparatus 101 according to another example embodiment. The plasma processing apparatus 101 shown in FIG. 10 will now be described focusing on differences from the plasma processing apparatus 1.

[0076] As shown in FIG. 10, the substrate support 11 of the plasma processing apparatus 101 further includes a first bias electrode BE1 and a second bias electrode BE2. The first bias electrode BE1 extends below the substrate support surface 111a and is disposed within the first region R1. The first bias electrode BE1 is electrically coupled to the substrate W on the substrate support surface 111a. In the example shown in FIG. 10, the first bias electrode BE1 is disposed inside the dielectric portion 1111d and within the first region R1. The first bias electrode BE1 may be a film formed from a conductive material. The first bias electrode BE1 may have a substantially circular planar shape. The first bias

electrode BE1 may be disposed such that the center thereof is located on the axis AX. The above-described chuck electrode CE1 can extend between the substrate support surface 111a and the first bias electrode BE1. Note that the chuck electrode CE1 may be used as the first bias electrode BE1.

[0077] The second bias electrode BE2 is an electrode separate from the first bias electrode BE1. The second bias electrode BE2 extends below the ring support surface 111b and is disposed within the second region R2. The second bias electrode BE2 is electrically coupled to the edge ring ER. The edge ring ER is placed on the ring support surface 111b so as to surround the substrate W. In the example shown in FIG. 10, the second bias electrode BE2 is disposed inside the dielectric portion 1111d and within the second region R2. The second bias electrode BE2 may be a film formed from a conductive material. The second bias electrode BE2 may have a substantially annular planar shape. The second bias electrode BE2 may be disposed such that the center thereof is located on the axis AX. Each of the above-described chuck electrodes CE2 and CE3 can extend between the ring support surface 111b and the second bias electrode BE2. Note that the chuck electrodes CE2 and CE3 may be used as the second bias electrode BE2.

[0078] The plasma processing apparatus 101 includes a bias power supply system 50D. The bias power supply system 50D is electrically coupled to the first bias electrode BE1 through an electrical path 301p. The bias power supply system 50D is electrically coupled to the second bias electrode BE2 through an electrical path 302p.

[0079] The bias power supply system 50D intermittently or periodically

applies a first voltage pulse VP1 to the first bias electrode BE1. The bias power supply system 50D intermittently or periodically applies a second voltage pulse VP2 to the second bias electrode BE2.

[0080] FIG. 11 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment. As shown in FIG. 11, the bias power supply system 50D includes a first DC power supply 511D, a second DC power supply 512D, a third DC power supply 513D, a fourth DC power supply 514D, a first switching circuit 531D, and a second switching circuit 532D. The first switching circuit 531D and the second switching circuit 532D may be configured as a single switching circuit.

[0081] The first DC power supply 511D is capable of outputting an output voltage having a potential difference smaller than a first target voltage level with respect to the reference potential. The first target voltage level is the voltage level that the first voltage pulse VP1 finally reaches. The second DC power supply 512D is capable of outputting an output voltage having the first target voltage level. The third DC power supply 513D is capable of outputting an output voltage having a potential difference smaller than a second target voltage level with respect to the reference potential. The second target voltage level is the voltage level that the second voltage pulse VP2 finally reaches. The fourth DC power supply 514D is capable of outputting an output voltage having the second target voltage level. Each of the first DC power supply 511D, the second DC power supply 512D, the third DC power supply 513D, and the fourth DC power supply 514D may be a variable DC power supply. The positive terminal of each of the first DC power

supply 511D, the second DC power supply 512D, the third DC power supply 513D, and the fourth DC power supply 514D is connected to ground.

[0082] The first switching circuit 531D is electrically connected between the first bias electrode BE1 and each of the first DC power supply 511D and the second DC power supply 512D. A filter 301f (see FIG. 10) may be connected between the first switching circuit 531D and the first bias electrode BE1. The filter 301f is configured to block or attenuate a high-frequency signal such as a source RF signal. The first switching circuit 531D may include a first switching element SW1, a second switching element SW2, and a switching element SWG1.

[0083] The first switching element SW1 is electrically connected between the negative terminal of the first DC power supply 511D and the first bias electrode BE1. The second switching element SW2 is electrically connected between the negative terminal of the second DC power supply 512D and the first bias electrode BE1. The switching element SWG1 is electrically connected between ground and the first bias electrode BE1.

[0084] The second switching circuit 532D is electrically connected between the second bias electrode BE2 and each of the third DC power supply 513D and the fourth DC power supply 514D. A filter 302f (see FIG. 10) may be connected between the second switching circuit 532D and the second bias electrode BE2. The filter 302f is configured to block or attenuate a high-frequency signal such as a source RF signal. The second switching circuit 532D may include a third switching element SW3, a fourth switching element SW4, and a switching element SWG2.

[0085] The third switching element SW3 is electrically connected between the negative terminal of the third DC power supply 513D and the second bias electrode BE2. The fourth switching element SW4 is electrically connected between the negative terminal of the fourth DC power supply 514D and the second bias electrode BE2. The switching element SWG2 is electrically connected between ground and the second bias electrode BE2.

[0086] The pulse controller 54D is electrically connected to the first switching element SW1, the second switching element SW2, the third switching element SW3, the fourth switching element SW4, the switching element SWG1, and the switching element SWG2. The pulse controller 54D provides pulse control signals to the first switching element SW1, the second switching element SW2, the third switching element SW3, the fourth switching element SW4, the switching element SWG1, and the switching element SWG2. This allows the pulse controller 54D to switch the open/closed states of these switching elements.

[0087] The pulse controller 54D is configured to control the first switching circuit 531D so as to cause the voltage level of the first voltage pulse VP1 to be applied to the first bias electrode BE1 to stepwise reach the first target voltage level thereof having a maximum potential difference in the negative direction with respect to the reference potential.

[0088] The pulse controller 54D is configured to control the second switching circuit 532D so as to cause the voltage level of the second voltage pulse VP2 to be applied to the second bias electrode BE2 to

stepwise reach the second target voltage level thereof having a maximum potential difference in the negative direction with respect to the reference potential.

[0089] The pulse controller 54D is configured to control the first switching circuit 531D so as to, in the application of the first voltage pulse VP1, set the first switching element SW1 to a closed state and set the second switching element SW2 to an open state, and then set the second switching element SW2 to a closed state and set the first switching element SW1 to an open state.

[0090] The pulse controller 54D is configured to control the second switching circuit 532D so as to, in the application of the second voltage pulse VP2, set the third switching element SW3 to a closed state and set the fourth switching element SW4 to an open state, and then set the fourth switching element SW4 to a closed state and set the third switching element SW3 to an open state.

[0091] An example of the operation of the pulse controller 54D will now be described. FIG. 12 is an example timing chart related to a bias power supply system according to yet another example embodiment. In FIG. 12, the horizontal axis represents time. In FIG. 12, the vertical axis represents the state of each of the first switching element SW1, the second switching element SW2, the third switching element SW3, the fourth switching element SW4, the switching element SWG1, and the switching element SWG2, and the voltage level of each of the first and second voltage pulses. In FIG. 12, the reference potential for each of the first and second voltage pulses is ground potential.

[0092] Each of the first switching element SW1, the second switching

element SW2, the third switching element SW3, the fourth switching element SW4, the switching element SWG1, and the switching element SWG2 is in a closed state during the period corresponding to "On" shown in FIG. 12. Each of the first switching element SW1, the second switching element SW2, the third switching element SW3, the fourth switching element SW4, the switching element SWG1, and the switching element SWG2 is in an open state during the period corresponding to "Off" shown in FIG. 12.

[0093] As shown in FIG. 12, the pulse controller 54D may be configured to periodically generate the first and second voltage pulses. The common waveform cycle of the first voltage pulse VP1 and the second voltage pulse VP2 includes a first period T1 and a second period T2. In the first period T1, the pulse controller 54D controls the first switching circuit 531D so as to cause the voltage level of the first voltage pulse VP1 to stepwise reach the first target voltage level thereof having a maximum potential difference in the negative direction with respect to the reference potential. Also, in the first period T1, the pulse controller 54D controls the second switching circuit 532D so as to cause the voltage level of the second voltage pulse VP2 to stepwise reach the second target voltage level thereof having a maximum potential difference in the negative direction with respect to the reference potential. In the second period T2 following the first period T1, the level of the output voltage of the bias power supply system 50D is set to the reference potential level (e.g., ground potential).

[0094] The first period T1 includes a period T11 and a period T12. The period T12 is a period following the period T11. In the period T11, the

pulse controller 54D sets the first switching element SW1 to a closed state and sets the second switching element SW2 to an open state. In the period T11, the pulse controller 54D sets the switching element SWG1 to an open state. In the period T11, the voltage level of the first voltage pulse VP1 reaches a first voltage level VD1, which is the voltage level of the output voltage of the first DC power supply 511D.

[0095] In the period T11, the pulse controller 54D sets the third switching element SW3 to a closed state and sets the fourth switching element SW4 to an open state. In the period T11, the pulse controller 54D sets the switching element SWG2 to an open state. In the period T11, the voltage level of the second voltage pulse VP2 reaches a third voltage level VD3, which is the voltage level of the output voltage of the third DC power supply 513D.

[0096] Next, in the period T12, the pulse controller 54D sets the second switching element SW2 to a closed state and sets the first switching element SW1 to an open state. In the period T12, the pulse controller 54D sets the switching element SWG1 to an open state. In the period T12, the voltage level of the first voltage pulse VP1 reaches a second voltage level VD2, which is the voltage level of the output voltage of the second DC power supply 512D, that is, the above-described first target voltage level.

[0097] Also, in the period T12, the pulse controller 54D sets the fourth switching element SW4 to a closed state and sets the third switching element SW3 to an open state. In the period T12, the pulse controller 54D sets the switching element SWG2 to an open state. In the period T12, the voltage level of the second voltage pulse VP2 reaches a fourth

voltage level VD4, which is the voltage level of the output voltage of the fourth DC power supply 514D, that is, the above-described second target voltage level.

[0098] Accordingly, as shown in FIG. 12, in the first period T1, the voltage level of each of the first voltage pulse VP1 and the second voltage pulse VP2 reaches its target voltage level in two steps.

[0099] Next, in the second period T2, the pulse controller 54D sets the first switching element SW1, the second switching element SW2, the third switching element SW3, and the fourth switching element SW4 to an open state. The pulse controller 54D may set the switching element SWG1 and the switching element SWG2 to a closed state in the second period T2.

[0100] According to the plasma processing apparatus 101, voltage pulses synchronized with each other can be applied to both the substrate W and the edge ring ER. Also, the potential difference of the target voltage level of the second voltage pulse VP2 with respect to the reference potential can be increased in accordance with the amount of wear of the edge ring ER. This allows the thickness of the sheath on the edge ring ER to be adjusted relative to the thickness of the sheath on the substrate W, and the direction of travel of ions supplied from the plasma to the edge of the substrate W to be corrected to the vertical direction. Also, this makes it possible to extend the replacement life of the edge ring ER.

[0101] Reference is now made to FIG. 13. FIG. 13 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment. A bias power supply system 50E shown

in FIG. 13 can be employed in the plasma processing apparatus 101 in place of the bias power supply system 50D.

[0102] In the bias power supply system 50E, the positive terminal of the second DC power supply 512D is floating from ground and is electrically connected to the negative terminal of the first DC power supply 511D. The positive terminal of the fourth DC power supply 514D is floating from ground and is electrically connected to the negative terminal of the third DC power supply 513D. The positive terminal of the third DC power supply 513D may be floating from ground and may be electrically connected to the negative terminal of the first DC power supply 511D. Alternatively, the positive terminal of the third DC power supply 513D may be connected to ground. Other configurations of the bias power supply system 50E are the same as the corresponding configurations of the bias power supply system 50D. Also, the control of the first switching circuit 531D and the second switching circuit 532D by the pulse controller 54D in the bias power supply system 50E is the same as the control of the first switching circuit 531D and the second switching circuit 532D by the pulse controller 54D in the bias power supply system 50D.

[0103] According to the bias power supply system 50E, it is possible to use a DC power supply having a relatively small maximum output voltage level as each of the second DC power supply 512D and the fourth DC power supply 514D. Also, when the positive terminal of the third DC power supply 513D is floating from ground and is electrically connected to the negative terminal of the first DC power supply 511D, it is possible to use a DC power supply having a relatively small maximum

output voltage level as the third DC power supply 513D.

[0104] Reference is now made to FIG. 14. FIG. 14 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment. A bias power supply system 50F shown in FIG. 14 can be employed in the plasma processing apparatus 101 in place of the bias power supply system 50D. In the bias power supply system 50F, the first DC power supply 511D includes a plurality of DC power supplies connected in series. Also, in the bias power supply system 50F, the second DC power supply 512D includes the plurality of DC power supplies of the first DC power supply 511D and a plurality of DC power supplies connected in series with the first DC power supply 511D. Also, in the bias power supply system 50F, the third DC power supply 513D includes a plurality of DC power supplies connected in series. Also, in the bias power supply system 50F, the fourth DC power supply 514D includes the plurality of DC power supplies of the third DC power supply 513D and a plurality of DC power supplies connected in series with the third DC power supply 513D. Other configurations of the bias power supply system 50F are the same as the corresponding configurations of the bias power supply system 50E. Also, the control of the first switching circuit 531D and the second switching circuit 532D by the pulse controller 54D in the bias power supply system 50F is the same as the control of the first switching circuit 531D and the second switching circuit 532D by the pulse controller 54D in the bias power supply system 50D.

[0105] Reference is now made to FIG. 15. FIG. 15 is a diagram schematically illustrating a bias power supply system according to yet

another example embodiment. A bias power supply system 50G shown in FIG. 15 can be employed in the plasma processing apparatus 101 in place of the bias power supply system 50D. The bias power supply system 50G will now be described focusing on differences from the bias power supply system 50D.

[0106] The bias power supply system 50G includes, as at least one DC power supply, a first DC power supply 511G and a second DC power supply 512G. The bias power supply system 50G further includes a first switching circuit 531G and a second switching circuit 532G. The first switching circuit 531G and the second switching circuit 532G may be configured as a single switching circuit. The bias power supply system 50G further includes a pulse controller 54G.

[0107] The first DC power supply 511G is capable of outputting an output voltage having the first target voltage level of the first voltage pulse VP1 (see FIG. 16(a)). The second DC power supply 512G is capable of outputting an output voltage having the second target voltage level of the second voltage pulse VP2 (see FIG. 16(a)). The positive terminal of the first DC power supply 511G and the positive terminal of the second DC power supply 512G may be connected to ground. The negative terminal of the first DC power supply 511G is connected to the first switching circuit 531G, and the negative terminal of the second DC power supply 512G is connected to the second switching circuit 532G.

[0108] The first switching circuit 531G includes a first switching element SW1 and a switching element SWG1. The first switching element SW1 is electrically connected between the negative terminal of the first DC power supply 511G and the first bias electrode BE1. The

switching element SWG1 is connected between the first bias electrode BE1 and ground. The second switching circuit 532G includes a second switching element SW2 and a switching element SWG2. The second switching element SW2 is electrically connected between the negative terminal of the second DC power supply 512G and the second bias electrode BE2. The switching element SWG2 is connected between the second bias electrode BE2 and ground.

[0109] The pulse controller 54G is configured to control the first switching circuit 531G and the second switching circuit 532G. The pulse controller 54G is configured to control the first switching circuit 531G so as to cause the voltage level of the first voltage pulse VP1 to stepwise reach the first target voltage level thereof having a maximum potential difference in the negative direction with respect to the reference potential. The pulse controller 54G is configured to control the second switching circuit 532G so as to cause the voltage level of the second voltage pulse VP2 to stepwise reach the target voltage level having a maximum potential difference in the negative direction with respect to the reference potential.

[0110] The pulse controller 54G is configured to control the first switching circuit 531G so as to alternately repeat opening and closing of the first switching element SW1 in the application of the first voltage pulse VP1 to the first bias electrode BE1. Also, the pulse controller 54G is configured to control the second switching circuit 532G so as to alternately repeat opening and closing of the second switching element SW2 in the application of the second voltage pulse VP2 to the second bias electrode BE2.

[0111] An example of the operation of the pulse controller 54G will now be described. FIG. 16(a) is an example timing chart related to a bias power supply system according to yet another example embodiment. FIG. 16(b) is a diagram showing an enlarged view of a portion S of FIG. 16(a). In FIG. 16(a), the vertical axis represents the state of each of the first switching element SW1, the second switching element SW2, the switching element SWG1, and the switching element SWG2, and the voltage level of each of the first voltage pulse VP1 and the second voltage pulse VP2.

[0112] As shown in FIG. 16(a), the pulse controller 54G may be configured to periodically apply the first voltage pulse VP1 and the second voltage pulse VP2 to the first bias electrode BE1 and the second bias electrode BE2, respectively. The waveform cycle of the first voltage pulse VP1 and the second voltage pulse VP2 includes a first period T1G and a second period T2G. In the first period T1G, the pulse controller 54G controls the first switching circuit 531G so as to cause the voltage level of the first voltage pulse VP1 to stepwise reach the first target voltage level. Also, in the first period T1G, the pulse controller 54G controls the second switching circuit 532G so as to cause the voltage level of the second voltage pulse VP2 to stepwise reach the second target voltage level. In the second period T2G, the pulse controller 54G sets the level of the output voltage from the bias power supply system 50G to the first bias electrode BE1 to the reference potential level (e.g., ground potential). Also, in the second period T2G, the pulse controller 54G sets the level of the output voltage from the bias power supply system 50G to the second bias electrode BE2 to the

reference potential level (e.g., ground potential).

[0113] In the first period T1G, the pulse controller 54G sets the switching element SWG1 and the switching element SWG2 to an open state. In the illustrated example, the first period T1G includes periods T11a to T14b. The duration of each of the periods T11a to T14b may be predetermined.

[0114] The period T11a is the first sub-period within the first period T1G. In the period T11a, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to a closed state. In the period T11a, the voltage level of the first voltage pulse VP1 reaches a first voltage level VG1, and the voltage level of the second voltage pulse VP2 reaches a fifth voltage level VG5. In the subsequent period T11b, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to an open state. In the period T11b, the first bias electrode BE1 and the second bias electrode BE2 are floating from ground.

[0115] In the subsequent period T12a, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to a closed state. In the period T12a, the voltage level of the first voltage pulse VP1 reaches a second voltage level VG2, and the voltage level of the second voltage pulse VP2 reaches a sixth voltage level VG6. The difference between the second voltage level VG2 and the reference potential is equal to or greater than the difference between the first voltage level VG1 and the reference potential, and the difference between the sixth voltage level VG6 and the reference potential is equal to or greater than the difference between the fifth voltage level VG5 and

the reference potential. In the subsequent period T12b, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to an open state. In the period T12b, the first bias electrode BE1 and the second bias electrode BE2 are floating from ground.

[0116] In the subsequent period T13a, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to a closed state. In the period T13a, the voltage level of the first voltage pulse VP1 reaches a third voltage level VG3, and the voltage level of the second voltage pulse VP2 reaches a seventh voltage level VG7. The difference between the third voltage level VG3 and the reference potential is equal to or greater than the difference between the second voltage level VG2 and the reference potential, and the difference between the seventh voltage level VG7 and the reference potential is equal to or greater than the difference between the sixth voltage level VG6 and the reference potential. In the subsequent period T13b, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to an open state. In the period T13b, the first bias electrode BE1 and the second bias electrode BE2 are floating from ground.

[0117] In the subsequent period T14a, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to a closed state. In the period T14a, the voltage level of the first voltage pulse VP1 reaches a fourth voltage level VG4, that is, the first target voltage level, and the voltage level of the second voltage pulse VP2 reaches an eighth voltage level VG8, that is, the second target voltage

level. The difference between the fourth voltage level VG4, that is, the first target voltage level, and the reference potential is equal to or greater than the difference between the third voltage level VG3 and the reference potential, and the difference between the eighth voltage level VG8, that is, the second target voltage level, and the reference potential is equal to or greater than the difference between the seventh voltage level VG7 and the reference potential. In the subsequent period T14b, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to an open state. In the period T14b, the first bias electrode BE1 and the second bias electrode BE2 are floating from ground.

[0118] As shown in FIG. 16(a), in the first period T1G, the voltage levels of the first voltage pulse VP1 and the second voltage pulse VP2 reach the first target voltage level and the second target voltage level, respectively, in four steps. Note that the number of steps for each of the first voltage pulse VP1 and the second voltage pulse VP2 to reach its target voltage level in the first period T1G is not limited to four steps.

[0119] In the second period T2G following the first period T1G, the pulse controller 54G sets the first switching element SW1 and the second switching element SW2 to an open state. Also, in the second period T2G, the pulse controller 54G may set the switching element SWG1 and the switching element SWG2 to a closed state.

[0120] Reference is now made to FIG. 17. FIG. 17 is a diagram schematically illustrating a bias power supply system according to yet another example embodiment. A bias power supply system 50H shown in FIG. 17 can be employed in the plasma processing apparatus 101 in

place of the bias power supply system 50D. The bias power supply system 50H will now be described focusing on differences from the bias power supply system 50G.

[0121] In the bias power supply system 50H, the positive terminal of the second DC power supply 512G is floating from ground and is connected to the negative terminal of the first DC power supply 511G. Other configurations of the bias power supply system 50H are the same as the corresponding configurations of the bias power supply system 50G. According to the bias power supply system 50H, it is possible to use a DC power supply having a relatively small maximum output voltage level as the second DC power supply 512G.

[0122] A plasma processing method according to one example embodiment will now be described in detail with reference to FIG. 18. FIG. 18 is a flowchart of a plasma processing method according to one example embodiment. The plasma processing method shown in FIG. 18 (hereinafter referred to as "method MT1") can be performed using the plasma processing apparatus 1 or the plasma processing apparatus 101. In each operation of the method MT1, each part of the plasma processing apparatus can be controlled by the controller 2 and/or the above-described pulse controller.

[0123] The method MT1 starts with operation STa. In operation STa, a substrate W is prepared. In operation STa, the substrate W is placed on the substrate support surface 111a of the substrate support 11 disposed in the chamber 10. The operations of the method MT1 after operation STa are performed with the substrate W placed on the substrate support 11.

[0124] After operation STa, operation ST11 is performed. In operation

ST11, plasma is generated in the chamber 10. In operation ST11, gas is supplied from the gas supply 20 to the interior space 10s. In operation ST11, the pressure in the chamber 10 is reduced to a specified pressure by the exhaust system 40. In operation ST11, plasma is generated from the gas in the chamber 10 by the plasma generator 12. In one embodiment, a source RF signal is supplied from the first RF generator 31a to generate plasma from the gas in the chamber 10.

[0125] After operation ST11, operation ST12 is performed. When the plasma processing apparatus 1 is used, in operation ST12, the voltage pulse VP is intermittently or periodically applied to the bias electrode BE of the substrate support 11 in order to draw ions from the plasma into the substrate W. In operation ST12, as described above with respect to the plasma processing apparatus 1, the switching circuit of the bias power supply system is controlled by the pulse controller so that the voltage pulse VP stepwise reaches its target voltage level.

[0126] When the plasma processing apparatus 101 is used, in operation ST12, the first voltage pulse VP1 and the second voltage pulse VP2 are intermittently or periodically applied to the first bias electrode BE1 and the second bias electrode BE2, respectively, in order to draw ions from the plasma into the substrate W. In operation ST12, as described above with respect to the plasma processing apparatus 101, the first switching circuit of the bias power supply system is controlled by the pulse controller so that the first voltage pulse VP1 stepwise reaches its first target voltage level. Also, in operation ST12, as described above with respect to the plasma processing apparatus 101, the second switching circuit of the bias power supply system is controlled by the pulse

controller so that the second voltage pulse VP2 stepwise reaches its second target voltage level.

[0127] The method MT1 may further include operation STJ1. In operation STJ1, it is determined whether a stop condition is satisfied. The stop condition is satisfied, for example, when the number of executions of a sequence SQ1 including operation ST11 and operation ST12 has reached a predetermined number. When it is determined in operation STJ1 that the stop condition is not satisfied, the sequence SQ1 is executed again from operation ST11. On the other hand, when it is determined in operation STJ1 that the stop condition is satisfied, the method MT1 ends.

[0128] An example of a processing circuit that can be used as one or more processing circuits in a plasma processing apparatus, such as the controller 2 and/or the pulse controllers 54, 54C to 54G, will now be described. FIG. 19 is a block diagram of a processing circuit that implements the operations described in the present specification on a computer. FIG. 19 illustrates a processing circuit 130 that can be used to control control processing on any computer. Descriptions or blocks in a flowchart represent modules, segments, or portions of code that include one or more executable instructions for implementing specific logical functions or steps of processing. As will be understood by those skilled in the art, other embodiments having functions that can be executed in a different order from the illustrated or described order, such as substantially simultaneously or in reverse order, depending on the functions involved, are included within the scope of the example embodiments of the present disclosure. The various elements, features,

and processes described in the present specification may be used independently of each other and may be combined in various ways. All possible combinations and sub-combinations may be included within the scope of the present disclosure.

[0129] In FIG. 19, the processing circuit 130 includes a CPU 1200 that implements one or more of the control processes described above/below. Processing data and instructions may be stored in a memory 1202. These processing data and instructions may be stored in a storage medium disk 1204 such as a hard disk drive (HDD) or a portable storage medium, or may be stored remotely. Furthermore, the present disclosure as set forth in the claims is not limited by the form of a computer-readable medium in which the instructions for the processes according to the present invention are stored. For example, these instructions may be stored in a CD, DVD, flash memory, RAM, ROM, PROM, EPROM, EEPROM, a hard disk, or any other information processing device such as a server and/or computer with which the processing circuit 130 communicates.

[0130] Furthermore, the present disclosure as set forth in the claims may be provided as a utility application, a background daemon, a component of an operating system, or a combination thereof. The present disclosure as set forth in the claims may be executed in conjunction with a CPU 1200 and an operating system known to those skilled in the art, such as Microsoft Windows (registered trademark), UNIX (registered trademark), Solaris (registered trademark), LINUX (registered trademark), or Apple MAC-OS.

[0131] The hardware elements constituting the processing circuit 130

can be realized by various circuit elements. Furthermore, each function of the above-described embodiments can be implemented by a circuit including one or more processing circuits. As shown in FIG. 19, the processing circuit includes a specifically programmed processing device, for example, a processing device (CPU) 1200. The processing circuit also includes devices such as an application specific integrated circuit (ASIC) and conventional circuit components configured to implement the described functions.

[0132] In FIG. 19, the processing circuit 130 includes a CPU 1200 that implements the above-described processing. The processing circuit 130 may be a general-purpose computer or a specific dedicated machine. In one embodiment, when the processing device 1200 is programmed to control the plasma generator 12 and the gas supply 20, or additionally or alternatively, to control the bias power supply systems 50, 50A to 50H, the processing circuit 130 functions as a specific dedicated machine.

[0133] Alternatively or additionally, the CPU 1200 may be implemented on an FPGA, ASIC, or PLD, or using discrete logic circuits, as will be understood by those skilled in the art. Furthermore, the CPU 1200 may be implemented as a plurality of processing devices that cooperate to implement the instructions of the above-described processes of the present invention in parallel.

[0134] The processing circuit 130 of FIG. 19 also includes a network controller 1206 for interfacing with a network 1228, such as an Intel Ethernet PRO network interface card from Intel Corporation of the United States. The network 1228 may be, as will be understood, a public network such as the Internet, a private network such as a LAN or WAN,

or any combination thereof, and may also include subnetworks such as PSTN or ISDN. The network 1228 may also be wired, such as an Ethernet network, or wireless, such as a cellular network including EDGE, 3G, and 4G wireless cellular systems. The wireless network may also be Wi-Fi, Bluetooth (registered trademark), or any other known form of wireless communication.

[0135] The processing circuit 130 further includes a display device controller 1208 such as a graphics card or graphics adapter for interfacing with a display device 1210 such as a monitor. A general-purpose I/O interface 1212 is interfaced with a keyboard and/or mouse 1214, and a touch panel 1216 that is integrated with or separate from the display device 1210. The general-purpose I/O interface is also connected to various peripheral devices 1218 such as printers and scanners.

[0136] A storage device controller 1224 is connected to a storage medium disk 1204 through a communication bus 1226 such as ISA, EISA, VESA, or PCI, and all components of the processing circuit 130 are connected to each other. The general features and functions of the display device 1210, the keyboard and/or mouse 1214, and the display device controller 1208, the storage device controller 1224, the network controller 1206, an audio controller 1220, and the general-purpose I/O interface 1212 are omitted herein as known for the sake of brevity.

[0137] The example circuit elements described in the present disclosure are interchangeable with other elements and may have structures different from the examples described in the present specification. Furthermore, circuits configured to implement the features described in

the present specification may be implemented in a plurality of circuit units (e.g., chips), or these features may be incorporated into the circuitry of a single chipset.

[0138] The functions and features described in the present specification may also be performed by various components distributed across a system. For example, one or more processing devices may perform the functions of these systems, in which case the processing devices are distributed across a plurality of components communicating within a network. The distributed components may include one or more client machines and server machines that can share processing, in addition to various human interface and communication devices (display monitors, smartphones, tablets, personal digital assistants (PDAs), and the like). The network may be a private network such as a LAN or WAN, or a public network such as the Internet. Input to the system may be received by direct input from a user, or may be received remotely in real time or as batch processing. Furthermore, some of the embodiments may be implemented on modules or hardware that are not identical to those described above. Accordingly, other embodiments are also included within the scope of the claims.

[0139] Although various example embodiments have been described above, various additions, omissions, substitutions, and changes may be made without being limited to the above-described example embodiments. Also, it is possible to combine elements in different embodiments to form other embodiments.

[0140] In the bias power supply systems of the various example embodiments described above, the switching operation of the switching

circuit for causing the voltage level of the voltage pulse to stepwise reach the target voltage level is controlled by the pulse controller of the bias power supply system. In another embodiment, the pulse controller need not constitute a part of the bias power supply system. Alternatively, the plasma processing apparatus need not include a pulse controller, and the switching circuit may be configured to perform the switching operation for causing the voltage level of the voltage pulse to stepwise reach the target voltage level without depending on control from any controller.

[0141] From the above description, it will be understood that various embodiments of the present disclosure are described in the present specification for the purpose of illustration, and that various changes may be made without departing from the scope and spirit of the present disclosure. Accordingly, the various embodiments disclosed in the present specification are not intended to be limiting, and the true scope and spirit are indicated by the appended claims.

Reference Signs List

[0142] 1, 101: plasma processing apparatus, 10: chamber, 11: substrate support, BE1: first bias electrode, BE2: second bias electrode, BE: bias electrode, 12: plasma generator, 50: bias power supply system, 51: DC power supply, 53: switching circuit, 54: pulse controller.

CLAIMS

[Claim 1]

A plasma processing apparatus, comprising:

a chamber;

a substrate support having a bias electrode and disposed in the chamber;

a plasma generator configured to generate plasma in the chamber; and

a bias power supply system electrically coupled to the bias electrode and configured to intermittently apply a voltage pulse to the bias electrode to draw ions from the plasma into a substrate on the substrate support,

wherein the bias power supply system includes:

at least one DC power supply;

a switching circuit electrically connected between the bias electrode and the at least one DC power supply; and

a pulse controller configured to control the switching circuit,

wherein the pulse controller is configured to control the switching circuit to cause a voltage level of the voltage pulse to stepwise reach a target voltage level thereof having a maximum potential difference in a negative direction with respect to a reference potential.

[Claim 2]

The plasma processing apparatus according to claim 1, wherein the at least one DC power supply includes:

a first DC power supply capable of outputting an output

voltage having a potential difference smaller than the target voltage level with respect to the reference potential; and

a second DC power supply capable of outputting an output voltage having the target voltage level,

the switching circuit includes:

a first switching element electrically connected between a negative terminal of the first DC power supply and the bias electrode; and

a second switching element electrically connected between a negative terminal of the second DC power supply and the bias electrode, and

the pulse controller is configured to control the switching circuit in application of the voltage pulse to,

set the first switching element to a closed state and set the second switching element to an open state, and

then set the second switching element to a closed state and set the first switching element to an open state.

[Claim 3]

The plasma processing apparatus according to claim 2,

wherein a positive terminal of the second DC power supply is floating from ground and is electrically connected to a negative terminal of the first DC power supply.

[Claim 4]

The plasma processing apparatus according to claim 2, wherein

the first DC power supply includes one or more DC power supplies, and

the second DC power supply includes:

the one or more DC power supplies of the first DC power supply; and

one or more DC power supplies connected in series with the one or more DC power supplies of the first DC power supply.

[Claim 5]

The plasma processing apparatus according to claim 2, wherein

the bias electrode is a first bias electrode,

the voltage pulse is a first voltage pulse,

the target voltage level is a first target voltage level,

the substrate support includes:

a substrate support surface;

a ring support surface;

the first bias electrode extending below the substrate support surface and electrically coupled to the substrate on the substrate support surface; and

a second bias electrode that is separate from the first bias electrode, extends below the ring support surface, and is electrically coupled to an edge ring placed on the ring support surface to surround the substrate,

the at least one DC power supply includes:

a third DC power supply capable of outputting an output voltage having a potential difference smaller than a second target voltage level with respect to the reference potential, the second target voltage level having a maximum potential difference in the negative direction with respect to the reference potential; and

a fourth DC power supply capable of outputting an output voltage having the second target voltage level,

the switching circuit includes:

a third switching element electrically connected between a negative terminal of the third DC power supply and the second bias electrode; and

a fourth switching element electrically connected between a negative terminal of the fourth DC power supply and the second bias electrode, and

the pulse controller is configured to control the switching circuit in application of a second voltage pulse to the edge ring to

set the third switching element to a closed state and set the fourth switching element to an open state, and

then set the fourth switching element to a closed state and set the third switching element to an open state.

[Claim 6]

The plasma processing apparatus according to claim 5, wherein a positive terminal of the fourth DC power supply is floating from ground and is electrically connected to a negative terminal of the third DC power supply.

[Claim 7]

The plasma processing apparatus according to claim 5, wherein

the first DC power supply includes one or more DC power supplies,

the second DC power supply includes:

the one or more DC power supplies of the first DC power

supply; and

one or more DC power supplies connected in series with the one or more DC power supplies of the first DC power supply,

the third DC power supply includes one or more DC power supplies, and

the fourth DC power supply includes:

the one or more DC power supplies of the third DC power supply; and

one or more DC power supplies connected in series with the one or more DC power supplies of the third DC power supply.

[Claim 8]

The plasma processing apparatus according to claim 1, wherein

the at least one DC power supply includes a single DC power supply,

the switching circuit includes a switching element connected between the bias electrode and the single DC power supply, and

the pulse controller is configured to control the switching circuit to cause the voltage level of the voltage pulse to stepwise reach the target voltage level by alternately repeating opening and closing of the switching element.

[Claim 9]

The plasma processing apparatus according to any one of claims 1 to 4 and 8, wherein

the switching circuit further includes an additional switching element electrically connected between ground and the bias electrode, and

the pulse controller is configured to control the switching circuit to:

set the additional switching element to an open state during a period in which the voltage pulse is being applied to the bias electrode; and

set the additional switching element to a closed state during a period in which the voltage pulse is not being applied to the bias electrode.

[Claim 10]

The plasma processing apparatus according to claim 1, wherein

the bias electrode is a first bias electrode,

the voltage pulse is a first voltage pulse,

the target voltage level is a first target voltage level,

the substrate support includes:

a substrate support surface;

a ring support surface;

the first bias electrode extending below the substrate support surface and electrically coupled to the substrate on the substrate support surface; and

a second bias electrode that is separate from the first bias electrode, extends below the ring support surface, and is electrically coupled to an edge ring placed on the ring support surface to surround the substrate,

the at least one DC power supply includes:

a first DC power supply capable of outputting an output voltage having the first target voltage level; and

a second DC power supply capable of outputting an output voltage having a second target voltage level having a maximum potential difference in the negative direction with respect to the reference potential,

the switching circuit includes:

a first switching element electrically connected between a negative terminal of the first DC power supply and the first bias electrode; and

a second switching element electrically connected between a negative terminal of the second DC power supply and the second bias electrode, and

the pulse controller is configured to control the switching circuit to:

cause the voltage level of the first voltage pulse to stepwise reach the first target voltage level by alternately repeating opening and closing of the first switching element in application of the first voltage pulse to the first bias electrode; and

cause the voltage level of a second voltage pulse to stepwise reach the second target voltage level by alternately repeating opening and closing of the second switching element in application of the second voltage pulse to the second bias electrode.

[Claim 11]

The plasma processing apparatus according to claim 10, wherein a positive terminal of the second DC power supply is floating from ground and is electrically connected to a negative terminal of the first DC power supply.

[Claim 12]

The plasma processing apparatus according to claim 5 or 10, wherein

the switching circuit further includes:

a first additional switching element connected between the first bias electrode and ground; and

a second additional switching element connected between the second bias electrode and ground, and

the pulse controller is configured to control the switching circuit to:

set the first additional switching element to an open state during a period in which the first voltage pulse is being applied to the first bias electrode, and set the first additional switching element to a closed state during a period in which the first voltage pulse is not being applied to the first bias electrode; and

set the second additional switching element to an open state during a period in which the second voltage pulse is being applied to the second bias electrode, and set the second additional switching element to a closed state during a period in which the second voltage pulse is not being applied to the second bias electrode.

[Claim 13]

A bias power supply system configured to intermittently apply a voltage pulse to a bias electrode of a substrate support to draw ions from plasma in a chamber of a plasma processing apparatus into a substrate on the substrate support in the chamber, the bias power supply system comprising:

at least one DC power supply; and

a switching circuit electrically connected between the bias electrode and the at least one DC power supply,

wherein the switching circuit is configured to cause, by switching operation thereof, a voltage level of the voltage pulse to stepwise reach a target voltage level thereof having a maximum potential difference in a negative direction with respect to a reference potential.

[Claim 14]

A plasma processing method, comprising:

(a) preparing a substrate, the substrate being placed on a substrate support in a chamber of a plasma processing apparatus; and

(b) generating plasma in the chamber; and

(c) intermittently applying a voltage pulse to a bias electrode of the substrate support to draw ions into the substrate,

wherein the (c) includes controlling a switching circuit electrically connected between the bias electrode and at least one DC power supply to cause a voltage level of the voltage pulse to stepwise reach a target voltage level thereof having a maximum potential difference in a negative direction with respect to a reference potential.