

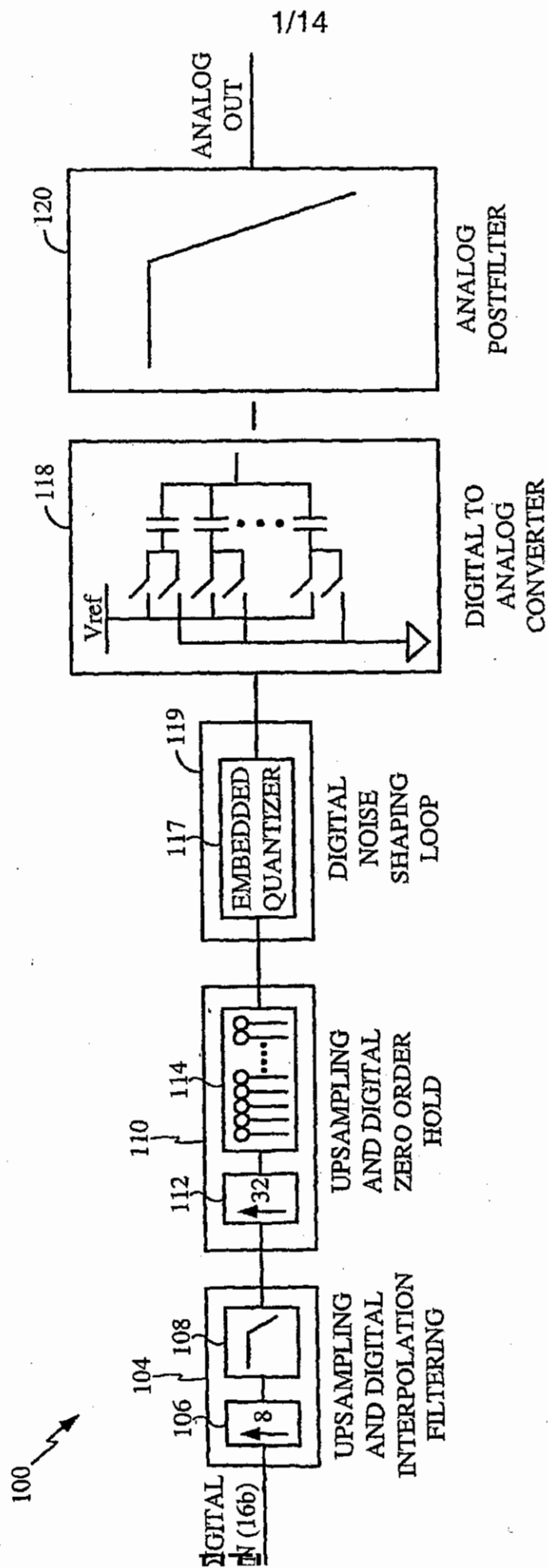


FIG. 1: BLOCK DIAGRAM OF OVERSAMPLED DIGITAL-TO-ANALOG CONVERTER

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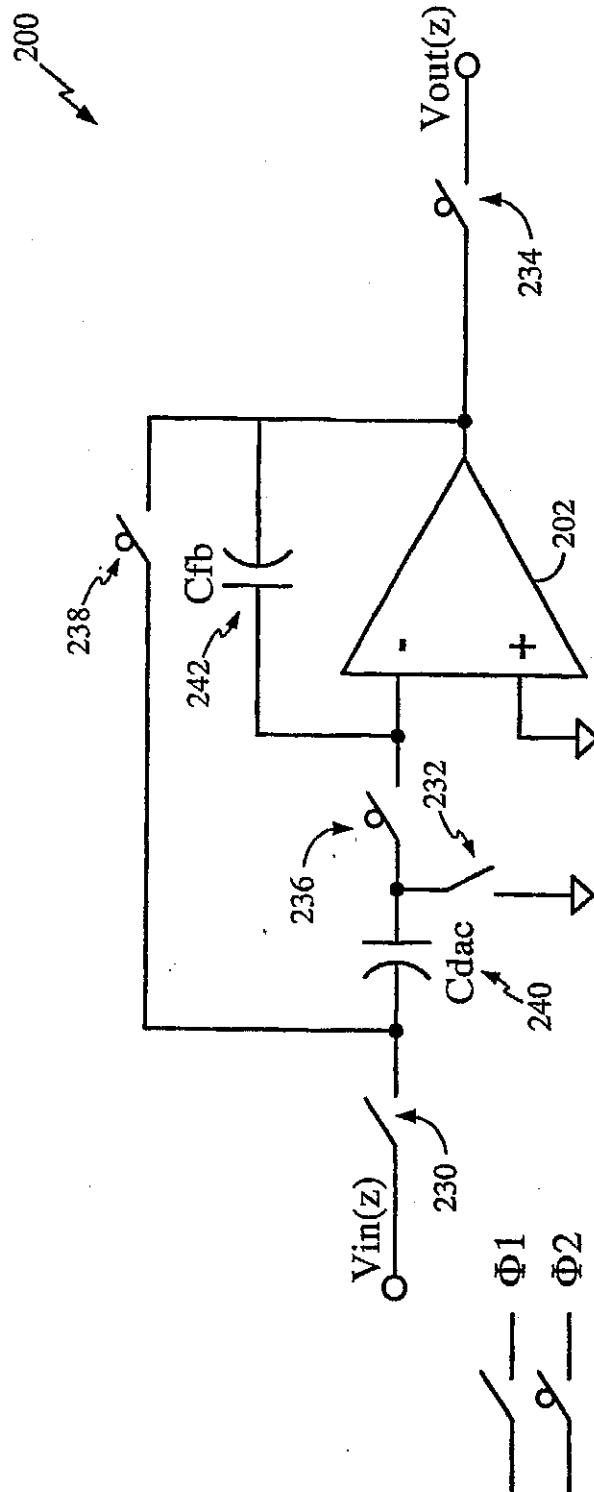


FIG. 2A: DIRECT CHARGE TRANSFER FILTER BLOCK

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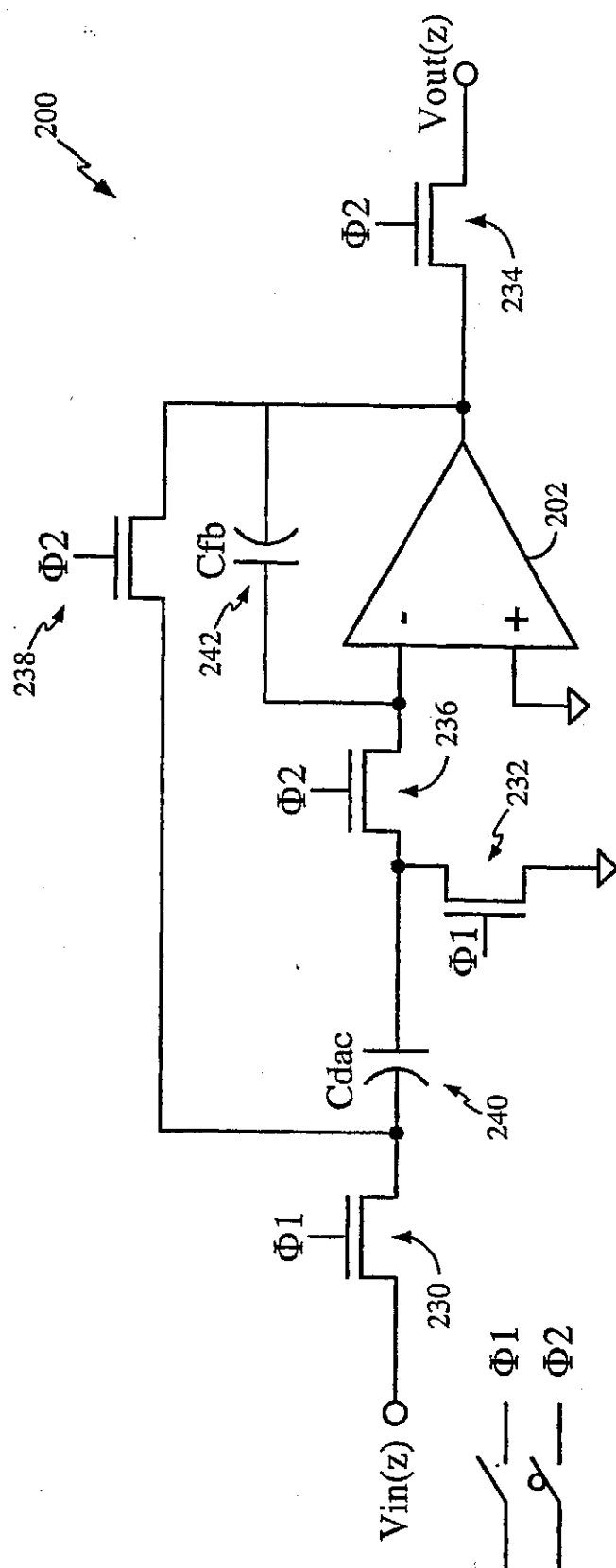


FIG. 2B: DIRECT CHARGE TRANSFER FILTER BLOCK

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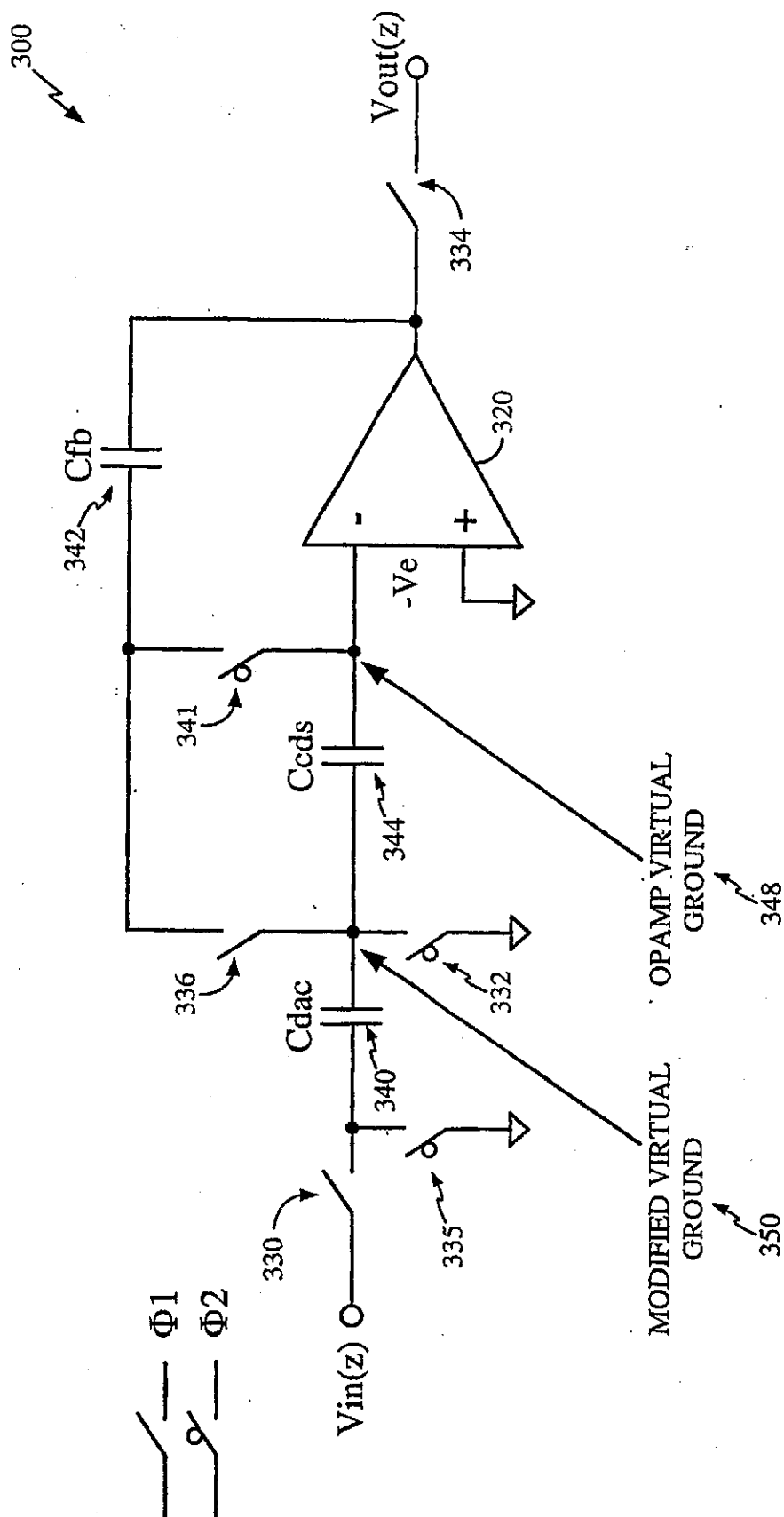


FIG. 3A: CORRELATED DOUBLE SAMPLING TECHNIQUE

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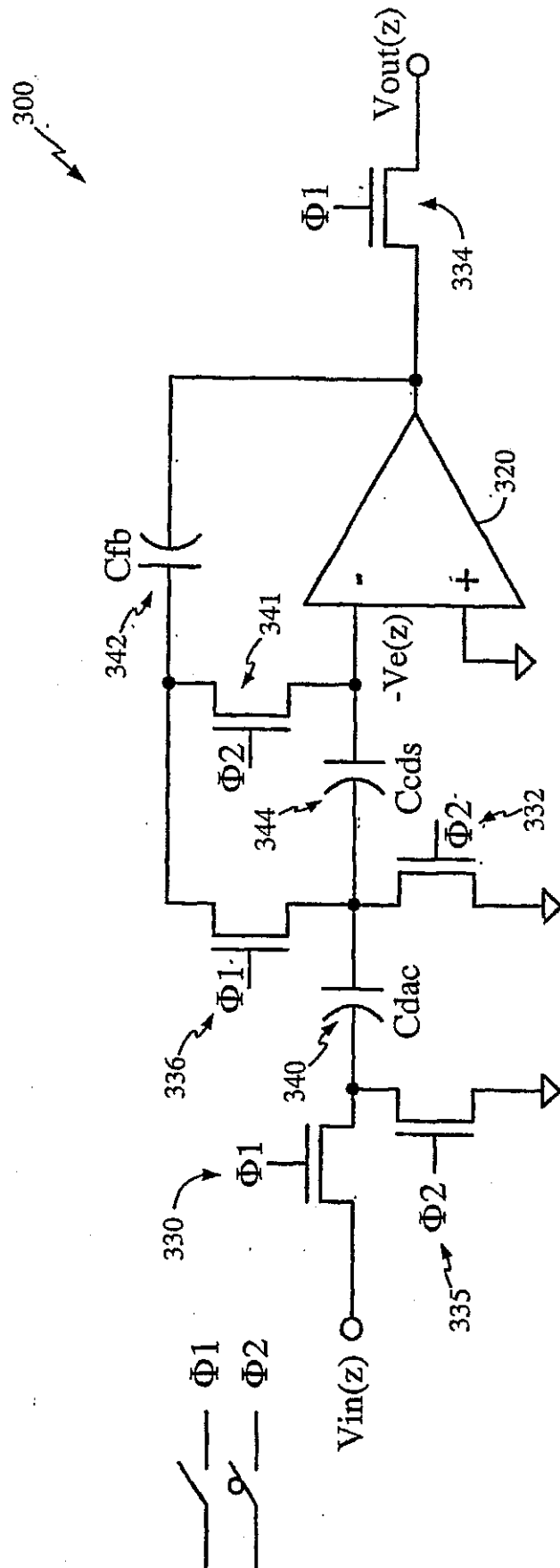


FIG. 3B: CORRELATED DOUBLE SAMPLING FOR A SWITCHED-CAPACITOR INTEGRATOR

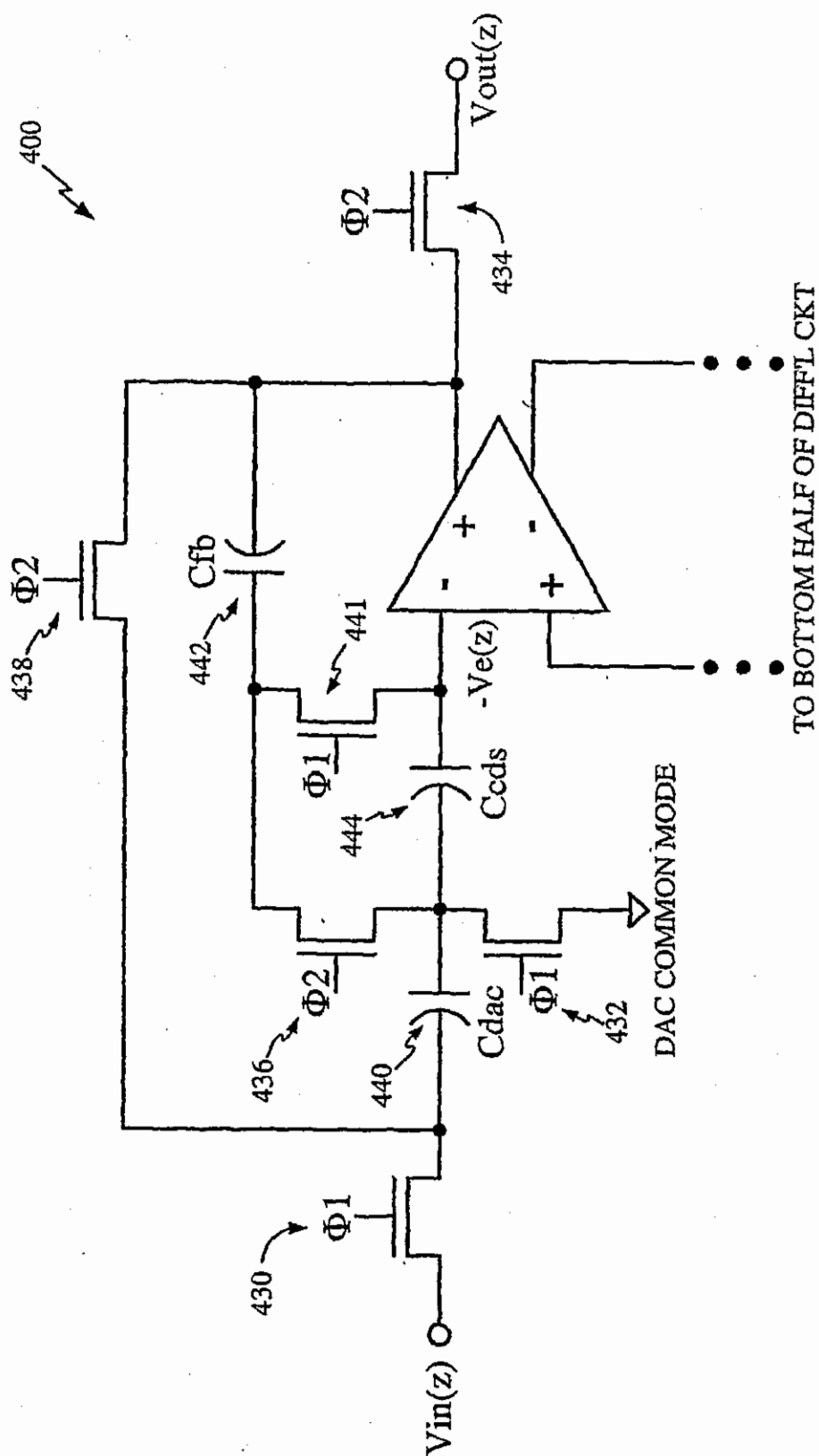


FIG. 4A: FIRST-ORDER DCT FILTER BLOCK WITH CDS

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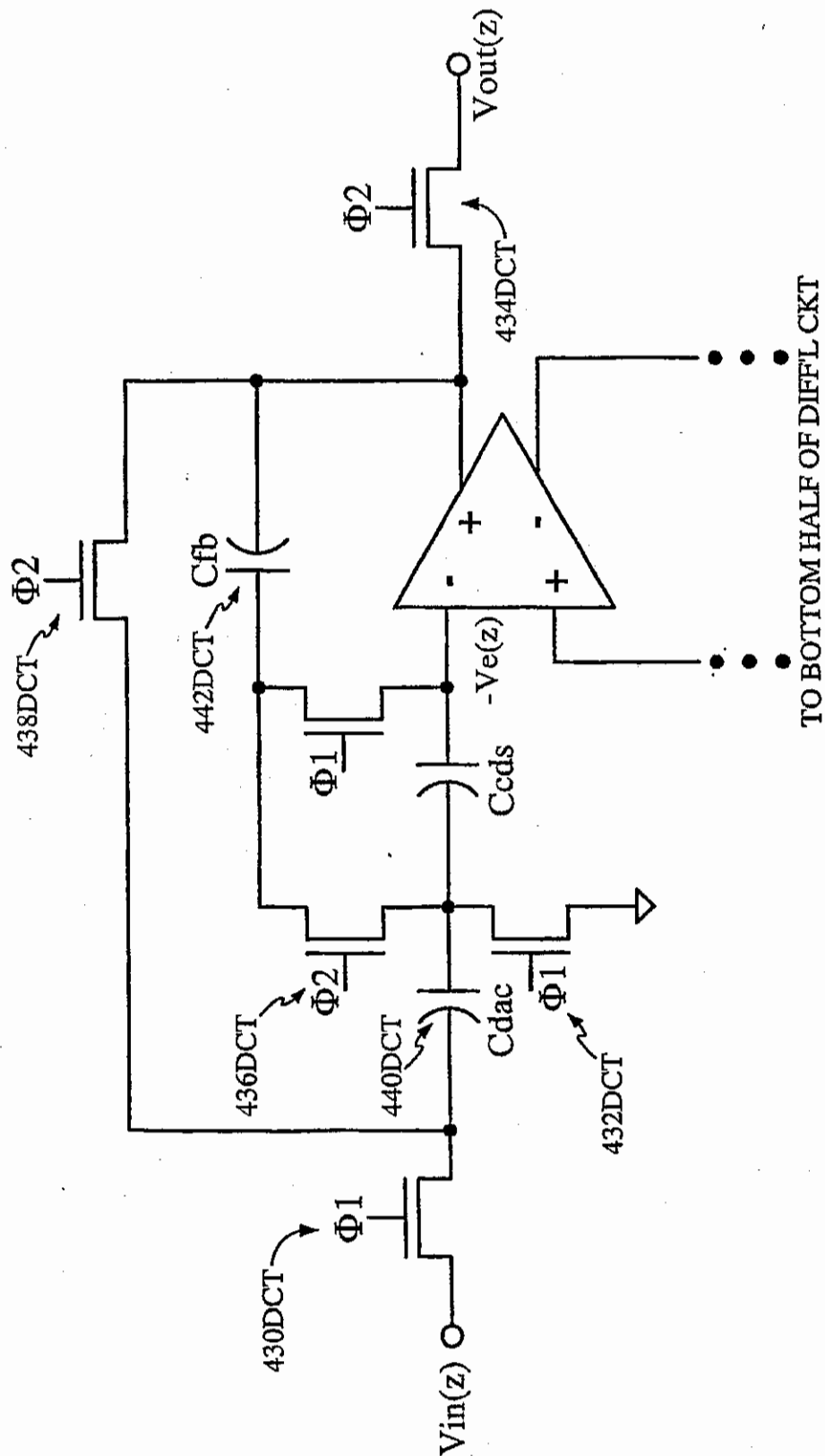


FIG. 4B: FIRST-ORDER DCT FILTER BLOCK WITH CDS

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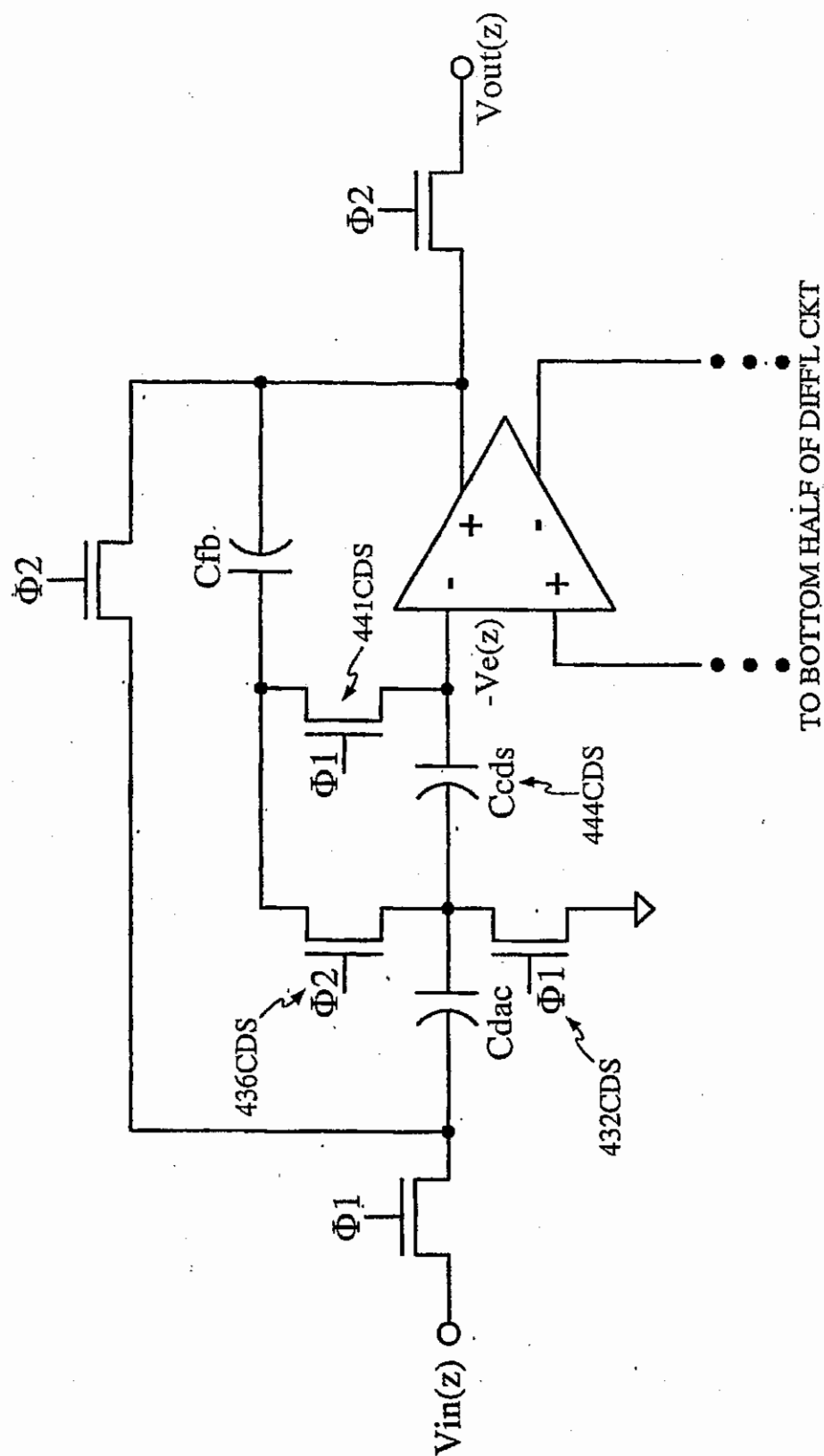
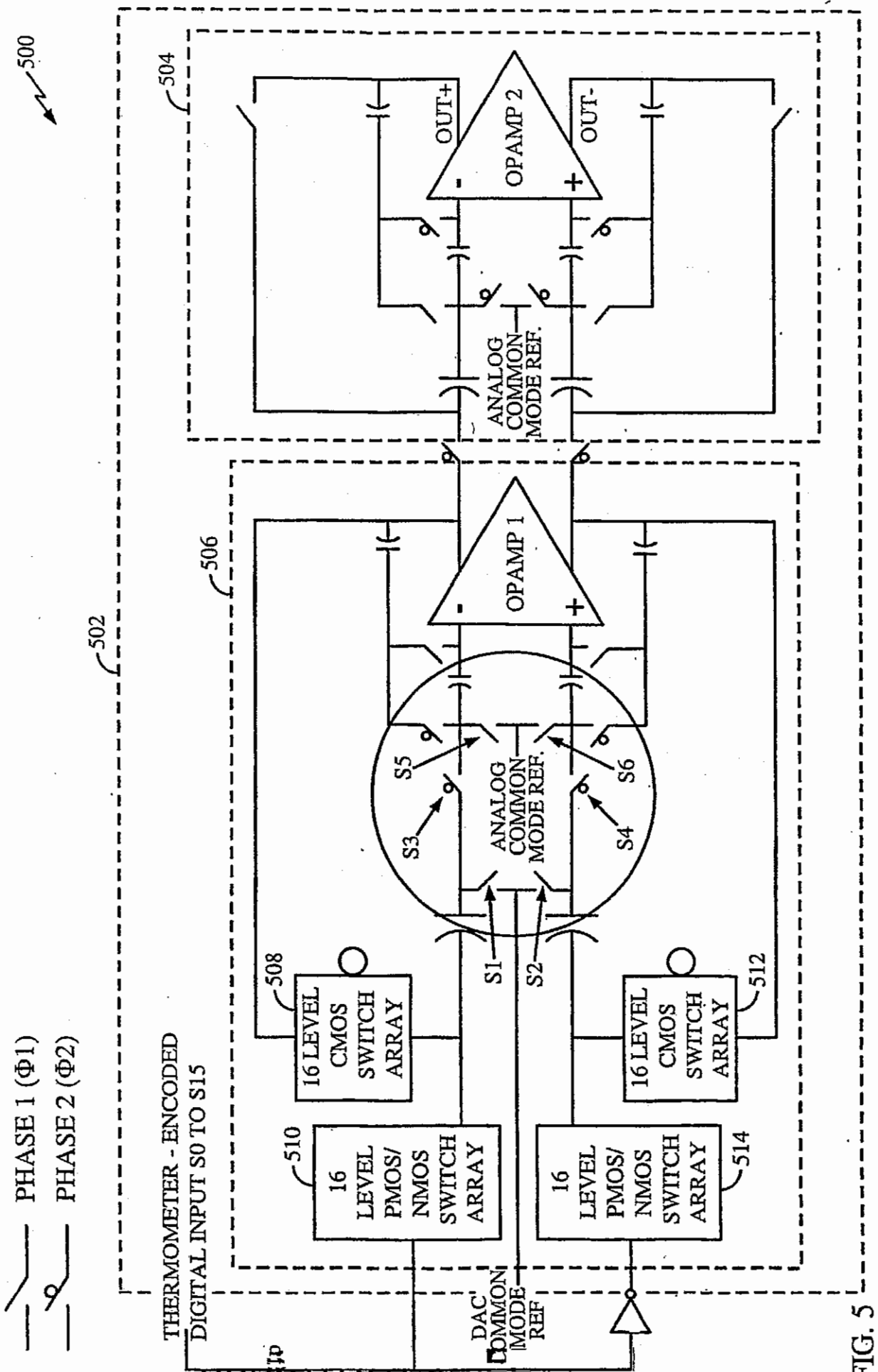
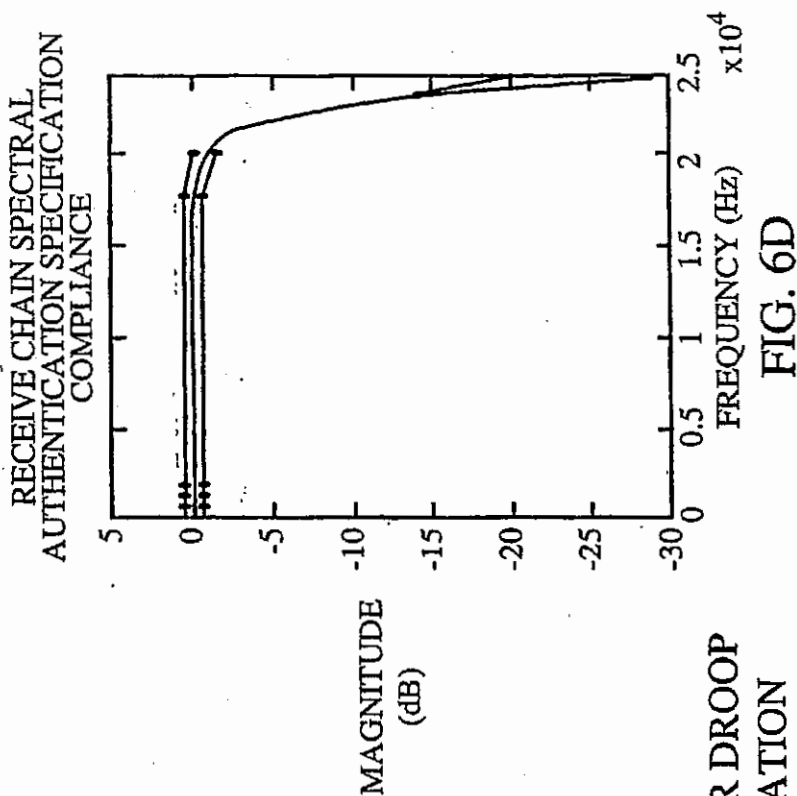


FIG. 4C: FIRST-ORDER DCT FILTER BLOCK WITH CDS

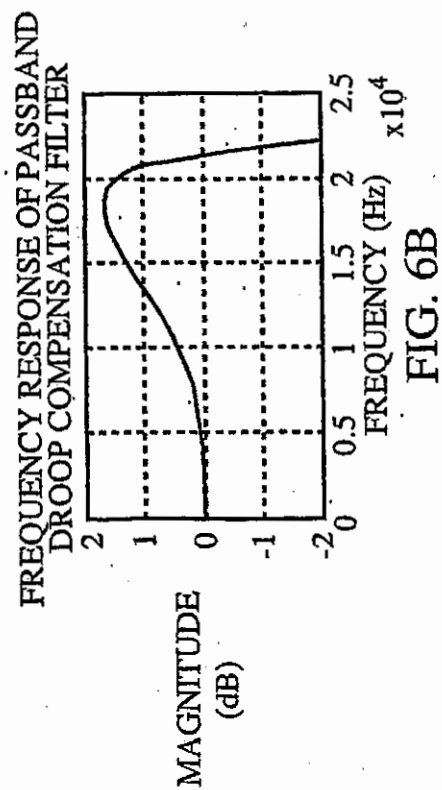
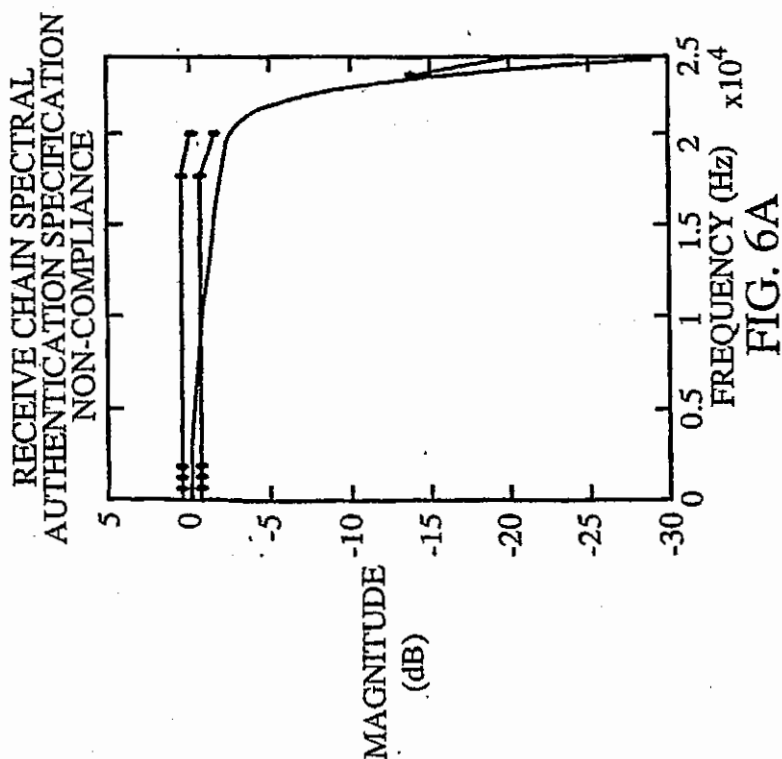
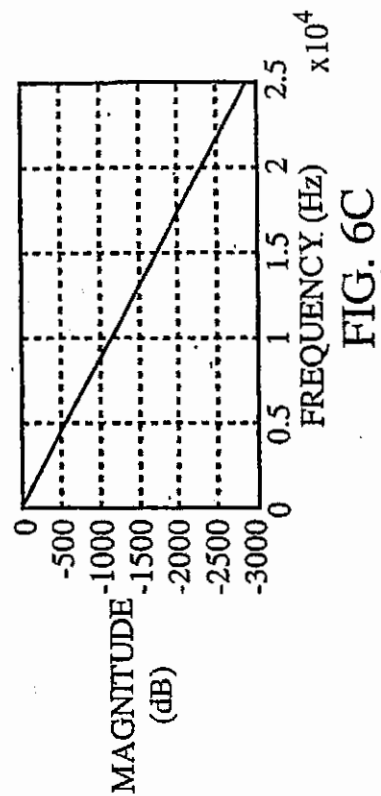
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POSTFILTER DROOP COMENSATION



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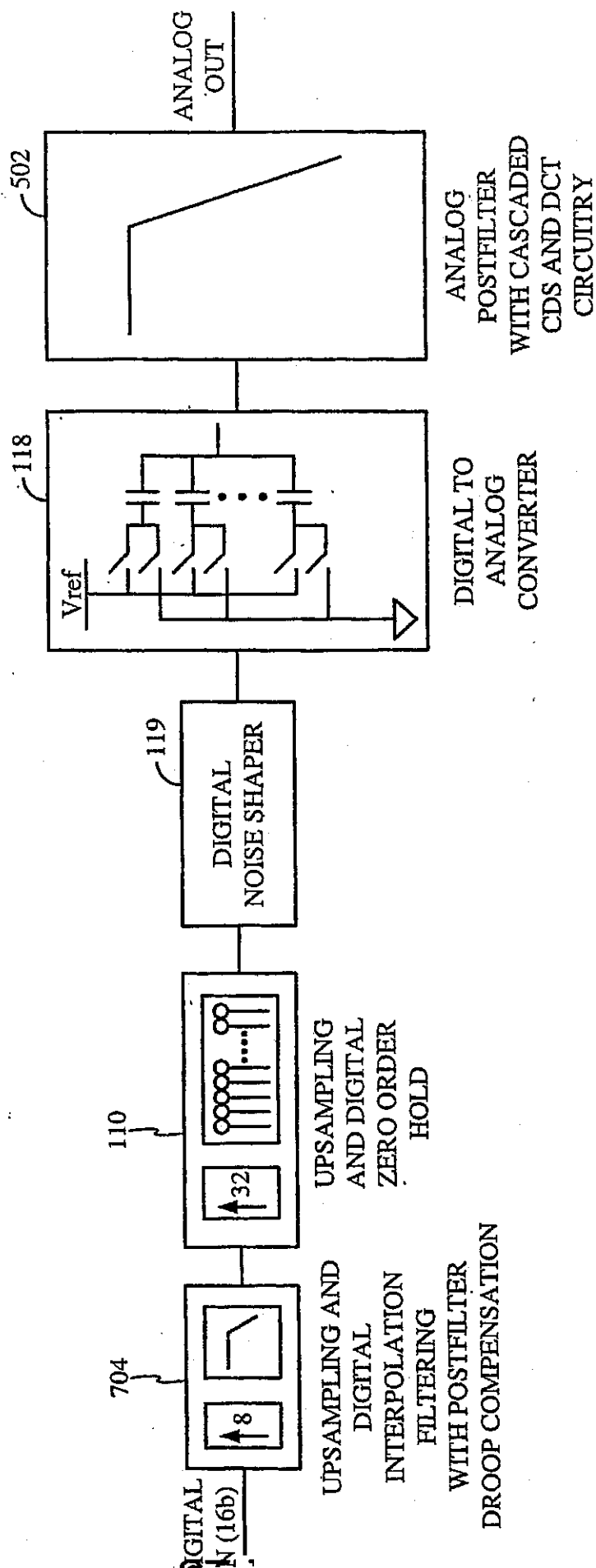


FIG. 7: BLOCK DIAGRAM OF PROPOSED DIGITAL-TO-ANALOG CONVERTER CHAIN

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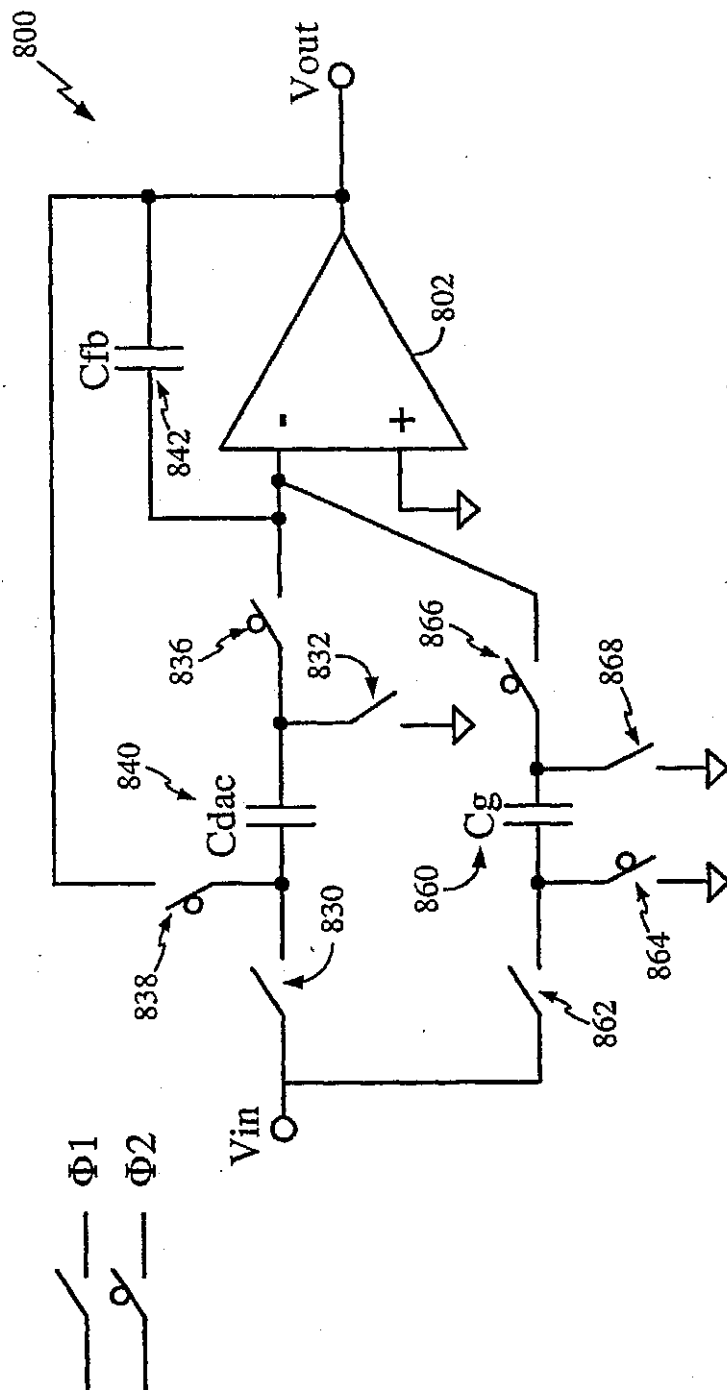
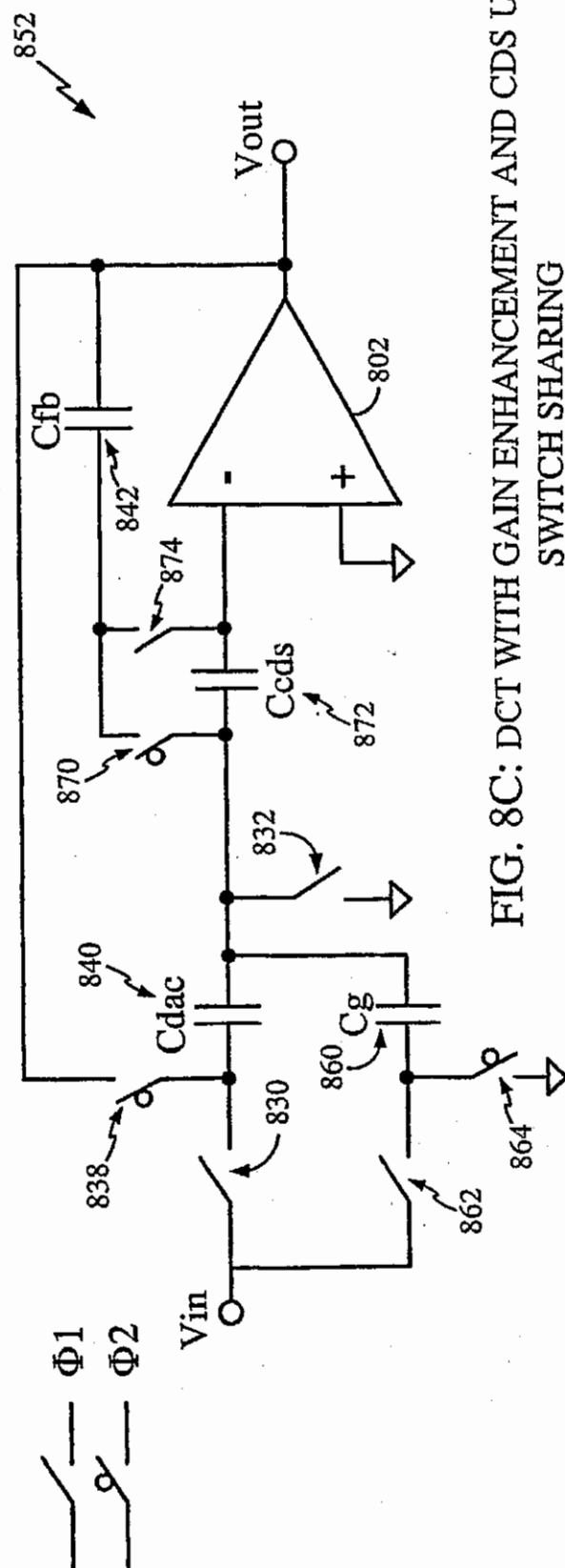
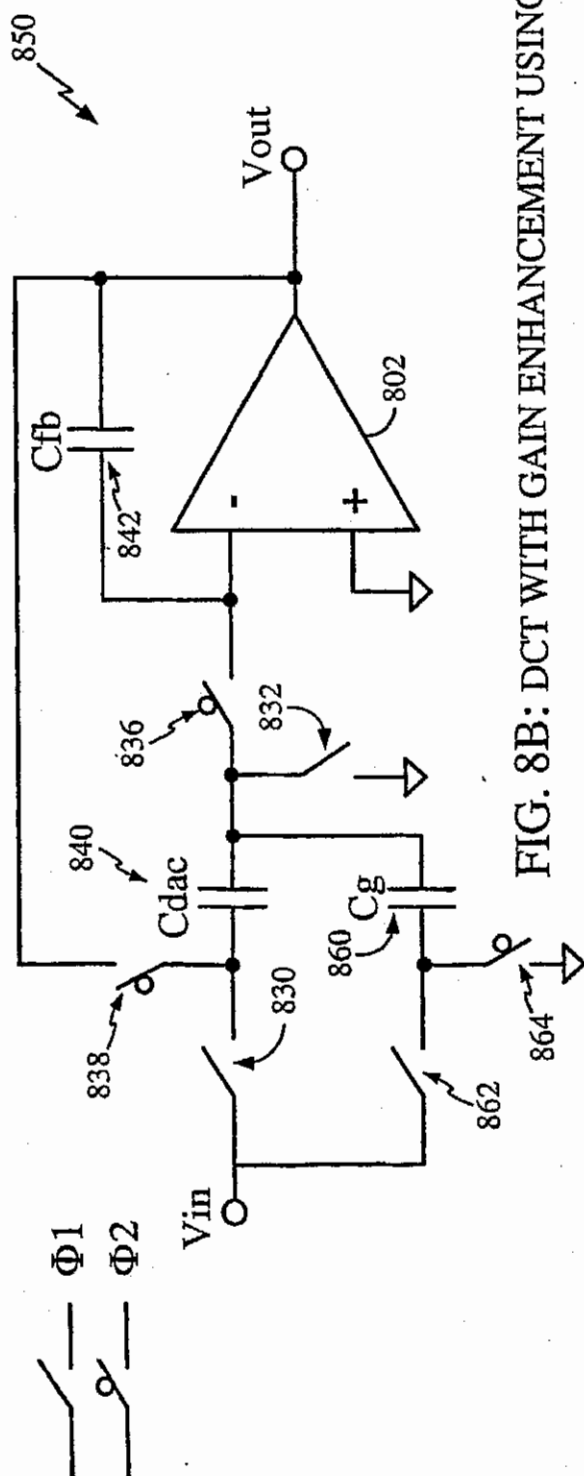


FIG. 8A: DCT WITH GAIN ENHANCEMENT



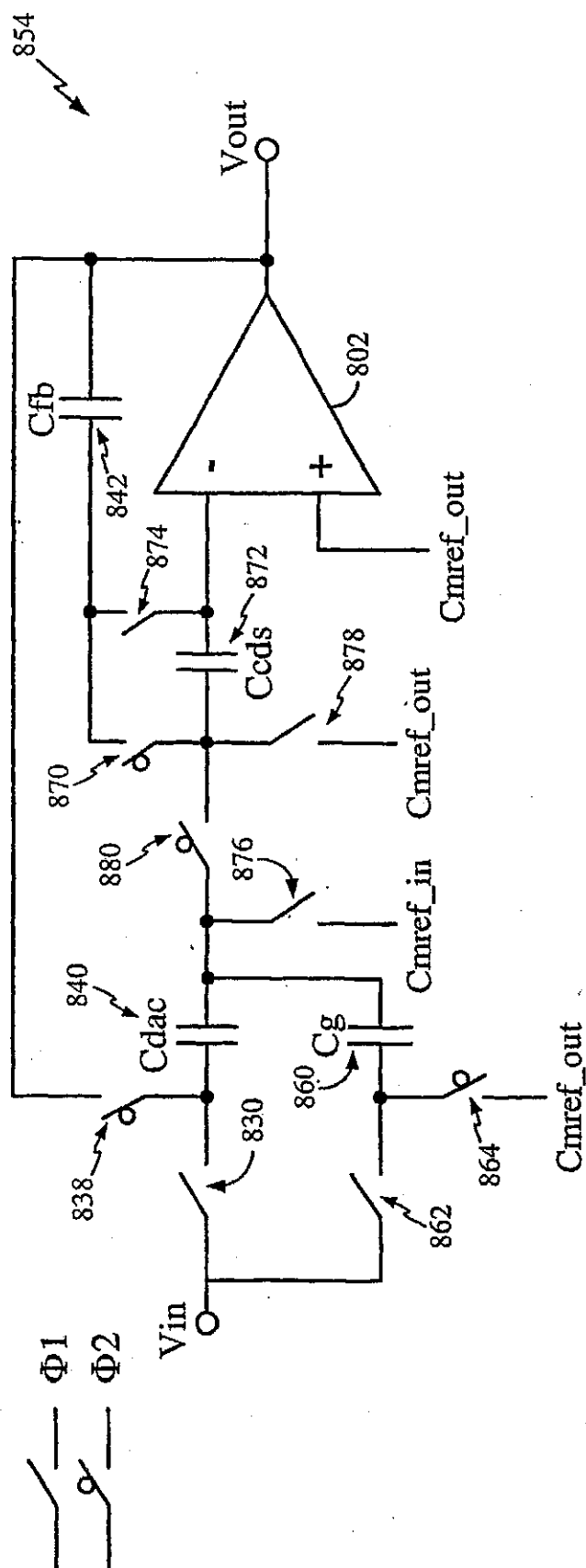


FIG. 8D: DCT WITH CDS, GAIN ENHANCEMENT, SWITCH SHARING, AND DUAL COMMON MODE REFERENCE