

Description

Field of the Invention

This invention relates to rectifiers and more particularly to a full wave rectifier suitable to be utilized in high speed, wide band input signal applications that can be fabricated in monolithic integrated circuit form and which exhibits excellent linearity between the output signal and the applied input signal thereto.

Description of the Prior Art

The prior art is replete with full wave rectifiers that are used in a myriad of applications. For instance, full wave rectifiers are commonly used in amplitude demodulation and amplitude measurement systems. Full wave rectifiers also may be utilized for video detection and are found as part of the video detector portions of television receivers to remove the video signal from the television composite carrier signal.

Some contemporary rectifiers that may be used in high speed, wide-band input signal schemes have a major problem associated therewith. In order to operate efficiently at high speeds contemporary full wave rectifiers are generally direct current biased at a quiescent operating point. As will be more fully explained later, the effect of direct current biasing causes these full wave rectifiers to have a non-linear transfer characteristic. Hence, the output signal is not an exact reproduction of the two halves of the applied alternating signal.

Another problem associated with some prior art detectors utilized, for example, as video detectors in a television set is that these detectors require a tuned circuit at the television carrier frequency. A typical example of such prior art is the Motorola Inc., MC1330 low level video detector integrated circuit which requires a tuned circuit. The tuned circuit may cause phase related problems in the television receiver as well as spurious feedback to the high sensitivity input terminals of the integrated circuit which is undesirable. Additionally, the need for a tuned circuit requires external terminals be provided between the integrated circuit and the tuned circuit which is undesirable.

Thus, a need exists for a linear full wave rectifier for operation in high speed applications and which may be utilized for example in video detection systems without the need for a tuned circuit.

Summary of the Invention

Accordingly, it is an object of the present invention to provide an improved full wave rectifier having excellent high frequency performance.

It is another object of the present invention to provide a full wave rectifier circuit for high speed, wide band input signal applications.

Still another object of the present invention is to provide a full wave rectifier circuit suitable for fabrication in monolithic integrated circuit form.

One other object of the present invention is to

provide a full wave rectifier circuit which may be utilized as the video detector of a television receiver which requires no tuned circuit for operation.

Accordingly the invention provides a full wave rectifier comprising first rectifier means adapted to receive an alternating input signal at an input thereof and producing an output signal that is a full wave rectified version of said alternating input signal;

current turnaround means responsive to said output signal from said first rectifier means for producing an output signal at an output substantially identical to said output signal from said first rectifier means;

second rectifier means coupled to said output of said current turnaround means having a substantially identical transfer characteristic to said first rectifier means; and

linearization circuit means coupled between said output of said current turnaround means and the input of said second rectifier means for providing feedback to said second rectifier means such that the signal appearing at a node at which said output of said current turnaround means and said second rectifier means is combined is substantially an exact full wave rectified version of said alternating input signal.

Brief Description of the Drawings

FIG. 1 is a schematic drawing of a full wave rectifier having a non-linear transfer characteristic which may be utilized in the present invention;

FIG. 2 is a graph illustrating the non-linear transfer characteristics of the non-linear full wave rectifier of FIG. 1;

FIG. 3 illustrates in block diagram form a preferred embodiment of the present invention;

FIG. 4 is a schematic diagram illustrating a single ended input full wave rectifier of the present invention;

FIG. 5 is a schematic and block diagram of a full wave rectifier of an embodiment of the present invention; and

FIG. 6 is a schematic diagram illustrating the full wave rectifier of FIG. 5 in complete detail.

Description of the Preferred Embodiments

A full wave rectifier 10 is shown in FIG. 1 which exhibits a non-linear transfer characteristic. Full wave rectifier 10 comprises transistors 12 and 14 which have collectors summed together at node 16 to output terminal 18 with the emitter of transistor 12 being connected to the base of transistor 14. The emitter of transistor 14 is returned to a terminal at which is provided a ground reference potential. A diode 20 is connected between the base and the emitter of transistor 14 with the interconnection between the emitter of transistor 12 and the anode of diode 20 being adapted to receive an alternating input signal I_{IN} thereat. In order to operate in high speed applications, transistors 12 and 14 must be DC biased at a quiescent operating point which is determined by the circuit connected at node 22 to the base of tran-

sistor 12 comprising current source 24 coupled between a source of operating potential V_{CC} and node 22 to serially connected diodes 26 and 28.

As configured, a positive going input current supplied at the interconnection of the emitter of transistor 12 and the anode of diode 20 will increase the current through the diode which increases the current through the collector-to-emitter path of transistor 14 to increase the output current, I_o . Likewise, a negative going current increases the collector-to-emitter current through transistor 12. Thus, applied alternating input current, I_{IN} , having both positive and negative going halves, produces a full wave rectified output current I_o at output terminal 18.

FIG. 2 illustrates the linearity between the output current I_o and the absolute magnitude of the applied input current I_{IN} . Straight line 30 represents the ideal output if rectifier 10 had a linear transfer characteristic, i.e., the output current was a direct function of the applied input signal. However, as shown by the curve 32, the output of full wave rectifier 10 asymptotically approaches straight line 30 and is only linear for the input signal I_{IN} being much greater than the bias current I_b . Hence, since the bias current is necessary to provide a low impedance at the input and to give good high frequency performance, the output of full wave rectifier 10 becomes non-linear at lower input current signal magnitudes.

Turning to FIG. 3 there is shown a substantially linear full wave rectifier 40 of the present invention. Full wave rectifier 40 is illustrated as including first and second non-linear rectifiers 42 and 44 respectively which, for example, may be identical to non-linear rectifier 10 of FIG. 1. As illustrated, symmetrical full wave rectifier 42 receives an alternating input current I_{IN} supplied from current source 46 at an input thereof to provide a full wave rectified output signal at the output thereof. As previously discussed, non-linear rectifier 42 may not have a perfect linear transfer characteristic such that the full wave rectified output signal appearing at lead 48 has non-linearities therein due to the biasing problems previously discussed. The full wave rectified output signal from rectifier 42 provides an input current to current mirror 50 which produces an output current over lead 52 which is substantially identical to the full wave rectified output signal from rectifier 42. Non-linear rectifier 44 which as an identical transfer characteristic to rectifier 42 is provided an input signal via lead 60 from a current feedback source 56 which is coupled to node 54. Thus, in order for the full wave rectified output signal appearing at the output of rectifier 44 via lead 62 to be identical to the full wave rectified signal produced at the output of current mirror 50, the full wave rectified signal supplied to the input thereof from current feedback source 56 must be a substantially perfect full wave rectified version of the two alternating halves of the applied alternating signal. Hence, the output current I_o which appears at terminal 58 is a perfect reproduction of the alternating halves of the input

current I_{IN} . Therefore, a substantially perfect full wave rectified output signal can be produced from an alternating input signal by utilizing two non-linear but symmetrical full wave rectifiers having substantially identical transfer characteristics.

Linear full wave rectifier 70 which shown in FIG. 4 illustrates one preferred embodiment of the present invention utilizing the non-linear symmetrical full wave rectifier shown in FIG. 1 for example. It is noted that components in FIG. 4 corresponding to like components in FIG. 1 are designated by the same reference numerals. Thus, non-linear rectifier 42 is illustrated as comprising transistors 12, 14 and diode 20 connected in the same manner as illustrated in FIG. 1 with the base of transistor 12 receiving a bias current through the bias circuit comprising current source 24 and diodes 26 and 28. Similarly, non-linear symmetrical full wave rectifier 44 is shown as comprising transistors 12', 14' and diode 20' configured in an identical manner as described in FIG. 1 for full wave rectifier 10. Full wave rectifier 44 is biased from current source 24 as understood.

In response to an input current I_{IN} provided by alternating current source 46 which is applied to the base of transistor 14 (the input of rectifier 42) a full wave rectified output signal is produced at the interconnection of the collectors of transistors 12 and 14 which provides the input current to current mirror 50. Current mirror 50 is illustrated as including diode connected transistor 72 and transistor 74 connected in a well known current mirror configuration. Thus, the non-linear full wave rectified current appearing at the output of rectifier 42 flows through the collector-emitter path of transistor 72 to cause an output non-linear full wave rectified current to appear at the collector of transistor 74, at node 76. This output current from current mirror 50 provides base drive to transistor 78 which produces the input signal to full wave rectifier 44 at the base of transistor 14'. This input current produces an output current which is summed at the collectors of transistors 12' and 14', at node 76, which is constrained to be identical to the output current from current mirror 50. Thus, in order for the full wave rectified output signal from rectifier 44 to be identical to the output full wave rectified signal appearing at the output of full wave rectifier 42 means that the input signal through the collector-emitter of transistor 78 must be a nearly perfect reproduction of the two halves of the alternating input signal I_{IN} . Thus, the output current I_o appearing at the collector of transistor 78, the output of linear full wave rectifier 70, is substantially a perfect full wave rectified version of the input signal to the full wave rectifier circuit.

FIG. 5 illustrates another embodiment of the present invention which is adapted to differentially receive an alternating input signal. Full wave rectifier 80 of FIG. 5 is shown as having differential input terminals 82 and 84 at which an applied alternating input signal appears. The differential input signal is coupled via coupling capacitors CC

to the anodes of diodes 86 and 88. Diodes 86 and 88 are connected respectively between a ground reference potential and the emitters of transistors 90 and 92 which have the collectors thereof connected at summing node 94. The bases of transistors 90 and 92 are coupled to a bias voltage. In response to the alternating input signal applied at terminals 82 and 84 transistors 90 and 92 are rendered alternately conducting or non-conducting as previously explained such that a full wave rectified output signal appears at node 94. A current mirror or current turn around circuit 96 is shown which is driven at the input thereof by the output signal from transistors 90 and 92 to produce a substantially identical output signal at node 98. This output signal is utilized to drive transistor 100 in the same manner as discussed above with respect to transistor 78 (FIG. 4) to provide an input signal to the input of full wave rectifier 44 which is shown as comprising diode 102 and transistors 104 and 106 configured in the same manner as described for full wave rectifier 42 of FIG. 4. Hence the output current at terminal 109, I_o , is a nearly perfect full wave rectified version of the input signal applied between terminals 82 and 84.

Turning to FIG. 6 current mirror 96 is shown in detail and is useful for explaining the operation thereof. The full wave rectified signals appearing at node 94 are applied to the input of amplifier 110 through resistor 116. The output of amplifier 110 is taken at node 111 and is supplied to resistors 112 and 114 which are substantially equal in value. By holding both nodes 94 and 98 at the same voltage (here two diode voltage drops above ground potential) and making the gain of amplifier 110 sufficiently high, the change in voltage at node 94 appears at node 111 such that equal currents flow through resistors 112 and 114. Thus, the current flowing at node 98 is substantially identical to the full wave rectified current flowing at node 94.

Amplifier 110 comprises transistor 118, which is the input stage of amplifier 110, coupled to resistor 116. Transistor 118 is coupled in an emitter-follower configuration with resistor 120 to the base of transistor 122 such that, for example, when transistor 92 is turned on, transistors 118 and 122 are turned off which increases the voltage at the collector of transistor 122. This causes buffer transistor 126 to be rendered conductive to change the voltage at the top of resistors 112 and 114 (nodes 94 and 98 being at virtual ground) and thus producing equal and like currents there-through. Thus, the output signal from current mirror 96 appearing at node 98 is substantially identical to the full wave rectified signal developed at node 94. The signal at node 98 drives transistor 100 via resistor 127 which in turn drives the rectifier input coupled between the emitter of this transistor and resistor 108. Essentially, transistor 100 therefore compares the output of current mirror 96 with the output of the rectifier at node 98 and constrains this output to be equal with the current mirror output. Hence, the output

signal at terminal 109 is a perfect full wave rectified version of the alternating input signal.

Resistor 108 is utilized to bias transistor 100 at a quiescent operating point in order that the output signal at terminal 109 rides about a DC bias level. The DC bias for full wave rectifier as previously suggested is provided between the interconnection of resistor 130 and serially connected diodes 132, 134. As shown by example, diodes 86, 88, 102 may be formed by using diode connected transistor as well may be remaining diodes 132 and 134.

Thus, what has been described above, is a method and circuit for producing a full wave rectified output signal which is linearly related to an alternating signal applied to the input of the full wave rectifier circuit. The full wave rectifier circuit comprises a pair of identical non-linear but symmetrical full wave rectifiers each having its output coupled to a current mirror. The input of the first rectifier is adapted to receive an alternating input signal such that at the output of the current mirror which is coupled to the output of the second rectifier there appears a full wave rectified output signal identical to the full wave rectified output signal produced by the first rectifier. A current feedback source coupled to the output of the current mirror provides an input signal to the second rectifier such that the output of the second rectifier is constrained to be identical to the output of the first rectifier. Thus, the input signal to the second rectifier is a perfect full wave rectified version of the input signal to the first rectifier since the input to the second rectifier is constrained to have one polarity.

Claims

1. A full wave rectifier (40) comprising, first rectifier means (42) adapted to receive an alternating input signal (I_{in}) at an input thereof and producing an output signal that is a full wave rectified version of said alternating input signal (I_{in});

current turnaround means (50) responsive to said output signal (48) from said first rectifier means (42) for producing an output signal (52) at an output substantially identical to said output signal from said first rectifier means (42);

second rectifier means (44) coupled to said output (52) of said current turnaround means (50) having a substantially identical transfer characteristic to said first rectifier means (42); and

linearization circuit means (56) coupled between said output (52) of said current turnaround means (50) and the input of said second rectifier means (44) for providing feedback to said second rectifier means (44) such that the signal appearing at a node at which said output (52) of said current turnaround means (50) and said second rectifier means (44) is combined is substantially an exact full wave rectified version (I_o) of said alternating input signal (I_{in}).

2. The full wave rectifier of claim 1 wherein said first rectifier means (42) comprises:

(11)

to the anodes of diodes 86 and 88. Diodes 86 and 88 are connected respectively between a ground reference potential and the emitters of transistors 90 and 92 which have the collectors thereof connected at summing node 94. The bases of transistors 90 and 92 are coupled to a bias voltage. In response to the alternating input signal applied at terminals 82 and 84 transistors 90 and 92 are rendered alternately conducting or non-conducting as previously explained such that a full wave rectified output signal appears at node 94. A current mirror or current turn around circuit 96 is shown which is driven at the input thereof by the output signal from transistors 90 and 92 to produce a substantially identical output signal at node 98. This output signal is utilized to drive transistor 100 in the same manner as discussed above with respect to transistor 78 (FIG. 4) to provide an input signal to the input of full wave rectifier 44 which is shown as comprising diode 102 and transistors 104 and 106 configured in the same manner as described for full wave rectifier 42 of FIG. 4. Hence the output current at terminal 109, I_o , is a nearly perfect full wave rectified version of the input signal applied between terminals 82 and 84.

Turning to FIG. 6 current mirror 96 is shown in detail and is useful for explaining the operation thereof. The full wave rectified signals appearing at node 94 are applied to the input of amplifier 110 through resistor 116. The output of amplifier 110 is taken at node 111 and is supplied to resistors 112 and 114 which are substantially equal in value. By holding both nodes 94 and 98 at the same voltage (here two diode voltage drops above ground potential) and making the gain of amplifier 110 sufficiently high, the change in voltage at node 94 appears at node 111 such that equal currents flow through resistors 112 and 114. Thus, the current flowing at node 98 is substantially identical to the full wave rectified current flowing at node 94.

Amplifier 110 comprises transistor 118, which is the input stage of amplifier 110, coupled to resistor 116. Transistor 118 is coupled in an emitter-follower configuration with resistor 120 to the base of transistor 122 such that, for example, when transistor 92 is turned on, transistors 118 and 122 are turned off which increases the voltage at the collector of transistor 122. This causes buffer transistor 126 to be rendered conductive to change the voltage at the top of resistors 112 and 114 (nodes 94 and 98 being at virtual ground) and thus producing equal and like currents there-through. Thus, the output signal from current mirror 96 appearing at node 98 is substantially identical to the full wave rectified signal developed at node 94. The signal at node 98 drives transistor 100 via resistor 127 which in turn drives the rectifier input coupled between the emitter of this transistor and resistor 108. Essentially, transistor 100 therefore compares the output of current mirror 96 with the output of the rectifier at node 98 and constrains this output to be equal with the current mirror output. Hence, the output

signal at terminal 109 is a perfect full wave rectified version of the alternating input signal.

Resistor 108 is utilized to bias transistor 100 at a quiescent operating point in order that the output signal at terminal 109 rides about a DC bias level. The DC bias for full wave rectifier as previously suggested is provided between the interconnection of resistor 130 and serially connected diodes 132, 134. As shown by example, diodes 86, 88, 102 may be formed by using diode connected transistor as well may be remaining diodes 132 and 134.

Thus, what has been described above, is a method and circuit for producing a full wave rectified output signal which is linearly related to an alternating signal applied to the input of the full wave rectifier circuit. The full wave rectifier circuit comprises a pair of identical non-linear but symmetrical full wave rectifiers each having its output coupled to a current mirror. The input of the first rectifier is adapted to receive an alternating input signal such that at the output of the current mirror which is coupled to the output of the second rectifier there appears a full wave rectified output signal identical to the full wave rectified output signal produced by the first rectifier. A current feedback source coupled to the output of the current mirror provides an input signal to the second rectifier such that the output of the second rectifier is constrained to be identical to the output of the first rectifier. Thus, the input signal to the second rectifier is a perfect full wave rectified version of the input signal to the first rectifier since the input to the second rectifier is constrained to have one polarity.

Claims

1. A full wave rectifier (40) comprising, first rectifier means (42) adapted to receive an alternating input signal (I_{in}) at an input thereof and producing an output signal that is a full wave rectified version of said alternating input signal (I_{in});

current turnaround means (50) responsive to said output signal (48) from said first rectifier means (42) for producing an output signal (52) at an output substantially identical to said output signal from said first rectifier means (42);

second rectifier means (44) coupled to said output (52) of said current turnaround means (50) having a substantially identical transfer characteristic to said first rectifier means (42); and

linearization circuit means (56) coupled between said output (52) of said current turnaround means (50) and the input of said second rectifier means (44) for providing feedback to said second rectifier means (44) such that the signal appearing at a node at which said output (52) of said current turnaround means (50) and said second rectifier means (44) is combined is substantially an exact full wave rectified version (I_o) of said alternating input signal (I_{in}).

2. The full wave rectifier of claim 1 wherein said first rectifier means (42) comprises:



a first transistor (12) having its emitter electrode coupled to said input, its collector electrode coupled to the output of said first rectifier means, and its base electrode coupled to a first terminal at which is supplied a bias potential;

a second transistor (14) having its emitter electrode coupled to a second terminal at which is supplied a ground reference potential, and its collector electrode coupled to said output; and

first diode means (20) coupled between said emitter electrode of said first transistor (12) and said second terminal.

3. The full wave rectifier of claim 2 wherein said second rectifier means (44) includes:

a third transistor (14'; Fig. 4) having its emitter electrode coupled to said second terminal, its collector electrode coupled to said output of said current turnaround means (50) and its base electrode adapted to receive said feedback from said linearization circuit means (56);

second diode means (20') coupled between said base electrode of said third transistor (14') and said second terminal; and

a fourth transistor (12') having its emitter electrode coupled to said second diode means (20'), its collector electrode coupled to said collector electrode of said third transistor (14') and its base electrode coupled to said first terminal.

4. The full wave rectifier of either claim 2 or claim 3 wherein the base electrode of said second transistor (14) is coupled to the emitter electrode of said first transistor (12).

5. The full wave rectifier of claim 4 wherein said current turnaround means (50) comprises a current mirror.

6. The full wave rectifier of either claim 2 or claim 3 wherein said alternating input signal comprises first and second oppositely phased alternating input signals at first and second inputs (82, 84) respectively, said first input (82) being coupled to the emitter electrode of said first transistor (90) and said second input (84) being coupled to the emitter electrode of said second transistor (92).

7. The full wave rectifier of claim 6 wherein the base electrode of said second transistor (92) is coupled to said first terminal (V_{bias} ; Fig. 5) and further comprising third diode means (88) coupled between the emitter electrode of said second transistor (92) and said second terminal.

8. The full wave rectifier of claim 7 wherein said current turnaround means (96) includes:

a first resistor (112, Fig. 6);

an amplifier (118, 122, 126) having an input and an output, said output and input being coupled across said first resistor (112) with said input being also coupled to said output of said first rectifier means; and

a second resistor (114) of substantially equal value to said first resistor (112), said second resistor (114) being coupled between said output of said amplifier (118, 122, 126) and said output (98) of said current turnaround means (96).

9. The full wave rectifier of claim 8 wherein said linearization circuit means includes a fifth tran-

sistor (100; Fig. 6) having its emitter electrode coupled to said base electrode of said third transistor, its base electrode coupled to said output (98) of said current turnaround means (96) and its collector electrode coupled to an output (I_o) of the full wave rectifier.

Patentansprüche

1. Vollwellengleichrichter (40) enthaltend:

eine erste Gleichrichtereinrichtung (42), die dazu eingerichtet ist, ein Wechseleingangssignal (I_{in}) an einem Eingang derselben entgegenzunehmen und ein Ausgangssignal zu liefern, das eine vollwellengleichgerichtete Version des wechselnden Eingangssignals (I_{in}) ist;

eine Stromumlaufanordnung (50), die auf das Ausgangssignal (48) von der ersten Gleichrichtereinrichtung (42) anspricht, um ein Ausgangssignal (52) an einem Ausgang zu erzeugen, das im wesentlichen identisch mit dem Ausgangssignal von der ersten Gleichrichtereinrichtung (42) ist;

eine zweite Gleichrichtereinrichtung (44), die mit dem Ausgang (52) der Stromumlaufanordnung (50) verbunden ist und eine im wesentlichen identische Übertragungscharakteristik wie die erste Gleichrichtereinrichtung (42) hat, und

eine Linearisierungsschaltungsanordnung (56), die zwischen den Ausgang (52) der Stromumlaufanordnung (50) und den Eingang der zweiten Gleichrichtereinrichtung (44) geschaltet ist, um eine Rückkopplung zu der zweiten Gleichrichtereinrichtung (44) zu erzeugen derart, daß das Signal, das an einem Knoten erscheint, bei welchem der Ausgang (52) der Stromumlaufanordnung (50) und der zweiten Gleichrichtereinrichtung (44) zusammengefaßt wird, im wesentlichen gleich eine exakte vollwellengleichgerichtete Version (I_o) des wechselnden Eingangssignals (I_{in}) ist.

2. Vollwellengleichrichter nach Anspruch 1, bei dem die erste Gleichrichtereinrichtung (42) enthält:

einen ersten Transistor (12), dessen Emittierelektrode mit dem Eingang verbunden ist, dessen Kollektorelektrode mit dem Ausgang der ersten Gleichrichtereinrichtung verbunden ist und dessen Basiselektrode mit einem ersten Anschluß verbunden ist, welchem ein Vorspannungspotential zugeführt wird;

einen zweiten Transistor (14), dessen Emittierelektrode mit einem zweiten Anschluß, dem ein Erdpotential zugeführt ist, verbunden ist und dessen Kollektorelektrode mit dem Ausgang verbunden ist; und

eine erste Diodeneinrichtung (20), die zwischen die Emittierelektrode des ersten Transistors (12) und den zweiten Anschluß geschaltet ist.

3. Vollwellengleichrichter nach Anspruch 2, bei dem die zweite Gleichrichtereinrichtung (44) enthält:

einen dritten Transistor (14'; Fig. 4), dessen Emittierelektrode mit dem zweiten Anschluß verbunden ist, dessen Kollektorelektrode mit dem Ausgang der Stromumlaufanordnung (50) ver-



bunden ist und dessen Basiselektrode dazu eingerichtet ist, die Rückkopplung von der Linearisierungsschaltungsanordnung (56) aufzunehmen;

eine zweite Diodeneinrichtung (20'), die zwischen die Basiselektrode des dritten Transistors (14') und den zweiten Anschluß geschaltet ist; und

einen vierten Transistor (12'), dessen Emittierelektrode mit der zweiten Diodeneinrichtung (20') verbunden ist, dessen Kollektorelektrode mit der Kollektorelektrode des dritten Transistors (14') verbunden ist, und dessen Basiselektrode mit dem ersten Anschluß verbunden ist.

4. Vollwellengleichrichter nach Anspruch 1 oder Anspruch 2, bei dem die Basiselektrode des zweiten Transistors (14) mit der Emittierelektrode des ersten Transistors (12) verbunden ist.

5. Vollwellengleichrichter nach Anspruch 4, bei dem die Stromumlaufanordnung (50) einen Stromspiegel enthält.

6. Vollwellengleichrichter nach Anspruch 2 oder Anspruch 3, bei dem das wechselnde Eingangssignal erste und zweite gegenphasige wechselnde Eingangssignale an ersten bzw. zweiten Eingängen (82, 84) enthält, wobei der erste Eingang (82) mit der Emittierelektrode des ersten Transistors (90) verbunden ist und der zweite Eingang (84) mit der Emittierelektrode des zweiten Transistors (92) verbunden ist.

7. Vollwellengleichrichter nach Anspruch 6, bei dem die Basiselektrode des zweiten Transistors (92) mit dem ersten Anschluß (V_{bias} ; Fig. 5) verbunden ist und weiterhin enthaltend eine dritte Diodeneinrichtung (88), die zwischen die Emittierelektrode des zweiten Transistors (92) und den zweiten Anschluß geschaltet ist.

8. Vollwellengleichrichter nach Anspruch 7, bei dem die Stromumlaufanordnung (96) enthält:

einen ersten Widerstand (112; Fig. 6);

einen Verstärker (118, 122, 126) mit einem Eingang und einem Ausgang, wobei der Ausgang und der Eingang über den ersten Widerstand (112) geschaltet sind, wobei der Eingang außerdem mit dem Ausgang der ersten Gleichrichtereinrichtung verbunden ist; und

einen zweiten Widerstand (114) von im wesentlichen gleichem Wert wie der erste Widerstand (112), wobei der zweite Widerstand (114) zwischen den Ausgang des Verstärkers (118, 122, 126) und den Ausgang (98) der Stromumlaufanordnung (96) geschaltet ist.

9. Vollwellengleichrichter nach Anspruch 8, bei dem die Linearisierungsschaltungsanordnung einen fünften Transistor (100; Fig. 6) enthält, dessen Emittierelektrode mit der Basiselektrode des dritten Transistors verbunden ist, dessen Basiselektrode mit dem Ausgang (98) der Stromumlaufanordnung (96) verbunden ist und dessen Kollektorelektrode mit einem Ausgang (I_o) des Vollwellengleichrichters verbunden ist.

Revendications

1. Redresseur à deux alternances (40), comportant un premier dispositif redresseur (42) agencé

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pour recevoir un signal alternatif d'entrée (lin) à son entrée et produisant un signal de sortie qui est une version redressée à deux alternances dudit signal alternatif d'entrée (lin); un dispositif de renversement de courant (50) réagissant audit signal de sortie (48) dudit premier dispositif redresseur (42) en produisant un signal de sortie (52) à une sortie, pratiquement identique audit signal de sortie dudit premier dispositif redresseur (42); un second dispositif redresseur (44) couplé avec ladite sortie (52) dudit dispositif de renversement de courant (50) ayant une caractéristique de transfert pratiquement identique à celle dudit premier dispositif redresseur (42); et un circuit de linéarisation (56) couplé entre ladite sortie (52) dudit dispositif de renversement de courant (50) et l'entrée dudit second dispositif redresseur (44) pour produire une réaction sur ledit second dispositif redresseur (44) de manière que le signal apparaissant à un point auquel ladite sortie (52) dudit dispositif de renversement de courant (50) et ledit second dispositif redresseur (44) sont combinés soit pratiquement une version exacte redressée à deux alternances (lo) dudit signal alternatif d'entrée (lin).

2. Redresseur à deux alternances selon la revendication 1, dans lequel ledit premier dispositif redresseur (42) comporte: un premier transistor (12) dont l'électrode d'émetteur est connectée à ladite entrée, dont l'électrode de collecteur est connectée à la sortie dudit premier dispositif redresseur et dont l'électrode de base est couplée à une première borne à laquelle est appliqué un potentiel de polarisation; un second transistor (14) dont l'électrode d'émetteur est couplée avec une seconde borne à laquelle est appliqué un potentiel de référence de masse et dont l'électrode de collecteur est connectée à ladite sortie; et une première diode (20) connectée entre ladite électrode d'émetteur dudit premier transistor (12) et ladite seconde borne.

3. Redresseur à deux alternances selon la revendication 2, dans lequel ledit second dispositif redresseur (44) comporte: un troisième transistor (14') figure 4) dont l'électrode d'émetteur est connectée à ladite seconde borne, dont l'électrode de collecteur est connectée à ladite sortie dudit dispositif de renversement de courant (50) et dont l'électrode de base est adaptée pour recevoir ladite réaction dudit circuit de linéarisation (56); une seconde diode (20') connectée entre ladite électrode de base dudit troisième transistor (14') et ladite seconde borne; et un quatrième transistor (12') dont l'électrode d'émetteur est connectée à ladite seconde diode (20'), dont l'électrode de collecteur est connectée à ladite électrode de collecteur dudit troisième transistor (14') et dont l'électrode de base est connectée à ladite première borne.

4. Redresseur à deux alternances selon la revendication 2 ou la revendication 3, dans lequel l'électrode de base dudit second transistor (14) est connectée à l'électrode d'émetteur dudit premier transistor (12).

5. Redresseur à deux alternances selon la



revendication 4, dans lequel ledit dispositif de renversement de courant (50) consiste en un miroir de courant.

6. Redresseur à deux alternances selon la revendication 2 ou la revendication 3, dans lequel ledit signal alternatif d'entrée consiste en un premier et un second signaux alternatifs d'entrée de phases opposées à une première et une seconde entrée (82, 84) respectivement, ladite première entrée (82) étant couplée avec l'électrode d'émetteur dudit premier transistor (90) et ladite seconde entrée (84) étant couplée avec l'électrode d'émetteur dudit second transistor (92).

7. Redresseur à deux alternances selon la revendication 6, dans lequel l'électrode de base dudit second transistor (92) est couplée avec ladite première borne (V_{bias} ; figure 5) et comportant en outre une troisième diode (88) couplée entre l'électrode d'émetteur dudit second transistor (92) et ladite seconde borne.

8. Redresseur à deux alternances selon la revendication 7, dans lequel ledit dispositif de

renversement de courant (96) comporte: une première résistance (112; figure 6); un amplificateur (118, 122, 126) comprenant une entrée et une sortie, ladite sortie et ladite entrée étant couplées aux bornes de ladite première résistance (112), ladite entrée étant également couplée avec ladite sortie dudit premier dispositif redresseur; et une seconde résistance (114) de valeur pratiquement égale à celle de la première résistance (112), ladite seconde résistance (114) étant connectée entre ladite sortie dudit amplificateur (118, 122, 126) et ladite sortie (48) dudit dispositif de renversement de courant (96).

9. Redresseur à deux alternances selon la revendication 8, dans lequel ledit circuit de linéarisation comporte un cinquième transistor (100; figure 6) dont l'électrode d'émetteur est couplée avec ladite électrode de base dudit troisième transistor, dont l'électrode de base est couplée avec ladite sortie (98) dudit dispositif de renversement de courant (96) et dont l'électrode de collecteur est couplée avec une sortie (10) du redresseur à deux alternances.

