What is claimed:

1. A device for use, with a print head, comprising

a plurality of memory banks storing data related to the print head, each memory bank comprising an array of memory units; and

a plurality of shift registers connected to the plurality of memory banks,

wherein, to address one of the memory units in the plurality of memory banks, the plurality of shift registers is to receive data signals and generate a three-dimensional address, the three-dimensional address comprising:

a row select signal, representing a first dimension of the three-dimensional address, to identify a row portion of an address of the memory unit in the plurality of memory banks,

a column select signal, representing a second dimension of the three-dimensional address, to identify a column portion of the address of the memory unit in the plurality of memory banks, and

a bank select signal, representing a third dimension of the three-dimensional address, generated by one of the plurality of shift registers to identify a specific memory bank of the plurality of memory banks where the memory unit is located.

2. The device of claim 1, wherein the data signals include first, second, and third data signals, and wherein the plurality of shift registers includes;

a first shift register to receive the first data signal and generate the row select signal, a second shift register to receive the second data signal and generate the column select signal, and

a third shift register to receive the third data signal and generate the bank select signal.

3. The device of claim 2, wherein each of the plurality of shift registers is to accept a number of inputs including a corresponding data signal and a number of corresponding select signals, wherein the corresponding data signal initiates a corresponding shift register and specifies the row portion and the column portion of the three-dimensional address, wherein the corresponding select signals precharge and advance the corresponding shift register, and wherein the corresponding shift register is advanced by one stage upon cycling through four of the corresponding select signals.

4. The device of claim 1, wherein the data signals include a first data signal, a second data signal, and a third data signal, and wherein the plurality of shift registers includes:

a first shift register to receive the first and second data signals and generate the row select signal and the column select signal, respectively, and

a second shift register to receive the third data signal and generate the bank select signal.

5. The device of claim 1, wherein, to address two of the memory units in the plurality of memory banks, the plurality of shift registers is to:

during a first clock cycle, generate a first bank select signal that identifies a first memory bank of the plurality of memory banks, wherein the row select signal, the column select signal, and the first bank select signal are used to identify a location of a first memory unit in the first memory bank, and

during a second clock cycle, generate a second bank select signal that identifies a second memory bank of the plurality of memory banks, wherein the row select signal, the column select signal, and the second bank select signal are used to identify a location of a second memory unit in the second memory bank.

6. The device of claim 1, wherein the bank select data signal specifies more than one of the plurality of memory banks associated with the row portion and the column portion to generate a parallel three-dimensional address.

7. The device of claim 1, wherein each of the plurality of memory banks is an erasable programmable read only memory (EPROM) bank.

8. A method for addressing a memory unit in a plurality of memory banks storing data related to a print head, comprising:

receiving, by a plurality of shift registers, data signals;

generating, by the plurality of shift registers, a three-dimensional address to the plurality of memory banks in response to the data signals, the three-dimensional address including:

a row select signal, representing a first dimension of the three-dimensional address, to identify a row portion of an address of the memory unit in the plurality of memory banks, a column select signal, representing a second dimension of the three-dimensional address, to identify a column portion of the address of the memory unit in the plurality of memory banks, and

a bank select signal, representing a third dimension of the three-dimensional address, to identify a specific memory bank of the plurality of memory banks where the memory unit is located; and

addressing, by the plurality of shift registers, the memory unit in the plurality of memory banks based on the row select signal, the column select signal, and the bank select signal.

9. The method of claim 8, wherein the data signals include first, second, and third data signals, the plurality of shift registers includes first, second, and third shift registers, and the method comprises:

receiving, by the first shift register, the first data signal and generating the row select signal,

receiving, by the second shift register, the second data signal and generating the column select signal, and

receiving, by the third shift register, the third data signal and generating the bank select signal.

10. The method of claim 9, wherein each of the plurality of shift registers is to accept a number of inputs including a corresponding data signal and a number of corresponding select signals, wherein the corresponding data signal initiates a corresponding shift register and specifies the row portion and the column portion of the three-dimensional address, wherein the corresponding select signals precharge and advance a corresponding shift register, and wherein the corresponding shift register is advanced by one stage upon cycling through four of the corresponding select signals.

11. The method of claim 8, wherein the data signals include first, second, and third data signals, the plurality of shift registers includes first and second shift registers, and the method comprises:

receiving, by the first shift register, the first data signal and generating the row select signal,

receiving, by the first shift register, the second data signal aid generating the column select signal, and

receiving, by the second shift register, the third data signal and generating the bank select signal.

12. The method of claim 8, further comprising:

during a first clock cycle, generating, by the plurality of shift registers, a first bank select signal that identifies a first memory bank of the plurality of memory banks;

addressing a first memory unit in the first memory bank based on the row select signal, the column select signal, and the first bank select signal;

during a second clock cycle, generating, by the plurality of shift registers, a second bank select signal that identifies a second memory bank of the plurality of memory banks; and

addressing a second memory unit in the second memory bank based on the row select signal, the column select signal, and the second bank select signal.

13. A system for use with a print head, comprising:

a plurality of shift registers to receive data signals and generate a three-dimensional address to locate a memory unit within a plurality of memory banks storing data related to the print head, the plurality of shift registers comprising:

a first shift register to receive a first data signal and generate a row select signal representing a first dimension of the three-dimensional address to identify a row portion of an address of the memory unit in the plurality of memory banks,

a second shift register to receive a second data signal and generate a column select signal representing a second dimension of the three-dimensional address to identify a column portion of the address of the memory unit in the plurality of memory banks, and

a third shift register to receive a third data signal and generate a bank select signal representing a third dimension of the three-dimensional address to identify a specific memory bank of the plurality of memory banks where the memory unit is located,

wherein the row select signal, the column select signal, and the bank select signal are transmitted to the plurality of memory banks to address the memory unit.

14. The system of claim 13, wherein the third shift register is to:

during a first clock cycle, generate a first bank select signal that identifies a first memory bank of the plurality of memory banks, wherein the row select signal, the column select signal, and the first bank select signal are used to locate a first memory unit in the first memory bank, and

during a second dock cycle, generate a second bank select signal that identifies a second memory bank of the plurality of memory banks, wherein the row select signal, the column select signal, and the second bank select signal are used to locate a second memory unit in the second memory bank.

15. The system of claim 13, wherein the bank select data signal specifies more than one of the plurality of memory banks associated with the row portion and the column portion to generate a parallel three-dimensional address.