[CLAIMS]

1. An information processing device comprising:

a decoding circuit, provided on a data bus for connecting a main memory and an external storage device, which is capable of switching between enabling and disabling a process for decoding information that is transmitted through the data bus; and

a readout processing unit that is configured to read out information written in the external storage device into the main memory,

wherein the readout processing unit is configured to enable the decoding process of the decoding circuit in a case where a snapshot image of the main memory is read out as the information written in the external storage device.

2. The information processing device according to claim 1, further comprising:

an encoding circuit, provided on the data bus, which is capable of switching between enabling and disabling a process for encoding the information that is transmitted through the data bus; and

a writing processing unit that writes information stored in the main memory in the external storage device,

wherein the writing processing unit is configured to enable the encoding process of the encoding circuit in a case where a snapshot image of the main memory is written as the information stored in the main memory.

3. The information processing device according to claim 1, wherein the decoding circuit includes

a logical arithmetic operation element that is configured to perform the decoding process, and

a selection element capable of selecting whether the information that is transmitted through the data bus passes through the logical arithmetic operation element in accordance with a control signal that is input.

4. The information processing device according to claim 1, further comprising a data recording memory for decoding in which data for decoding is recorded,

wherein the decoding circuit performs the process for decoding the information that is transmitted through the data bus on the basis of the data for decoding read out from the data recording memory for decoding.

5. The information processing device according to claim 4, wherein the data for decoding is information recorded in the main memory in an initial state immediately after power-on.

6. A method for controlling an information processing device including a decoding circuit, provided on a data bus for connecting a main memory and an external storage device, which is capable of switching between enabling and disabling a process for decoding information that is transmitted through the data bus,

wherein the method comprises a readout step of reading out information written in the external storage device into the main memory, and

the decoding process of the decoding circuit is enabled in the readout step in a case where a snapshot image of the main memory is read out as the information written in the external storage device.

7. A non-transitory computer readable medium that records a program causing an information processing device including a decoding circuit that is provided on a data bus for connecting a main memory and an external storage device and is capable of switching between enabling and disabling a process for decoding information transmitted through the data bus to function as a readout processing unit that is configured to read out information written in the external storage device into the main memory,

wherein the readout processing unit is configured to enable the decoding process of the decoding circuit in a case where a snapshot image of the main memory is read out as the information written in the external storage device.