FeRAM devices may thus have improved performance compared to other non-volatile and volatile memory devices. It is desirable, however, to improve the operation of FeRAM devices. For example, it may be desirable to have improved noise resistance during memory cell sensing, more compact circuits and reduced layout size, and improved timing for operation of FeRAM devices.

SUMMARY

**[005]** Apparatuses and methods are disclosed that include ferroelectric memory and for accessing ferroelectric memory. In an aspect of the disclosure, an example method includes increasing a voltage of a first cell plate of a capacitor to change the voltage of a second cell plate of the capacitor, a second digit line, and a second sense node. The voltage of the second cell plate and the second digit line is decreased to change the voltage of the first cell plate, a first digit line, and a first sense node. The first node is driven to a first voltage and the second node is driven to a second voltage responsive to the voltage of the first node being greater than the second node. The first node is driven to the second voltage and the second node is driven to the first voltage responsive to the voltage of the first node being less than the second node.

**[006]** In another aspect of the disclosure, an example apparatus includes first and second digit lines, a ferroelectric memory cell, first and second word lines, a sense component, and first and second drivers. The ferroelectric memory cell includes a ferroelectric capacitor, a first selection component, and a second selection component. The first selection component is coupled between the first digit line and a first plate of the ferroelectric capacitor and the second selection component is coupled between the second digit line and a second plate of the ferroelectric capacitor. The first word line is coupled to a gate of the first selection component and the second word line is coupled to a gate of the second selection component. The sense component includes a first sense node coupled to the first digit line through a switch and further includes a second sense node coupled to the second digit line through an isolation switch. The sense component is configured to latch voltages of the first and second sense nodes. The first driver circuit is coupled to the first digit line and configured to provide a read voltage when activated. The second driver circuit is coupled to the second digit line and configured to provide a ground voltage when activated.

**[024]** A memory cell 105 may be programmed, or written, by activating the relevant word lines 110 and digit lines 115. As discussed above, activating word lines 110 electrically couples the corresponding row of memory cells 105 to their respective digit lines 115. By controlling the relevant digit lines 115 while the word lines 110 are activated, a memory cell 105 may be written—e.g., a logic value may be stored in the memory cell 105. Column decoder 130 may accept data, for example input 135, to be written to the memory cells 105. A ferroelectric memory cell 105 may be written by applying a voltage across the ferroelectric capacitor. This process is discussed in more detail below.

**[025]** In some memory architectures, accessing the memory cell 105 may degrade or destroy the stored logic state, and re-write (e.g., restore) operations may be performed to return the original logic state to memory cell 105. For example, the capacitor may be partially or completely discharged during a sense operation, corrupting the stored logic state. So the logic state may be re-written after a sense operation. Additionally, activating word lines 110 may result in the discharge of all memory cells in the row. Thus, several or all memory cells 105 in the row may need to be re-written.

**[026]** The memory controller 140 may control the operation (e.g., read, write, re-write, etc.) of memory cells 105 through the various components, such as row decoder 120, column decoder 130, and sense component 125. Memory controller 140 may generate row and column address signals in order to activate the desired word lines 110 and digit lines 115. Memory controller 140 may also generate and control various voltage potentials used during the operation of memory array 100. In general, the amplitude, shape, or duration of an applied voltage discussed herein may be adjusted or varied and may be different for the various operations for operating memory array 100. Furthermore, one, multiple, or all memory cells 105 within memory array 100 may be accessed simultaneously. For example, multiple or all cells of memory array 100 may be accessed simultaneously during a reset operation in which all memory cells 105, or a group of memory cells 105, are set to a single logic state.

**[027]** Figure 2A illustrates an example circuit 200 that includes a column of memory cells according to an embodiment of the present disclosure. Figure 2A illustrates an example circuit 200 that includes memory cells 105 in accordance with various embodiments of the present disclosure. Circuit 200 includes memory cells 105 MC(0)-

MC(n), where “n” depends on the array size. The circuit 200 further includes word lines WL-CT(0)-WL-CT(n) and WL-CB(0)-WL-CB(n), digit lines BL-CT and BL-CB, and sense component 125. The word lines, digit lines, and sense component may be examples of memory cells 105, word lines 110, digit lines 115, and sense component 125, respectively, as described with reference to Figure 1. While one column and n rows of memory cells 105 are shown in Figure 2A, a memory array may include many columns and rows of memory cells as those shown.

**[028]** Memory cells 105 may include a logic storage component, such as capacitor 205 that has a first plate, cell top 230, and a second plate, cell bottom 215. Cell tops 230 and cell bottoms 215 may be capacitively coupled through a ferroelectric material positioned between them. The orientation of cell tops 230 and cell bottoms 215 may be flipped without changing the operation of memory cell 105. The memory cells 105 may further include selection components 220 and 224. The selection components 220 and 224 may be transistors, for example, n-type field effect transistors. In such an example, each of the memory cells 105 includes two transistors and one capacitor (e.g., 2T1C).

**[029]** Circuit 200 also includes isolation switch 231 and reference switch 233. A reference signal VBLREF is provided to the reference switch 233. The isolation switch 231 and the reference switch 233 are coupled to a sense node A of the sense component 125. Activation of the isolation switch 231 is controlled by a signal ISO and activation of the reference switch 233 is controlled by a signal ISOREF. In some embodiments, the reference switch 233 is not included in the circuit 200. For example, in embodiments where the circuit 200 provides on its own reference voltage for determining the logic value stored by a memory cell 105. In such embodiments, providing a separate reference voltage (e.g., the voltage VREF of the VBLREF reference signal) to the sense component 125 is not necessary. Circuit 200 also includes switch 235 and driver circuits 237 and 239. In some examples, isolation switch 231, reference switch 233, and switch 235 may be transistors, for example, n-type field effect transistors, which may be activated by applying a voltage equal to or greater than its threshold voltage. Activation of the switch 235 is controlled by a signal RESTORE. The driver circuit 237 provides a VREAD voltage when activated and the driver circuit 239 provides a ground voltage (GND) when activated.

cell 105 to restore the original data state read. By restoring the data, a separate restore operation is unnecessary.

**[035]** As previously described, the word lines WL-CB and WL-CT and the selection components 220 and 224 provide independent control of cell bottom 215 and cell top 230 of the capacitor 205, thus, removing the need for a shared cell plate, as is typical with conventional ferroelectric memories. As a result, the cells may be less susceptible to disturb mechanisms, for example, cell plate related pattern noise. Additionally, cell plate driver circuits, which are needed for shared cell plate designs, are not needed which can reduce circuit size. The digit lines of the plurality of columns of memory cells may be driven to voltages independently of one another. For example, the digit line BL-CT (the digit line coupled through a selection component to the cell top, which is opposite of the cell bottom) of a first column of memory cells may be driven to a voltage independently of the voltage to which the digit line BL-CT of a second column of memory cells are driven.

**[036]** Figure 2B illustrates a sense component 125 according to an embodiment of the disclosure. The sense component 125 includes p-type field effect transistors 252 and 256 and n-type field effect transistors 262 and 266. Gates of the transistor 252 and transistor 262 are coupled to sense node A. Gates of the transistor 256 and transistor 266 are coupled to sense node B. The transistors 252 and 256, and the transistors 262 and 266 represent a sense amplifier. A p-type field effect transistor 258 is configured to be coupled to a power supply (e.g., VREAD voltage power supply) and is coupled to a common node of the transistors 252 and 256. The transistor 258 is activated by an active PSA signal (e.g., active low logic). An n-type field effect transistor 268 is configured to be coupled to a sense amplifier reference voltage (e.g., ground) and is coupled to a common node of the transistors 262 and 266. The transistor 268 is activated by an active NSA signal (e.g., active high logic). Reference switch 233 coupled to sense node A is also shown in Figure 2B. A reference signal VBLREF is provided to the reference switch 233. Activation of the reference switch 233 is controlled by a signal ISOREF. As previously described, in some embodiments, the reference switch 233 is not included in the circuit 200, such as in embodiments where the circuit 200 provides on its own reference voltage for determining the logic value stored by a memory cell 105. In such embodiments, providing a separate reference

ferroelectric capacitor (e.g., capacitor 205 of Figure 2A) as a function of a voltage difference, V.

**[041]** A ferroelectric material is characterized by a spontaneous electric polarization, for example, it maintains a non-zero electric polarization in the absence of an electric field. Example ferroelectric materials include barium titanate ($BaTiO_3$), lead titanate ($PbTiO_3$), lead zirconium titanate (PZT), and strontium bismuth tantalate (SBT). The ferroelectric capacitors described herein may include these or other ferroelectric materials. Electric polarization within a ferroelectric capacitor results in a net charge at the ferroelectric material's surface and attracts opposite charge through the capacitor terminals. Thus, charge is stored at the interface of the ferroelectric material and the capacitor terminals. Because the electric polarization may be maintained in the absence of an externally applied electric field for relatively long times, even indefinitely, charge leakage may be significantly decreased as compared with, for example, capacitors employed in volatile memory arrays. This may reduce the need to perform refresh operations as described above for some volatile memory architectures.

**[042]** Hysteresis curves 300 may be understood from the perspective of a single terminal of a capacitor. By way of example, if the ferroelectric material has a negative polarization, positive charge accumulates at the terminal. Likewise, if the ferroelectric material has a positive polarization, negative charge accumulates at the terminal. Additionally, it should be understood that the voltages in hysteresis curves 300 represent a voltage difference across the capacitor and are directional. For example, a positive voltage may be realized by applying a positive voltage to the terminal in question (e.g., a cell top 230) and maintaining the second terminal (e.g., a cell bottom 215) at ground (or approximately zero volts (0V)). A negative voltage may be applied by maintaining the terminal in question at ground and applying a positive voltage to the second terminal, for example, positive voltages may be applied to negatively polarize the terminal in question. Similarly, two positive voltages, two negative voltages, or any combination of positive and negative voltages may be applied to the appropriate capacitor terminals to generate the voltage difference shown in hysteresis curves 300.

**[043]** As depicted in hysteresis curve 300-a, the ferroelectric material may maintain a positive or negative polarization with a zero voltage difference, resulting in two possible charged states: charge state 305 and charge state 310. According to the

analysis. Charge states 305-c and 310-c may be defined with respect to the digit line capacitance. As a result, the voltage of the capacitor, voltage 350 or voltage 355, may be different and may depend on the initial state of the capacitor.

**[047]** By comparing the digit line voltage to a reference voltage, the initial state of the capacitor may be determined. The digit line voltage may be the difference between voltage 335 and the final voltage across the capacitor, voltage 350 or voltage 355 (e.g., voltage 335 – voltage 350) or (e.g., voltage 335 – voltage 355). A reference voltage may be generated such that its magnitude is between the two possible digit line voltages in order to determine the stored logic state, for example, if the digit line voltage is higher or lower than the reference voltage. For example, the reference voltage may be an average of the two quantities (voltage 335 – voltage 350) and (voltage 335 – voltage 355). In another example, the reference voltage may be provided by isolating a voltage on first sense node of a sense component, then causing a voltage change on a second sense node of the sense component through a digit line, and comparing the resulting voltage of the second sense node with the isolated voltage of the first sense node. Upon comparison by the sense component, the sensed digit line voltage may be determined to be higher or lower than the reference voltage, and the stored logic value of the ferroelectric memory cell (e.g., a logic 0 or 1) may be determined.

**[048]** Figures 4A-4E are timing diagrams of various signals during a read operation according to an embodiment of the disclosure. Figures 4A-4E will be described with reference to memory array 100 and example circuit 200 of Figures 1 and 2. The example read operation of Figures 4A-4E may provide increased voltage margin relative to a reference voltage used to determine the stored state (and the corresponding logic value) of a memory cell.

**[049]** Prior to time T0 the digit line BL-CB is coupled to the sense node A of the sense component 125 through an activated isolation switch 231. The switch 235 is deactivated so that the voltage of the digit line BL-CT and the voltage of the sense node B are independent of one another. The digit line BL-CB and sense node A, and the digit line BL-CT and sense node B are all precharged to a voltage, such as ground. At time T0, the word line WL-CB is activated to activate the selection component 220 to couple the cell bottom 215 to the digit line BL-CB. At time T1 the driver circuit 237

230 of capacitor 205, and the pillar 202 extends from the digit line BL-CB to the cell bottom 215 of capacitor 205.

**[085]** The selection component 224 has source/drain region 214 extending to the cell top 230 of capacitor 205, and has source/drain region 216 extending to the digit line BL-CT. The selection component 224 also has channel region 218 between the source/drain regions 214 and 216. Gate 211 is along the channel region 218 and offset from the channel regions by gate dielectric material 213. The gate 211 may be included in a word line WL-CT.

**[086]** The selection component 220 has source/drain region 204 extending to the cell bottom 215 of capacitor 205, and has source/drain region 206 extending to the digit line BL-CB. The selection component 220 also has channel region 208 between the source/drain regions 204 and 206. Gate 201 is along the channel region 208 and offset from the channel regions by gate dielectric material 203. The gate 201 may be included in a word line WL-CB.

**[087]** As shown in the embodiment of Figure 8, the selection components 220 and 224 and capacitor 205 of the memory cell 105 are vertically stacked, which may enable memory cells 105 to be packed to high levels of integration.

**[088]** In some embodiments, the relative orientations of digit lines BL-CT and BL-CB are reversed so that the digit line BL-CT is over a supporting substrate 15 and the digit line BL-CB is over the digit line BL-CT. In such other embodiments the illustrated capacitors 205 would be inverted relative to the shown configuration of Figure 8 and accordingly container shaped cell tops 230 would open upwardly instead of downwardly.

**[089]** Figure 9 illustrates a block diagram of a portion of memory 900 that includes memory array 100 that supports a ferroelectric memory in accordance with various embodiments of the present disclosure. Memory array 100 may be referred to as an electronic memory apparatus and includes memory controller 140 and memory cell 105, which may be examples of memory controller 140 and memory cell 105 described with reference to Figures 1, 2, or 4-7.

**[090]** Memory controller 140 may include biasing component 905 and timing component 910, and may operate memory array 100 as described in Figure 1. Memory controller 140 may be in electronic communication with word lines 110, digit lines 115,

voltage responsive to increasing the voltage of the first cell plate for a second polarization of the capacitor, the first and second voltages are different.

6. The method of claim 5 wherein decreasing the voltage of the second cell plate and the second digit line comprises decreasing the voltage of the second cell plate from the first or second increased to the initial voltage.

7. A method, comprising:

providing a read voltage to a first digit line and to a first plate of a capacitor coupled to the first digit line to cause a voltage of a second plate of the capacitor, of a second digit line coupled to the second plate of the capacitor, and of a second sense node of a sense component to change from an initial voltage to an increased voltage, the second sense node coupled to the second digit line;

coupling a first sense node of the sense component to the first digit line;

decoupling the second sense node from the second digit line;

driving the voltage of the second digit line and the second plate of the capacitor from the increased voltage to the initial voltage to cause a voltage of the first plate of the capacitor, the first digit line, and the first sense node to change;

comparing at the sense component the voltage of the first sense node to a reference voltage; and

based on the comparison, driving the first sense node, first digit line, and first plate of the capacitor to a first voltage and driving the second sense node, second digit line, and second plate of the capacitor to a second voltage, the second voltage complementary to the first voltage.

8. The method of claim 7, further comprising activating selection components to couple the first plate of the capacitor to the first digit line and to couple the second plate of the capacitor to the second digit line.

9. The method of claim 7, further comprising:

changing the voltage of the first and second plates of the capacitor to a same voltage; and

deactivating selection components to isolate the first plate and the second plate of the capacitor from the first and second digit lines, respectively.

10. The method of claim 7 wherein the initial voltage is ground.

11. The method of claim 7 wherein driving the first sense node, first digit line, and first plate of the capacitor to a first voltage and driving the second sense node, second digit line, and second plate of the capacitor to a second voltage, the second voltage complementary to the first voltage, comprises:

driving the first sense node, first digit line, and first plate of the capacitor to ground and driving the second sense node, second digit line, and second plate of the capacitor to the read voltage responsive to the voltage of the first sense node being less than the reference voltage; and

driving the first sense node, first digit line, and first plate of the capacitor to the read voltage and driving the second sense node, second digit line, and second plate of the capacitor to ground responsive to the voltage of the first sense node being greater than the reference voltage.

12. The method of claim 7 wherein the reference voltage is a constant voltage.

13. The method of claim 7 wherein the reference voltage is a first reference voltage responsive to a first increased voltage and wherein the reference voltage is a second reference voltage that is different than the first reference voltage responsive to a second increased voltage.

14. A method, comprising:

coupling a voltage increase across a capacitor from a first plate to a second plate, a resulting voltage at the second plate provided to a sense component, the resulting voltage at the second plate having a first voltage responsive to the capacitor having a first polarization and having a second voltage responsive to the capacitor having a second polarization;