What is claimed is:

1. A semiconductor memory device comprising:

a memory cell array including a plurality of memory blocks, each of the plurality of memory blocks including a plurality of dynamic memory cells coupled to word-lines and bit-lines, wherein each of the plurality of memory blocks are divided into a plurality of row blocks by at least one row block identity bit corresponding to a portion of bits of a row address, and each of the row blocks includes a plurality of sub-array blocks arranged in a first direction;

a row decoder configured to activate a first word-line in a first row block of the plurality of row blocks in response to the row address, configured to activate a second word-line in a second row block of the plurality of row blocks, the second row block being different from the first row block, when the first row block includes at least one defective cell, and configured to output a row block information signal indicating whether the second word-line is activated, wherein the first row block is associated with a first segment of a plurality of segments, the second row block is associated with a second segment of the plurality of segments, the second segment being different from the first segment, and the plurality of memory blocks are divided into the plurality of segments in a second direction crossing the first direction; and

a column decoder configured to receive the row block information signal and to repair a first bit-line coupled to the at least one defective cell with one of a first spare bit-line in the first segment and a second spare bit-line in the second segment in response to a column address and the row block information signal.

2. The semiconductor memory device of claim 1,

wherein each of the plurality of segments includes a plurality of bit-lines and at least one spare bit-line,

wherein the row address is received with an active command, and

wherein the column address is received with a write command or a read command.

3. The semiconductor memory device of claim 1 or claim 2,

wherein the row decoder includes a plurality of row block fuse circuits, each row block fuse circuit corresponding to one of the plurality of row blocks, and

wherein each of the plurality of row block fuse circuits includes:

a row block information storage table configured to store a defective row block address associated with a defective row block including the at least one defective cell, a row block address information of a corresponding row block, a replacement row block information to determine whether to activate the second word-line and a master fuse bit, the master fuse bit indicating whether the corresponding row block is capable of being used as a replacement row block;

a row block comparator configured to compare the at least one row block identity bit with the defective row block address to output a row block match signal; and

a signal generator configured to provide the column decoder with the row block information signal associated with the row block match signal and configured to output a first activation signal associated with activation of the second word-line, based on the row block match signal and the replacement row block information,

wherein the row block information storage table is configured to provide the replacement row block information to the signal generator in response to the row block match signal.

4. The semiconductor memory device of any one of claims 1 to 3, wherein the column decoder includes:

a plurality of sub column decoders corresponding to the plurality of memory blocks; and

a plurality of repair circuits corresponding to the plurality of sub column decoders, and

wherein each of the plurality of repair circuits is configured to apply a first repair signal, a second repair signal and an internal enable signal to a corresponding sub column decoder of the plurality of sub column decoders, the internal enable signal being associated with activation of the second word-line.

5. The semiconductor memory device of claim 4, wherein a repair circuit of the plurality of repair circuits corresponding to a first memory block of the plurality of memory blocks is configured to repair the first bit-line with the first spare bit-line by activating the first repair signal and is configured to repair the first bit-line with the second spare bit-line by activating the second repair signal.

6. The semiconductor memory device of claim 4 or claim 5, wherein each of the plurality of repair circuits includes:

a fail address storage table configured to store fail column address information associated with column address information of defective cells of a corresponding memory block of the plurality of memory blocks;

a column address comparator configured to compare the column address with the fail column address information to output a column match signal indicating whether the

column address matches the fail column address information;

a fuse circuit that includes a plurality of fuse sets, wherein each of the plurality of fuse sets stores a spare bit-line information on a spare bit-line of each of the segments in the corresponding memory block, and a master fuse bit associated with a usability of a spare bit-line of a corresponding segment;

a signal generator configured to generate the internal enable signal associated with the activation of the second word-line based on the row block information signal, the spare bit-line information, and the master fuse bit; and

a repair signal generator configured to selectively activate the first repair signal and the second repair signal based on the column match signal and the master fuse bit.

7. The semiconductor memory device of any one of claims 4 to 6, wherein each of the plurality of sub column decoders includes:

a column selection line driver configured to select a column selection line to select the first bit-line in the first segment in response to the column address and a column match signal output by a corresponding repair circuit of the plurality of repair circuits; and

a spare column selection line driver configured to selectively activate a second enable signal associated with the second segment and configured to select a spare column selection line to select the spare column selection line such that data is input and output through the first spare bit-line in the first segment or the second spare bit-line in the second segment in response to the column match signal, the first repair signal, the second repair signal and the internal enable signal.

8. The semiconductor memory device of claim 7, wherein the column

selection line driver is configured to select the column selection line corresponding to the column address when the column match signal indicates that the column address does not match a fail column address information.

9. The semiconductor memory device of claim 7 or claim 8, wherein the spare column selection line driver is configured to deactivate the second enable signal and configured to select the spare column selection line such that the data is input and output through the first spare bit-line in the first segment when the column match signal indicates that the column address matches a fail column address information and the first repair signal is activated.

10. The semiconductor memory device of any one of claims 7 to 9, wherein the spare column selection line driver is configured to deactivate the second enable signal and configured to select the spare column selection line such that the data is input and output through the second spare bit-line in the second segment when the column match signal indicates that the column address matches a fail column address information and the second repair signal is activated.

11. The semiconductor memory device of any one of claims 4 to 10,

wherein the plurality of segments are disposed in the first direction and the second direction of a substrate, and

wherein the memory cell array further includes:

a plurality of sub word-line driver regions disposed between the plurality of segments in the first direction;

a plurality of bit-line sense amplifier regions disposed between the plurality of

segments in the second direction; and

a plurality of local sense amplifier circuits disposed in the plurality of bit-line sense amplifier regions.

12. The semiconductor memory device of claim 11, wherein the memory cell array further includes:

a logic gate configured to perform a logical operation on a first enable signal and a second enable signal associated with activation of the second segment to provide a local enable signal to a corresponding local sense amplifier circuit of the plurality of local sense amplifier circuits.

13. The semiconductor memory device of claim 12, wherein the corresponding local sense amplifier circuit corresponding to the second segment is activated and data is input and output through the second spare bit-line in the second segment.

14. The semiconductor memory device of any one of claims 1 to 13, further comprising:

a peripheral circuit configured to control the row decoder and the column decoder in response to a command and an address received from an external device,

wherein the peripheral circuit includes an error correction code (ECC) engine configured to perform ECC encoding on data to be stored in the memory cell array and configured to perform ECC decoding on data read from the memory cell array.

15. The semiconductor memory device of claim 14, wherein the peripheral

circuit is configured to control repair of the first bit-line with one of the first spare bit-line and the second spare bit-line based on error correction capability of the ECC engine.

16. The semiconductor memory device of any one of claims 1 to 15, comprising:

first group dies including at least one buffer die; and

second group dies including a plurality of memory dies, wherein the plurality of memory dies are stacked on the first group dies and configured to convey data through a plurality of through silicon via (TSV) lines,

wherein each of the plurality of memory dies includes a plurality of dynamic memory cells, and

wherein the at least one buffer die includes the row decoder and the column decoder.

17. A semiconductor memory device comprising:

a memory cell array including a plurality of memory blocks, each of the plurality of memory blocks including a plurality of dynamic memory cells coupled to word-lines and bit-lines, wherein each of the plurality of memory blocks is divided into a plurality of row blocks by row block identity bits corresponding to a portion of bits of a row address, and each of the row blocks includes a plurality of sub-array blocks arranged in a first direction; and

an address decoder configured to change a physical row address of a memory cell that stores or outputs data based on a column address received with a write command or a read command,

wherein the address decoder includes:

a row decoder configured to activate a first word-line in a first row block of the plurality of row blocks in response to the row address, configured to activate a second word-line in a second row block of the plurality of row blocks different from the first row block when the first row block includes at least one defective cell and configured to output a row block information signal indicating whether the second word-line is activated, wherein the first row block is associated with a first segment of a plurality of segments, the second row block is associated with a second segment of the plurality of segments different from the first segment, and the plurality of memory blocks are divided into the plurality of segments in a second direction crossing the first direction; and

a column decoder configured to receive the row block information signal output from the row decoder and to repair a first bit-line coupled to the at least one defective cell with one of a first spare bit-line in the first segment and a second spare bit-line in the second segment in response to the column address and the row block information signal.

18. The semiconductor memory device of claim 17,

wherein the row address is received with an active command.

19. A method of operating a semiconductor memory device, wherein the semiconductor memory device includes a memory cell array including a plurality of memory blocks, each of the plurality of memory blocks including a plurality of dynamic memory cells coupled to word-lines and bit-lines, wherein each of the plurality of memory blocks is divided into a plurality of row blocks by a row block identity bit corresponding to a portion of bits of a row address, and each of the row blocks includes a plurality of sub-array blocks arranged in a first direction, the method comprising:

activating, by a row decoder, a first word-line in a first row block of the plurality

of row blocks in response to the row address;

activating a second word-line in a second row block of the plurality of row blocks different from the first row block when the first row block includes at least one defective cell;

outputting, by the row decoder, a row block information signal indicating that the second word-line in the second row block has been activated;

receiving, by a column decoder, the row block information signal; and

repairing, by the column decoder, a first bit-line coupled to the at least one defective cell with one of a first spare bit-line in a first segment of a plurality of segments and a second spare bit-line in a second segment of the plurality of segments in response to a column address and the row block information signal,

wherein the row block information signal indicates that the first row block includes the at least one defective cell.

20. The method of claim 19,

wherein the first row block is associated with the first segment of the plurality of segments, the second row block is associated with the second segment of the plurality of segments different from the first segment, and the plurality of memory blocks are divided into the plurality of segments in a second direction crossing the first direction,

wherein each of the plurality of segments includes a plurality of bit-lines and at least one spare bit-line,

wherein the row address is received with an active command, and

wherein the column address is received with a write command or a read command.