

VERTICAL RETRACE WITH ZOOM AND CENTERED FAST
RETRACE

The invention concerns a video display deflection apparatus.

5 If an aspect ratio other than 4 x 3 is used for video production, an aspect ratio conversion may be performed to enable display of the program on a 4 x 3 consumer television receiver. For example, a wide aspect ratio program may be formatted for display on a 4 x 3 television receiver by adding
10 blank top and/or bottom strips, forming a so-called letterbox display, with a 16 x 9 active area in the 4 x 3 display area.

A wide screen television receiver is described, for example, in published International Application No. PCT/US91/03822 entitled WIDESCREEN TELEVISION -
15 Rodriguez-Cavazos, et al. The display screen has a format display ratio of e.g. 16 x 9, and a variety of alternative picture displays are made possible, including zoom or image scale factor control and multiple picture display arrangements.

20 It may be desirable to display the image content of a baseband video signal conforming to, for example, the NTSC standard that uses an aspect ratio of 4 x 3, on a display such as a 16 x 9 wide screen television receiver. Where the picture is in letterbox display format, the raster may be
25 expanded such that the picture fills the wide screen. The horizontal displacement spans the full screen width. The vertical displacement is expanded or zoomed by a factor of 4/3 such that the picture, without top and bottom black strips, fills the wide screen vertically.

30 Apart from controlling deflection to best fit the picture of a wide screen program on a wide screen display, it may be desirable to zoom a video program for other reasons. For example, when showing a conventional 4 x 3 picture, the user may wish to expand the picture, enlarging a certain area and
35 cropping off peripheral portions that are less interesting. Such a feature is especially advantageous in connection with a capability for vertical panning of the picture relative to the display.

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A vertical deflection circuit typically applies a ramping vertical deflection voltage signal to one input of a differential amplifier. A current sensing resistor in series with the vertical deflection coil is coupled to the other input of the amplifier and senses the deflection current. The amplifier drives the deflection coil in a closed-loop negative feedback manner. The deflection current defines a ramping vertical trace portion and a retrace which is synchronized to vertical sync pulses derived from the video signal.

Vertical zoom may be achieved by increasing the slope or rate of change of the ramping vertical trace portion of the vertical deflection current. This causes the beam to scan across the screen in a shorter time, as needed for zoom, but increases the time in which the beam is at its extremes of deflection and the deflection current is at a significant level. For example, if the deflection current ramp is made more steep from the outset of a vertical field, the electron beam reaches the bottom of the raster sooner. If the deflection current remains such as to hold at the bottom of the raster, e.g., at a small overscan position, the DC component of power supply loading is increased with zoom, due to the need to maintain the beam at the bottom of the raster until retrace.

The electron beam is blanked when not scanning actively across the display screen. One possibility to reduce current loading is to reduce the deflection current to near zero at the end of the zoomed scan, thus returning the beam to the center of the screen while awaiting the next retrace. If cathode ray tubes have significant spurious emission, the beam location may be visible on the screen during retrace if the retrace is slower than the usual time of about 600 to about 1,100 microseconds. Returning the beam to near center thus reduces the DC loading by the deflection circuits, but relies on the blanking circuits and means for minimizing electron emission during blanking, because any spurious beam current may render the beam position visible, as a horizontal line across the center of the display. In a cathode ray tube, the electron gun has a heated cathode, and it is difficult to block all spurious emission of electrons.



It may be desirable that a low average deflection current is maintained, e.g. by locating the beam for part of the vertical blanking period at one extreme of deflection and for part of the period at the other extreme. The retrace thus occurs during the blanking period rather than at the beginning or end. For a given image scale factor (e.g., a $4/3$ zoom), the retrace could be timed to advantageously occur at a central point in time within blanking. Advantageously, the retrace may be centered in the blanking period adaptively using a feedback control circuit to determine the appropriate time to begin retrace during zoom modes such that the DC component of the vertical yoke current is appropriately small, accommodating any degree of zoom. The beam is thus placed at its extremes of deflection in a manner that precisely balances the times the beam is disposed at each of the two extremes.

In accordance with an inventive arrangement, a video display apparatus includes a vertical deflection winding located on a cathode ray tube. A source of an image control signal is provided which represents an image scale factor selected from a range of values. A deflection ramp generator responsive to a synchronization signal and to the image control signal generates a ramp with a slope that varies with the selected scale factor. A deflection amplifier is responsive to the ramp for generating in the deflection winding a cyclical deflection current having a period of a vertical interval. The deflection current ranges between a first extreme and a second extreme during a trace interval that is shorter than the vertical interval by a time that varies with the selected scale factor. A retrace signal generator is operable to return the deflection current from the second extreme to the first extreme during a retrace interval that is positioned within a nontrace interval, but not generally positioned adjacent to either end point.

In accordance with a different inventive arrangement, a servo circuit is coupled in the feedback path of a retrace signal generator for positioning a retrace interval within a nontrace interval by means of servo feedback control.



FIGURES 1a, 1b and 1c illustrate an inventive embodiment of a vertical deflection circuit;

FIGURES 2a-2e illustrate idealized waveforms useful for explaining the timing functions of the arrangement of FIGURES 1a-1c;

FIGURE 3 illustrates current, voltage and timing waveforms useful for explaining the operation of the arrangement of FIGURES 1a-1c when top panning is provided;

FIGURE 4 illustrates comparable selected waveforms useful for explaining the operation of the arrangement of FIGURES 1a-1c when bottom panning is provided.

A sawtooth generator 100, shown in detail in FIGURE 1b, is controlled as to image scale factor and centering via a microprocessor controller and retrace triggering arrangement, as shown in FIGURE 1a, producing vertical deflection signals that are coupled to the vertical deflection coils via an output stage, as shown in FIGURE 1c. Corresponding symbols and numerals are used throughout the figures for corresponding signals, items or functions.

A vertical synchronizing signal SYNC of FIGURE 1a is coupled to a vertical timing generator 10. Signal SYNC is produced by a video detector 9 of a television receiver that processes a baseband television receiver signal SNTSC, for example conforming to the NTSC standard. The elapsed time between consecutive occurrences of SYNC in signal SNTSC accounts for a vertical interval equal to $262 \frac{1}{2}$ horizontal video line intervals that define a given picture image or field.

Generator 10 includes a microprocessor 10a, shown in FIGURE 1a, that generates a vertical cycle synchronizing pulse signal for triggering vertical reset. Under user control, for example via a remote controller, microprocessor 10a generates a pulse signal A, as shown in FIGURE 2a, that is delayed by a controllable amount TD relative to pulse signal SYNC as seen in FIGURE 2e. By delaying the occurrence of vertical reset relative to the SYNC pulse, microprocessor 10a controls panning of the picture on the screen. The delay may be, for example, a small fraction of the vertical interval between occurrences of SYNC for top panning, or a larger



fraction less than a full interval, for bottom panning, or anywhere in between. The amount by which pulse signal A of FIGURE 2a is delayed varies in accordance with the degree of panning that is required by the user.

5 Signal A of FIGURE 1a is coupled by a resistor R73 to the trigger input of a pulse stretcher flip-flop U07, and generates the leading edge of a vertical reset signal VRESET in the normal non-zoom mode of operation. A logical OR function with an input signal D is provided by a transistor
10 Q04, for controlling the timing of the leading edge of the vertical reset signal VRESET in the zoom mode of operation. The base of transistor Q04 is coupled to input signal D, generated according to FIGURE 1c, from a current IERROR. Current IERROR represents the difference between a
15 reference current level and an average vertical deflection current generated from a power supply powering the vertical output stage. As explained more fully below, the current error IERROR provides a ramping input voltage, represented by signal D, at the leading edge of vertical blanking pulse B
20 (see FIGURES 2b, 2d and 3e).

 When the ramping input voltage reaches the threshold of the triggering input of flip-flop U07, the leading edge of signal VRESET is generated at a signal line C. The leading edge LEVRESET of the VRESET pulse, shown in FIGURE 2c,
25 initiates vertical retrace. Vertical retrace is thus controlled to occur earlier or later as a function of the difference between the deflection current produced by the power supply and a reference level. The circuit minimizes the DC current loading of the half supply arrangement by equalizing the time during
30 which the vertical deflection current is at its extremes following the vertical trace, and responds adaptively to variations in the amount of time between the end of the current vertical trace ramp and the beginning of the next
35 cycle trace ramp, that results from variations in the amount of zoom and the corresponding variations in the slope of the vertical trace ramp.

 Immediately after the trailing edge TEVRESET of signal VRESET, a transistor U01A of FIGURE 1b becomes



nonconductive. A DC current IURAMP through the collector of a transistor U06A of a voltage-to-current (V/I) converter 21, then charges a capacitor C03 to produce a voltage ramp that defines the trace portion TRACE of the vertical deflection signal VSAW, shown in FIGURE 1b. The slope of ramp TRACE of deflection signal VSAW is determined by the magnitude of controllable collector current IURAMP of transistor U06A.

V/I converter 21 is controlled by an analog voltage ZOOM which services as an image scale factor control signal. Voltage ZOOM is generated by a digital-to-analog (D/A) converter 10a1 coupled to the microprocessor 10a as shown in FIGURE 1a. Voltage ZOOM represents the degree of zoom required by the user, and is arranged in the circuit to vary the rate of change of a vertical deflection current i_y applied to a vertical deflection coil L_y as shown in FIGURE 1c.

Voltage ZOOM of FIGURE 1b is coupled via a resistor R49 of FIGURE 1b to the emitter of a current control transistor Q07. An adjustable voltage V-SIZE, that may be adjusted manually using a potentiometer (not shown), is coupled via a resistor R22 to the emitter of transistor Q07 for picture height service adjustment purposes. In addition, a DC supply voltage of +12V is coupled to the emitter of transistor Q07 via a resistor R21. The base of transistor Q07 is coupled to a diode CR02 that develops a temperature compensating base voltage equal to the forward biased voltage of diode CR02. The voltages that are coupled via resistors R21, R22 and R49 produce a collector current in transistor Q07 that controls the voltage at the base of current source transistor U06A. The base voltage of transistor U06A, determined by the collector current of transistor Q07, is developed in a series arrangement of a temperature compensating transistor U06C, whose base and collector are coupled to function as a diode, and a resistor R14 that is coupled to a -9V supply.

A resistor R16 is coupled between the emitter of transistor U06A and the -9V supply voltage. A transistor U06B has a base voltage that is equal to the base voltage of transistor U06A. A potentiometer resistor R43 is coupled between the emitter of transistor U06B and the -9V voltage



supply. A resistor R18 is coupled between the emitter of transistor U06A and an adjustable moveable contact TAP of resistor R43.

5 When contact TAP is moved close to the junction of the emitter of transistor U06B and resistor R43, resistor R18 has no effect on the emitter current in transistor U06A because the emitter voltage of transistor U06B is equal to that of transistor U06A. On the other hand, when contact TAP is
10 adjusted closer to the -9V supply, resistor R18 is coupled more in parallel with resistor R16. Potentiometer resistor R43 thereby adjusts the current gain of V/I converter 21 to enable compensation for tolerances of capacitor C03, producing the sawtooth voltage as current is drawn by transistor U06A.

15 Voltage VSAW from capacitor C03 is coupled to the base of a transistor U01B. Transistor U01B is coupled with a transistor U01C to form a differential pair. The base of transistor U01C is coupled to one terminal of a resistor R09, having an opposite terminal at ground potential. A transistor
20 U02A draws a current I_0 , setting the voltage at the base of transistor U01C through resistor R09. The base voltage of transistor U01C tracks variation of height adjustment voltage V-SIZE so as to maintain vertical centering. Current I_0 provides a zero current reference, setting voltage VSAW to a
25 level that produces a correctly timed zero point to the vertical deflection current, as explained later on.

To develop current I_0 through transistor U02A in FIGURE 1b, a second V/I converter 21A, similar to V/I convertor 21, is utilized. A transistor Q09 produces a
30 collector current that tracks the collector current in transistor Q07, when an adjustment in height adjustment voltage V-SIZE is made. Voltage V-SIZE is coupled to the emitters of transistors Q07 and Q09 via resistors R22 and R56, respectively. The bases of transistors Q09 and Q07 are
35 coupled at the cathode of diode CR02 and are at equal voltage. Transistor U02B and resistor R06 form a temperature compensated main load with respect to the collector current of transistor Q09. A similar load with

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respect to the collector current of transistor Q07 is formed by the network of transistor U06C and resistor R14. Transistor U02A of V/I converter 21A produces current I0.

Advantageously, current I0 tracks variations in current IURAMP of transistor U06A in a way to maintain vertical centering unaffected when a change in height adjustment voltage V-SIZE occurs. The tracking occurs because of circuit symmetry, for example, the symmetry with respect to transistors U06A and U02A. A transistor U02C produces the emitter currents of transistors U01C and U01B. An emitter resistor R17 establishes the value of a base voltage-to-collector current ratio in transistor U02A. A resistor R49A couples a voltage CENTER, generated in a D/A converter 10a2 of FIGURE 1a, to the emitter of transistor Q09. Voltage CENTER is controlled in a manner to produce approximately equal collector currents in transistors Q09 and Q07 when the zoom mode is not selected. Voltage CENTER compensates for a non-zero offset value of voltage ZOOM when the zoom mode is not selected.

The base voltage of transistor U01C of FIGURE 1b is controlled by current I0. The values of resistor R09 and current I0 are selected such that the base voltage of transistor U01C is equal to the level of voltage VSAW at the base of transistor U01B at the time of the midpoint of the image interval, when the regular (non-zoom) mode is selected. Advantageously, as a result of tracking between V/I converters 21 and 21A, any change in size adjustment voltage V-SIZE and in the 12V supply voltage does not affect a ratio between currents I0 and IURAMP. The resulting variations in currents I0 and IURAMP maintain the base voltage of transistor U01C at the level of sawtooth voltage VSAW that corresponds to vertical center for each level of voltage V-SIZE and of the 12V supply voltage, until saturation occurs. Therefore, vertical centering is, advantageously, unaffected by adjustment of voltage V-SIZE that is used for adjusting picture height. The emitters of transistors U01B and U01C are coupled via emitter resistors R07 and R08, respectively, to the collector of transistor U02C



that controls the sum of the emitter currents. The base voltage of transistor U02C is the same as that of transistor U02A. The emitter voltage of transistor U02C, that is approximately equal to that of transistor U02B, produces an emitter current in transistor U02C that is determined by a resistor R05.

During vertical trace in the zoom mode, such as during interval t_0 - t_1 in FIGURE 3b, transistors U01B and U01C form a differential amplifier. The collector currents of transistors U01B and U01C develop, in corresponding collector resistors, voltages that are coupled via emitter follower transistors 71 and 70 to develop sawtooth signals VRAMP2 and VRAMP1, respectively.

FIGURES 3a-3f illustrate waveforms useful for explaining the operation of the arrangement of FIGURES 1a-1c. Blanking signal B, vertical reset signal VRESET and retrace timing signal D are shown again in FIGURE 3e for comparison with the current and voltage waveforms of FIGURES 2a-2d and the functional timing diagram of FIGURE 3f, and in connection with the amount of zoom shown in FIGURES 3a-3d.

Signals VRAMP1 and VRAMP2 of FIGURES 3b and 3c, respectively, are complementary signals that change in opposite directions during the vertical trace interval t_0 - t_1 . The waveforms of FIGURES 3b and 3c that are drawn in solid line occur in the zoom mode of operation, for comparison with the waveforms in dashed line, occurring in the regular or non-zoom mode of operation. An even greater degree of zoom is shown in dash-dot line. Vertical trace occurs between, for example, time t_0 and t_1 when the zoom mode is selected, and between time t_0 and time t_2 when the zoom mode is not selected, as shown in the waveforms of FIGURES 3a-3d.

A DC coupled deflection circuit 11 of FIGURE 1c, is controlled by signals VRAMP1 and VRAMP2. In circuit 11, a deflection winding L_y provides vertical deflection in a cathode ray tube, CRT 22, for example of the type W86EDV093X710, having an aspect ratio of 16 x 9.



Winding Ly is coupled in series with a deflection current sampling resistor R80. Winding Ly and resistor R80 of FIGURE 1c form a series arrangement that is coupled between an output terminal 11b of an amplifier 11a and a junction terminal 11c of a power supply decoupling capacitor Cb. A resistor R70 couples a supply voltage V+, for example +26 volts, to terminal 11c via an emitter follower transistor Q46. Transistor Q46 produces a DC voltage $+V/2$ at terminal 11c that is equal to about one half of voltage V+, in particular about +12.4 volts. The half supply voltage is determined by coupling the base of transistor Q46 to the junction of voltage dividing resistors R91 and R92. A junction terminal 11d, coupled between winding Ly and resistor R80, is coupled via a feedback resistor R60 to an inverting input terminal of amplifier 11a. Terminal 11c of resistor R80 is coupled via a resistor R30 to a noninverting input terminal of amplifier 11a. A negative feedback voltage is developed across resistor R80, representing the current in deflection coil Ly, and is applied to the input terminals of amplifier 11a. Amplifier 11a develops an output voltage as needed to cause the deflection coil current to track the voltage drive signal applied to the amplifier, as derived from sawtooth voltage signal VSAW by way of complementary voltages VRAMP1 and VRAMP2.

Complementary sawtooth signals VRAMP1 and VRAMP2 are coupled via resistors R40 and R50, to the noninverting and inverting input terminals, respectively, of amplifier 11a for controlling deflection current i_y . Differences between signals VRAMP1 and VRAMP2 due to component mismatch or offset voltage tolerances, for example, are compensated by a potentiometer 88 that is coupled between the collectors of transistors U01B and U01C. The vertical trace portion of deflection current i_y begins at time t_0 , shown in FIGURES 3e and 3f, when signals VRAMP1 and VRAMP2 begin to ramp from one extreme toward the other.

When top panning is utilized, signal VRESET of FIGURE 2c, is produced from or synchronized to the vertical



synchronization pulse signal SYNC, shown in FIGURE 2e.

Signal SYNC is associated with the picture information that follows signal SYNC in signal SNTSC, and occurs immediately prior to an image interval IMAGE of signal SNTSC. Image interval IMAGE of FIGURE 2e contains the picture information that is to be presently displayed on CRT 22 of FIGURE 1c. The vertical trace portion of deflection current i_y begins after the same delay time relative to the vertical sync pulse (which can be changeable when varying the extent of vertical panning), in each successive field or image interval. As a result, deflection current i_y of FIGURE 1c is properly synchronized in each period. Therefore, advantageously, field-to-field variations of sync signal SYNC will not cause vertical position jitter of the displayed picture.

FIGURE 3a illustrates in solid line the deflection current i_y waveform when a first exemplary amount of zoom is selected, and in dash-dot line the deflection current for a higher degree of zoom. The non-zoom regular mode is shown by a dashed line wherein the trace portion of the deflection current occupies most (15.7 mS) of the 16.7mS interval between successive occurrences of SYNC. FIGURES 3b-3d illustrate respective voltages using the same line conventions, and FIGURE 3e is specific to the amount of zoom shown in solid line in FIGURES 3a-3d. FIGURE 3f illustrates schematically an example of the timing diagram of signal SNTSC of FIGURE 1a, for the first exemplary amount of zoom. Interval 301 of interval IMAGE in FIGURE 3f would contain the picture information for the top half of the picture displayed in a non-zoom mode of operation. An interval 300 contains the picture information of the bottom portion of such picture; however, interval 300 is not used because the picture is zoomed such that interval 301 is used for the whole vertical display area. During interval 300, the video is blanked.

Signal SYNC, occurring at the time shown in FIGURE 3f, controls the beginning time of vertical trace in this top-panning mode. Vertical trace therefore begins, in each vertical field, at time t_0 . A top panning mode of operation is



obtained when a bottom portion of the displayed picture is cropped by a greater amount than a top portion. Thus, the example of FIGURES 3a-3f depicts maximum top panning. This is so because a video line TOP that is the first video line of interval 301 of FIGURE 3f capable of providing picture information in the non-zoom mode of operation is also the first video line to provide the picture information in the maximum top panning mode. As discussed below, it is also possible to use a bottom panning or a centered arrangement. However, top panning is discussed first for purposes of simplicity.

In regular, non-zoom operation, the beginning time t_0 of a trace portion of current i_y of FIGURE 3a, shown in dashed line, may be delayed slightly less in order to keep the same video picture element at the top of the screen. The difference in delay compensates for the difference that occurs in the beginning of vertical trace, between the rate of change of current i_y of FIGURE 3a in the zoom mode of operation and that in the regular, non-zoom mode of operation.

The example of FIGURES 4a and 4b illustrates a comparable case wherein the last video line BOTTOM of interval 300 of image interval IMAGE is arranged to occupy the bottom of the display screen, i.e., at maximum bottom panning. Similar symbols and numerals in FIGURES 4a, 4b, 3a-3f, 2a-2e and 1a-1c are used for similar items or functions. The delay between SYNC and the commencement of the trace ramp in current i_y of FIGURE 4a with respect to signal SNTSC of FIGURE 4b is significantly longer than the delay according to FIGURE 3a, as needed to expand or zoom the bottom portion of the picture rather than the top. It will be appreciated that by choice of an appropriate delay, which can be by horizontal line counting or the like, a top pan or bottom pan, or any position in between may be selected.

It is advantageous for purposes of circuit simplicity to utilize a deflection circuit 11 as in FIGURE 1c, relying on a positive supply voltage $V+$ and not requiring a negative supply voltage for generating an alternating deflection current i_y . A half supply voltage $+V/2$ is derived from the



full supply voltage $V+$, e.g., 26 volts, for driving the deflection circuit. Current limiting resistor R70 is coupled to voltage $V+$ for generating, via transistor Q46, the half supply voltage at terminal 11c.

5 It is desirable to reduce the average or DC current through current limiting resistor R70 so that a large resistance can be used. The large value of resistor R70 is desirable to provide for current limitation so that excessive deflection current i_y may be prevented if a fault condition
10 occurs. Such fault condition may occur, for example, if output terminal 11b of amplifier 11a is shorted to ground. It may also be desirable to prevent excessive deflection current i_y in order to avoid damage to the neck of CRT 22 by a beam current strike.

15 In accordance with an inventive feature, the average value of the deflection current i_y is reduced or limited, in the zoom mode of operation. Referring to FIGURE 3a, this is accomplished by adjusting the timing of the leading edge of VRESET so that retrace commences at or near the midpoint of
20 the interval between time t_1 , when trace is completed, and time t_2 , immediately prior to the beginning of the next vertical trace. Thus, the vertical retrace interval t_a - t_b is positioned within the nontrace interval t_1 - t_2 , but is not generally adjacent to either end point t_1 or t_2 . By balancing
25 the time at which the deflection current is at its opposite extremes, the average value of the deflection current is minimized.

 As shown in FIGURE 1c, the collector of half supply transistor Q46 is coupled to the positive supply $V+$ through
30 resistor R70, and the base of transistor Q46 is coupled to a voltage divider having equal value resistors, R91 and R92, thus setting the base voltage of transistor Q46 at half the level of $V+$. The emitter of transistor Q46 is thereby regulated to half the voltage at $V+$, less the forward biased
35 base-emitter voltage of transistor Q46. The current I_s supplied by the half supply, flowing through resistor R70, produces a voltage signal at the collector of transistor Q46 representing the level of current I_s . This voltage signal is



filtered by the network including capacitor C71 and resistors R71 and R73, and applied to the base of an error amplifier transistor Q73. The network of capacitor C71 and resistors R71 and R73 form an integrator applying to error amplifier Q73 a voltage that varies with the average current supplied through half supply transistor Q46. The output of the error amplifier transistor Q73 is a current proportional to the amount by which the half supply current exceeds a reference level of about 13 mA according to the circuit values of the embodiment shown. The half supply emitter resistor R79 sinks about 21 mA. Feedback via diode CR71 causes the circuit to regulate near 21 mA, keeping supply transistor Q46 in conduction during at least a portion of the vertical interval.

Referring to FIGURE 1a, the current output IERROR of error amplifier transistor Q73 is coupled to a timing capacitor C17. The timing capacitor is disabled by a timer switch Q02 and an inverter Q01, except when signal B is high. Signal B is the vertical blanking signal generated by microprocessor 10a, and is at the high blanking level except during vertical trace. It is used by blanking circuitry, not shown, to blank the screen of CRT 22. In the zoom mode, the leading edge of blanking occurs earlier than the vertical timing signal A, generated by the microprocessor to initiate a new vertical trace in the non-zoom mode.

Current signal IERROR from error amplifier Q73 in FIGURE 1c is coupled to capacitor C17, charging the capacitor to produce a voltage signal D as shown in FIGURE 2d (see also FIGURE 3e), that ramps upwardly at a rate proportional to IERROR. This timing signal D is coupled to the base of transistor Q04, which forms a buffer between capacitor C17 and the threshold input of flip-flop IC U07. The threshold input of IC U07 is one input to a comparator U7a, the other input being coupled internally to a voltage divider setting a threshold of about 3.4 volts. When the buffered ramp exceeds the threshold level, the set input of the flip-flop FF in IC U07 triggers, causing the Q output of flip-flop FF to go high and the low-true output at pin 3 to go low. This low-true output is coupled to the base of a transistor

Q10, which clamps the VRESET signal C high, initiating a fast vertical retrace by clamping voltage signal VSAW via transistors U01A and U01B in FIGURE 1b. Simultaneously, the output of the flip-flop in IC U07 turns on a transistor Q11 to discharge timing capacitor C17.

The amount of current IERROR produced by the error amplifier of Q73 in FIGURE 1c is determined by the emitter voltage set by the voltage divider of resistors R75 and R77, and by the voltage signal at the base of transistor Q73, coupled from the collector of the half supply regulator transistor Q46 by resistor R71. The gain of the current amplifier is set in conjunction with the value of timing capacitor C17 (FIGURE 1a) and the threshold defined by the internal voltage divider in IC U07 such that the threshold is reached and retrace is initiated at a time causing the deflection current during retrace to cross zero current near the midpoint of the blanking interval, as shown in FIGURE 3a. As a result, the DC component of the deflection current is appropriately small, and can be zero or a small absolute value.

The timer IC U07 remains in a state clamping VRESET high, until the vertical blanking signal B from microprocessor 10a drops below the trigger input voltage of IC U07. The trigger input of IC U07 is also arranged to be coupled to a comparator U7b which triggers at about 1.7 volts. When this occurs, signalling the beginning of a new vertical trace, output pin 3 of IC U07 again goes high, releasing the clamping of VRESET and allowing VSAW to begin a new trace ramp. Simultaneously, IC U07 releases discharge pin 7, enabling timer capacitor C17 for timing during the next vertical blanking pulse B.

Vertical timing signal A from microprocessor 10a is OR'ed with timing ramp signal D via resistor R73, coupled to the threshold input of IC U07 and the emitter of buffer transistor Q04. In the normal (non-zoom) mode of operation, timing ramp signal D may not reach the threshold level at the input of IC U07 before the leading edge of vertical timing signal A. In that mode, the leading edge of timing signal A



sets the flip-flop in IC U07 and initiates clamping of VRESET and retrace of VSAW synchronously with the leading edge of timing signal A.

5 The circuit as thus described causes the leading edge of VRESET in the zoom mode, and the initiation of vertical retrace by clamping signal VSAW, to occur after the beginning of blanking (i.e., after the change of state of signal B), by an amount determined by the ramping voltage on signal D. The circuit responds adaptively to changes in the
10 amount of zoom, to minimize the DC current loading of the half supply. As discussed above, the error amplifier of transistor Q73 produces a current representing the amount by which the half supply current varies from a reference level.

15 Assume the amount of zoom and the slope of the trace ramp are increased suddenly, for example from the amount shown in solid line in FIGURE 3a to the amount shown in dash-dot line, so that the deflection current reaches its negative maximum sooner. Before further servo adjustment
20 is initiated, the longer dwell time, for example at the negative maximum, for a greater proportion of the vertical interval, produces a DC deflection current offset and a change in DC current loading of the half supply. This results in the current output of error amplifier Q73 being likewise changed as a
25 function of the difference in supplied current from the reference level. A larger current IERROR then causes a faster rising ramp in signal D, making VRESET occur earlier in the vertical blanking period defined by signal B.

30 In this manner, if the amount of zoom is increased and the deflection current reaches its negative peak sooner, the delay between the blanking signal and the vertical reset is increased and the retrace is advanced in a feedback servo manner. Similarly, if the amount of zoom is decreased, such that the negative peak occurs later, retrace is retarded
35 to a later point in the vertical blanking period. As illustrated by the dashed line waveform of FIGURE 3a, at the latest, retrace occurs between times t_2' - t_2 , with the vertical synchronizing signal A, defining the normal, non-zoom mode.



For any amount of zoom, the timing of retrace is adjusted automatically to occur at or near the midpoint of retrace, by the advantageous feedback control circuit, wherein DC current loading of the half supply is sensed and controlled by adjusting the timing of the leading edge of VRESET.

Signal VSAW as shown in FIGURE 3d continues to ramp downwardly during the beginning of the blanking interval; however, VRAMP1 and VRAMP2 level out at the saturation voltages of the differential amplifier arrangement of FIGURE 1b, e.g., at about 2.3 and 4.3 volts, respectively. At the leading edge of VRESET, signal VSAW is clamped high by transistor U01A, causing VRAMP1 and VRAMP2 to switch to their opposite states. Deflection amplifier 11a in FIGURE 1c then ceases operating in a linear feedback mode and a voltage VB at supply terminal 6 of amplifier 11a is applied to deflection winding Ly via output terminal 11b. A retrace voltage V11b is produced immediately after time ta in FIGURE 3a, to enable deflection current iy to complete retrace by time tb. Switch 11f1 in FIGURE 1c of a boost stage 11f causes a capacitor 11g to be coupled in series with a boost capacitor 11e. Capacitor 11e is charged via a diode X and a switch 11f2 from the +26V supply voltage V+, during vertical trace. A supply voltage, developed across filter capacitor 11g, is summed up with a voltage developed across boost capacitor 11e so as to form boost voltage VB. Voltage VB is decoupled from the +26V supply voltage V+ via a diode DR, when boost voltage VB is formed. During the short interval ta-tb in FIGURES 3a and 3e, retrace portion RETRACE of current iy is produced. Electromagnetic energy stored in deflection winding Ly of FIGURE 1c due to current iy is used in the boost circuit, shown schematically as switch 11f1, to generate the vertical retrace voltage V11b at terminal 11b of FIGURE 1c that is larger than voltage V+, causing a fast retrace.

Near time tb, deflection current iy has increased in value to a point which permits linear operation of amplifier 11a. Feedback from resistor R80 enables the deflection current to follow the flat top portions of VRAMP1 and



VRAMP2 between times t_b and t_2 . At the end of vertical retrace, at time t_2 deflection amplifier 11a of FIGURE 1c, operating in its linear feedback mode, again produces the sawtooth trace portion of deflection current i_y .

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WHAT IS CLAIMED IS:

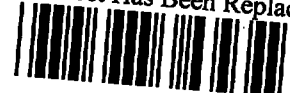
1. A video display apparatus, comprising:
a cathode ray tube (22);
a vertical deflection winding (L_y) on said cathode ray tube;
a source (10a1) of an image control signal (ZOOM) representing an image scale factor selected from a range of values;
a source (9) of a vertical synchronization signal (SYNC);
a deflection ramp generator (100) responsive to said synchronization and image control signals for generating a ramp (VSAW) with a slope that varies with the selected scale factor; characterized by
a deflection amplifier (11a) responsive to said ramp for generating in said deflection winding a cyclical deflection current (i_y) having a period of a vertical interval, the deflection current ranging between a first extreme (+IP) and a second extreme (-IP) during a trace interval (t_0-t_1) that is shorter than the vertical interval (t_0-t_2) by a time (t_1-t_2) that varies with the selected scale factor; and
a retrace signal (VRESET) generator (10a, Q73, C17, U07) operable to return the deflection current from the second extreme to the first extreme during a retrace interval (t_a-t_b) that is positioned within a nontrace interval (t_1-t_2), but not generally positioned adjacent to either end point of the trace interval.

2. The video display apparatus according to Claim 1, characterized in that a timing means (10a, Q73, C17) of the retrace signal generator is operable to generate said retrace interval substantially centered about a midpoint of the time by which the trace interval (t_0-t_1) is shorter than the vertical interval (t_0-t_2).

3. The video display apparatus according to Claim 1, characterized in that the ramp generator, the deflection amplifier and the deflection winding form a DC-coupled vertical deflection circuit (11), and the retrace signal



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generator reduces a DC average current (I_s) in said deflection winding.

4. The video display apparatus according to Claim 3, characterized in that the retrace signal generator is coupled in a feedback loop to the vertical deflection circuit to advance or retard the retrace interval to minimize the DC average current.

5. The video display apparatus according to Claim 4, characterized in that the retrace signal generator includes a current error amplifier (Q73) coupled to the vertical deflection circuit and operable to produce an error current signal as a function of a difference between the DC average current and a reference level, the error current signal being coupled to charge a capacitor (C17), and further comprising a threshold detector (U7a) operable to trigger the initiation of the retrace interval when a timing ramp signal (D) on the capacitor reaches a threshold.

6. The video display apparatus according to Claim 4, further characterized by a power supply (V_+ , Q46) for generating a first supply voltage (V_+) and a second supply ($+V/2$) voltage having the same polarity as said first supply voltage, the first and second supply voltages being coupled to opposite ends of the deflection winding.

7. The video display apparatus according to Claim 6, further characterized by a current limiting resistor (R80) coupled to the deflection circuit, a lower ($+V/2$) voltage one of the first and second supply voltages being coupled to a terminal (11c) of said resistor remote from said deflection amplifier.

8. The video display apparatus according to Claim 4, further characterized by a current limiting resistor (R80) coupled to the deflection circuit, and wherein the retrace

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* C L M S *

signal generator is operable to minimize a DC current flowing in the current limiting resistor.

9. The video display apparatus according to Claim 4 further characterized by a power supply (V+, Q46) for generating a first supply voltage (V+) and a second supply voltage (+V/2) having the same polarity as said first supply voltage, the first and second supply voltages being coupled to opposite ends of the deflection winding.

10. The video display apparatus according to Claim 1, characterized in that said retrace signal VRESET is time shifted relative to the vertical synchronization signal for panning to a zoomed portion of a picture being displayed.

11. The video display apparatus according to Claim 1, characterized in that said retrace signal generator centers said retrace interval within said nontrace interval.

12. The video display apparatus according to Claim 1, characterized in that said deflection amplifier maintains said deflection current near said second extreme from the end of said trace interval to the beginning of said retrace interval and maintains said deflection current near said first extreme from the end of said retrace interval to the beginning of the next subsequent trace interval.

13. The video display apparatus according to Claim 12, characterized in that said retrace signal generator centers said retrace interval within said nontrace interval.

14. A video display apparatus, comprising:
a cathode ray tube (22);
a vertical deflection winding (L_y) on said cathode ray tube;
a source (9) of a vertical synchronization signal (SYNC);



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a deflection ramp generator (100) responsive to said synchronization signal for generating a synchronized ramp (VSAW); characterized by

a deflection amplifier (11a) responsive to said ramp for generating in said deflection winding a cyclical deflection current (I_y) having a period of a vertical interval (t_0 - t_2), the deflection current ranging between a first extreme (+IP) and a second extreme (-IP) during a trace interval (t_0 - t_1) that is shorter than the vertical interval; and

a servo circuit (10a, Q73, C17, U07) coupled to said deflection amplifier for positioning a retrace interval (t_a - t_b) within a nontrace interval (t_1 - t_2) by means of servo feedback control.

15. The video display apparatus according to Claim 14, characterized in that said servo circuit centers said retrace interval within said nontrace interval.

16. The video display apparatus according to Claim 15, characterized in that said deflection amplifier maintains said deflection current near said second extreme (-IP) from the end (t_1) of said trace interval to the beginning (t_a) of said retrace interval and maintains said deflection current near said first extreme (+IP) from the end (t_b) of said retrace interval to the beginning (t_2) of the next subsequent trace interval.

17. The video display apparatus according to Claim 14, characterized in that said servo circuit includes means (R70) for generating a signal (I_s) representative of average deflection current and means (Q73) responsive to said average deflection current representative signal for providing servo feedback control of said average deflection current.



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ABSTRACT

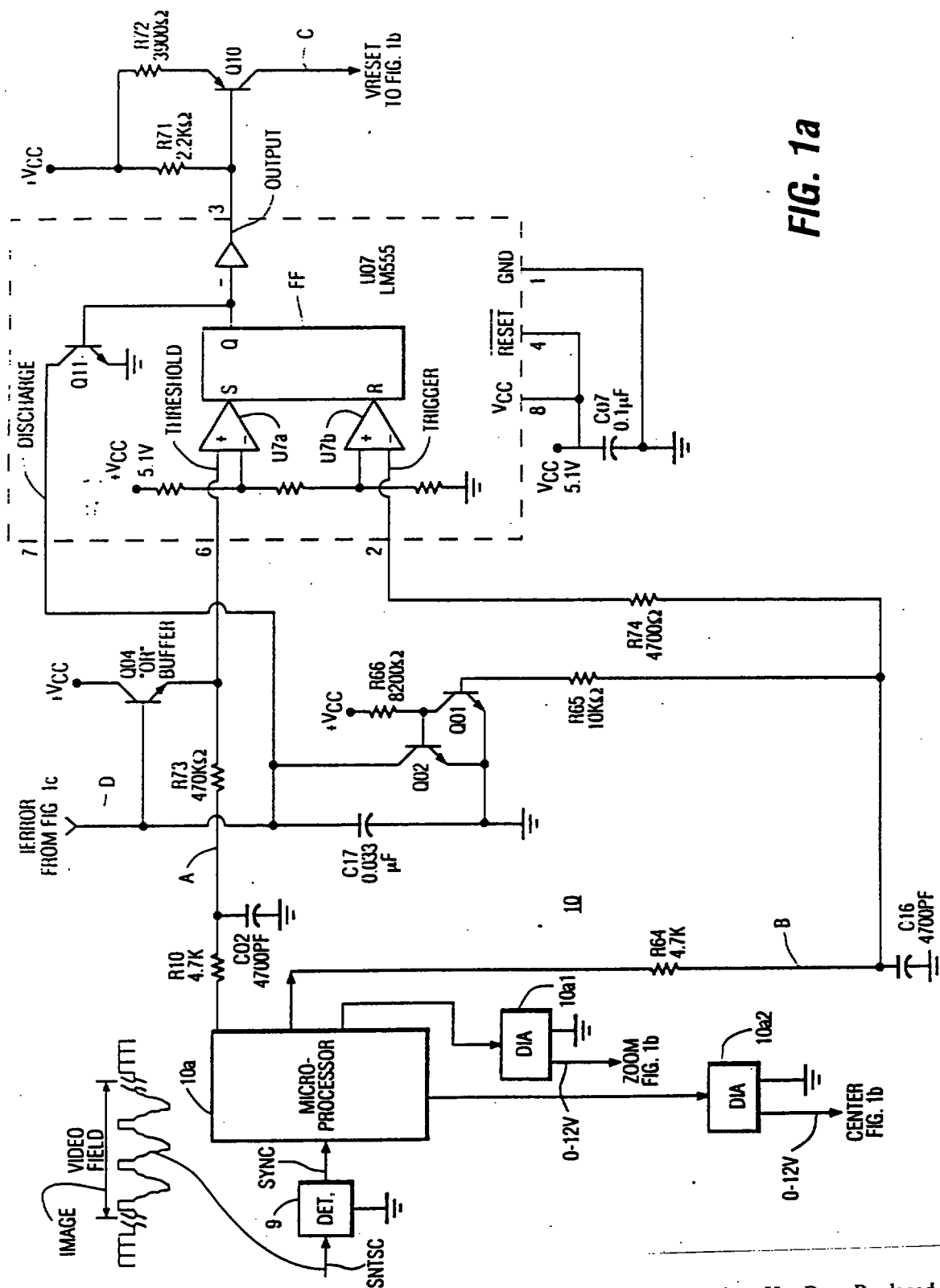
A television receiver is controlled as to the degree of vertical zoom via a deflection current ramp that varies in slope and which may be delayed to achieve panning. Due to the increased slope when zoomed, the deflection current and the electron beam complete a trace in less time than the normal vertical interval. The deflection current is maintained at one extreme or the other outside the trace interval, and the beam is blanked. A retrace signal generator (10a, C17, U07) coupled in a feedback (IERROR) loop with the power supply for the deflection circuit determines the midpoint of the blanking period and generates a fast retrace (VRESET) at or near the midpoint. The feedback loop is arranged to minimize the DC average current in the deflection winding by having a current source responsive to the DC average current for charging a timing ramp (C17) that triggers retrace upon reaching a threshold. The slope of the timing ramp varies with DC loading, thus advancing or retarding retrace to center retrace in the blanking interval.

20

FIGURE 1a

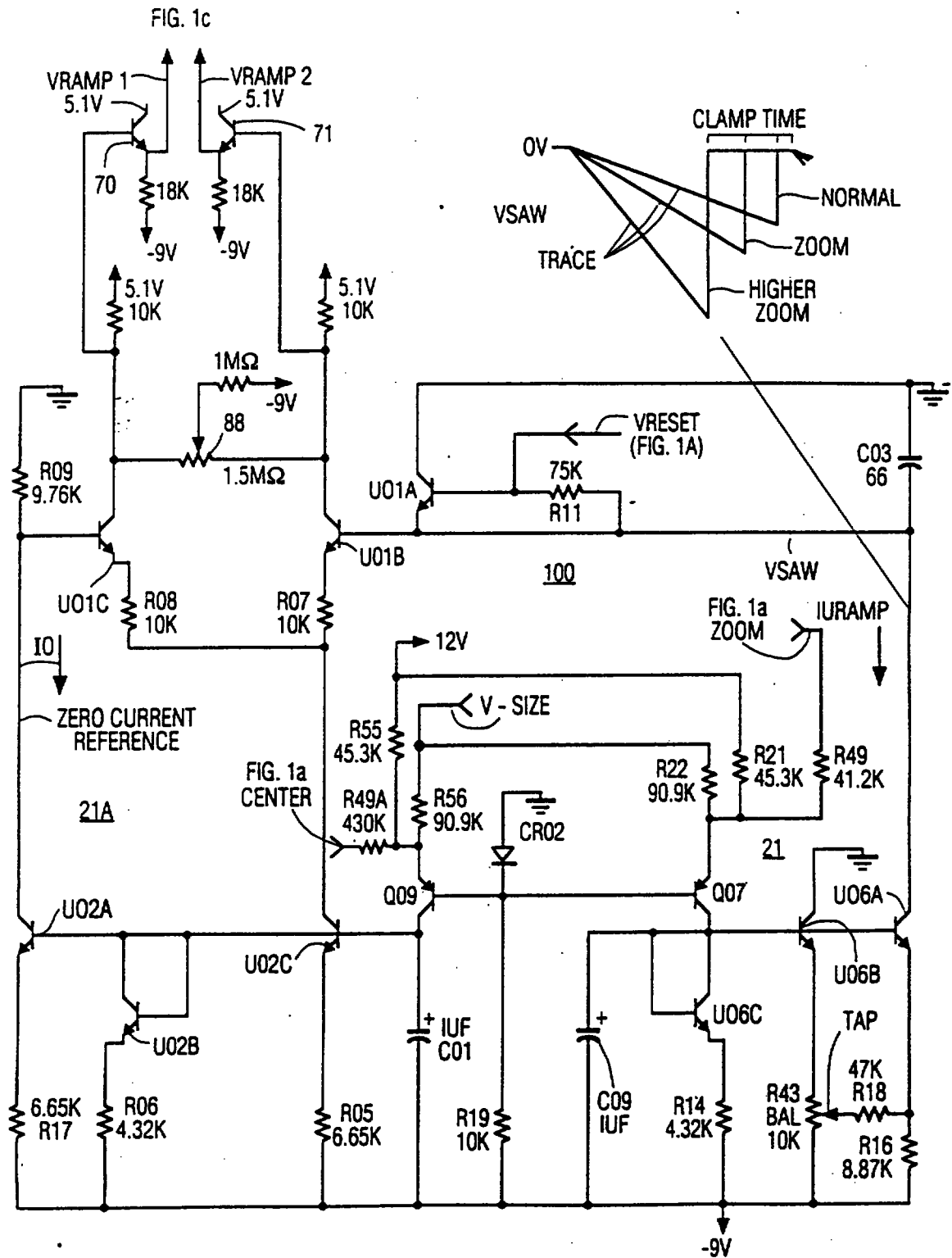
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FIG. 1b

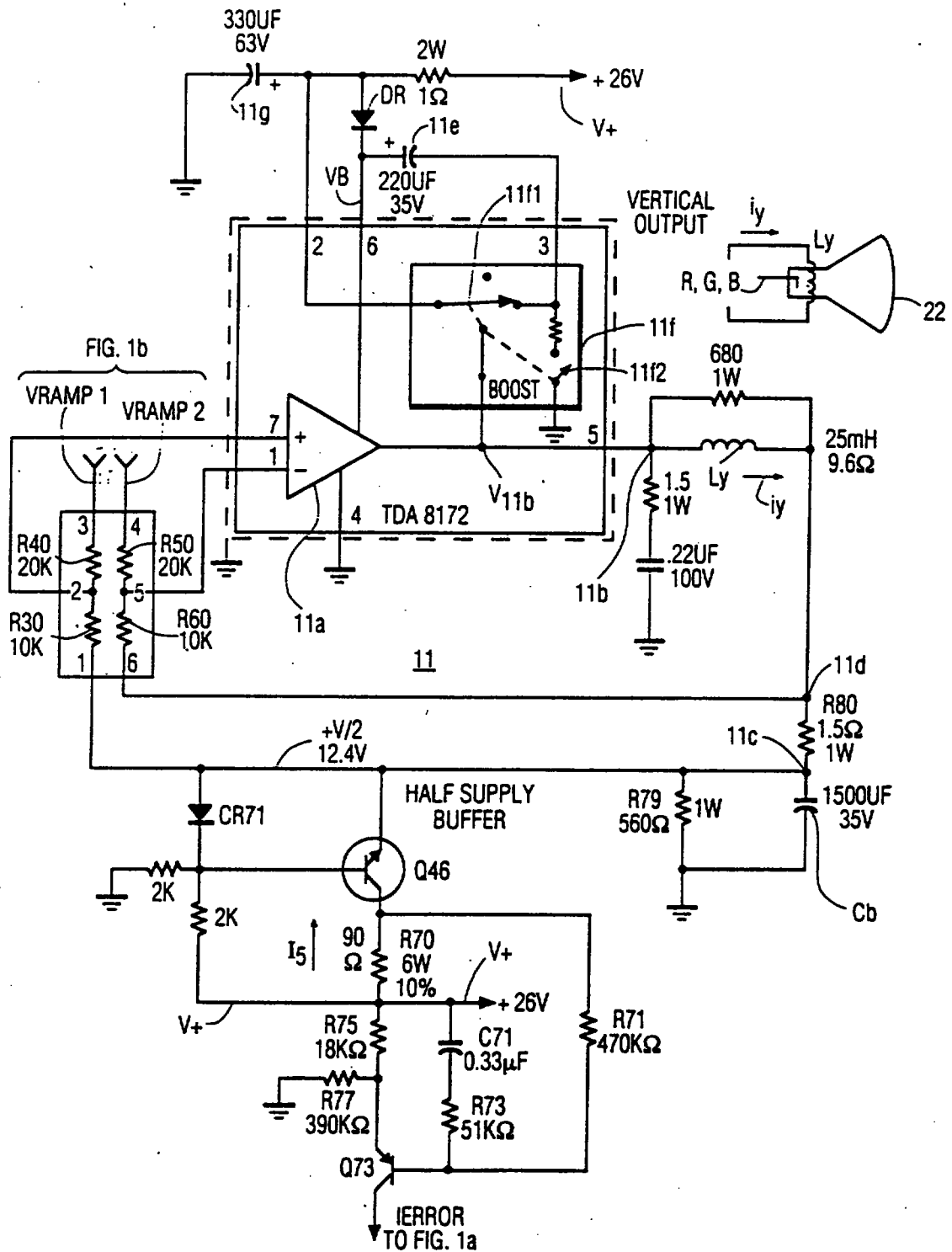
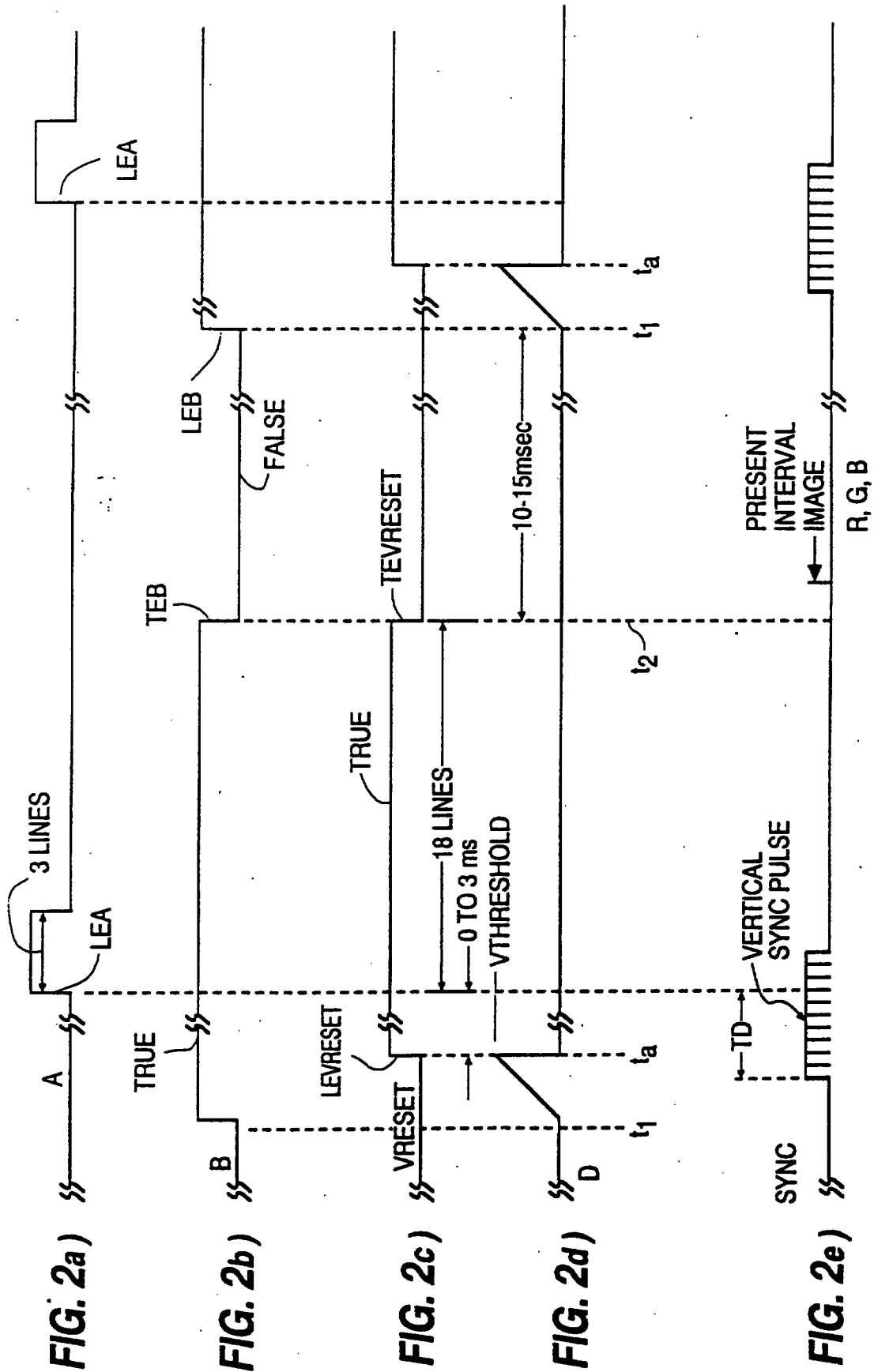
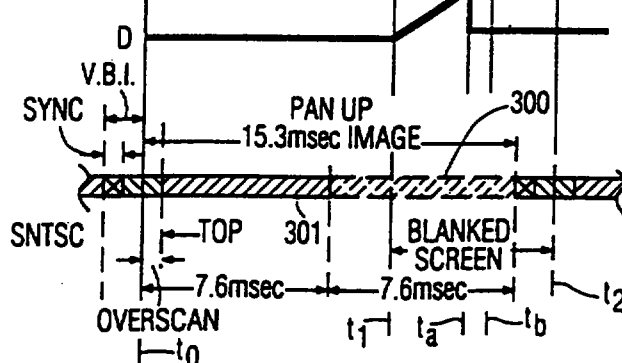


FIG. 1c

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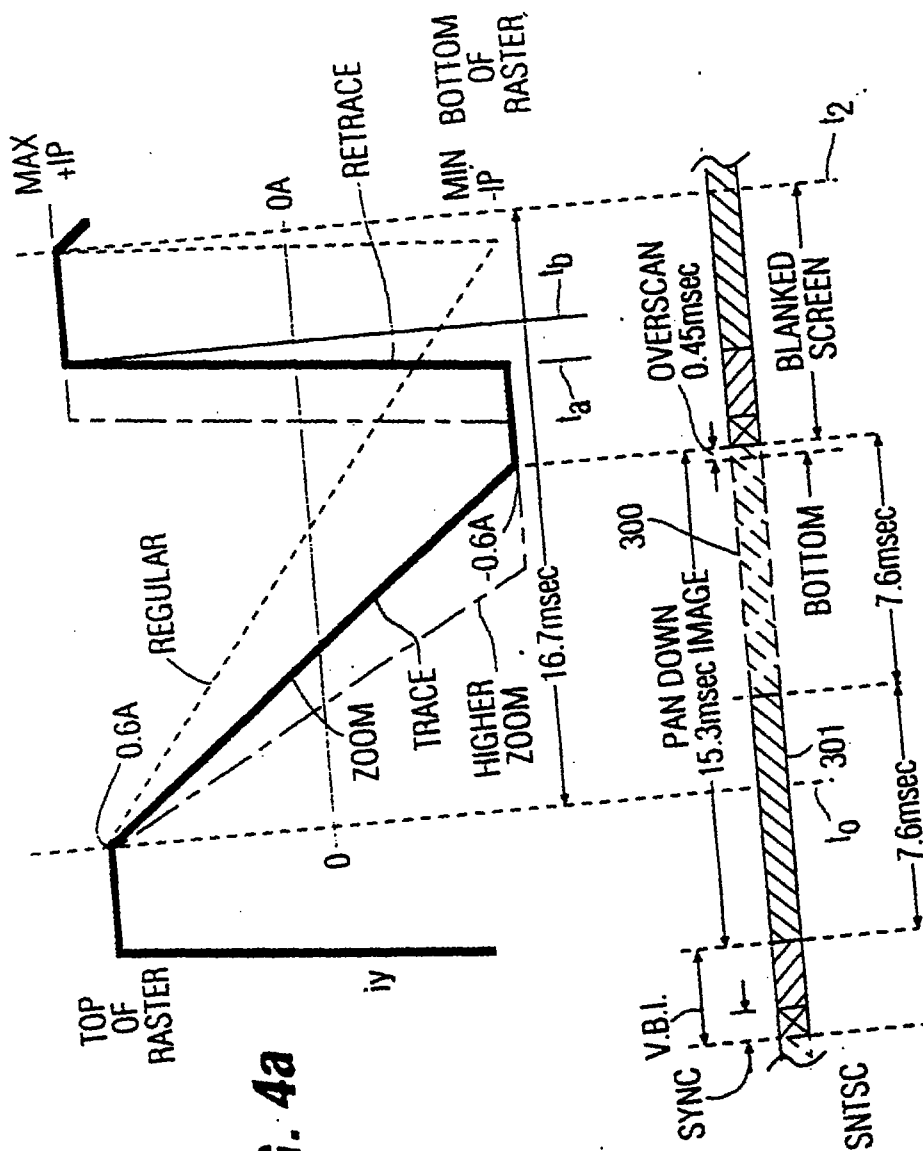
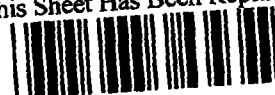


FIG. 4a

FIG. 4b

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VERTICAL RETRACE WITH ZOOM AND CENTERED FAST
RETRACE

The invention concerns a video display deflection apparatus.

5 If an aspect ratio other than 4 x 3 is used for video production, an aspect ratio conversion may be performed to enable display of the program on a 4 x 3 consumer television receiver. For example, a wide aspect ratio program may be formatted for display on a 4 x 3 television receiver by adding
10 blank top and/or bottom strips, forming a so-called letterbox display, with a 16 x 9 active area in the 4 x 3 display area.

A wide screen television receiver is described, for example, in published International Application No. PCT/US91/03822 entitled WIDESCREEN TELEVISION -
15 Rodriguez-Cavazos, et al. The display screen has a format display ratio of e.g. 16 x 9, and a variety of alternative picture displays are made possible, including zoom or image scale factor control and multiple picture display arrangements.

20 It may be desirable to display the image content of a baseband video signal conforming to, for example, the NTSC standard that uses an aspect ratio of 4 x 3, on a display such as a 16 x 9 wide screen television receiver. Where the picture is in letterbox display format, the raster may be
25 expanded such that the picture fills the wide screen. The horizontal displacement spans the full screen width. The vertical displacement is expanded or zoomed by a factor of 4/3 such that the picture, without top and bottom black strips, fills the wide screen vertically.

30 Apart from controlling deflection to best fit the picture of a wide screen program on a wide screen display, it may be desirable to zoom a video program for other reasons. For example, when showing a conventional 4 x 3 picture, the user may wish to expand the picture, enlarging a certain area and cropping off peripheral portions that are less interesting.
35 Such a feature is especially advantageous in connection with a capability for vertical panning of the picture relative to the display.

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☒ Description : paged ..1.. to paged ..17..
☒ Claim(s) : paged ..19.. to paged ..22..
☒ Drawing(s) : paged ..4.. to paged ..4..
☒ Abstract : paged ..23.. to paged

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A vertical deflection circuit typically applies a ramping vertical deflection voltage signal to one input of a differential amplifier. A current sensing resistor in series with the vertical deflection coil is coupled to the other input of the amplifier and senses the deflection current. The amplifier drives the deflection coil in a closed-loop negative feedback manner. The deflection current defines a ramping vertical trace portion and a retrace which is synchronized to vertical sync pulses derived from the video signal.

Vertical zoom may be achieved by increasing the slope or rate of change of the ramping vertical trace portion of the vertical deflection current. This causes the beam to scan across the screen in a shorter time, as needed for zoom, but increases the time in which the beam is at its extremes of deflection and the deflection current is at a significant level. For example, if the deflection current ramp is made more steep from the outset of a vertical field, the electron beam reaches the bottom of the raster sooner. If the deflection current remains such as to hold at the bottom of the raster, e.g., at a small overscan position, the DC component of power supply loading is increased with zoom, due to the need to maintain the beam at the bottom of the raster until retrace.

The electron beam is blanked when not scanning actively across the display screen. One possibility to reduce current loading is to reduce the deflection current to near zero at the end of the zoomed scan, thus returning the beam to the center of the screen while awaiting the next retrace. If cathode ray tubes have significant spurious emission, the beam location may be visible on the screen during retrace if the retrace is slower than the usual time of about 600 to about 1,100 microseconds. Returning the beam to near center thus reduces the DC loading by the deflection circuits, but relies on the blanking circuits and means for minimizing electron emission during blanking, because any spurious beam current may render the beam position visible, as a horizontal line across the center of the display. In a cathode ray tube, the electron gun has a heated cathode, and it is difficult to block all spurious emission of electrons.

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It may be desirable that a low average deflection current is maintained, e.g. by locating the beam for part of the vertical blanking period at one extreme of deflection and for part of the period at the other extreme. The retrace, thus occurs during the blanking period rather than at the beginning or end. For a given image scale factor (e.g., a $4/3$ zoom), the retrace could be timed to advantageously occur at a central point in time within blanking. Advantageously, the retrace may be centered in the blanking period adaptively using a feedback control circuit to determine the appropriate time to begin retrace during zoom modes such that the DC component of the vertical yoke current is appropriately small, accommodating any degree of zoom. The beam is thus placed at its extremes of deflection in a manner that precisely balances the times the beam is disposed at each of the two extremes.

In accordance with an inventive arrangement, a video display apparatus includes a vertical deflection winding located on a cathode ray tube. A source of an image control signal is provided which represents an image scale factor selected from a range of values. A deflection ramp generator responsive to a synchronization signal and to the image control signal generates a ramp with a slope that varies with the selected scale factor. A deflection amplifier is responsive to the ramp for generating in the deflection winding a cyclical deflection current having a period of a vertical interval. The deflection current ranges between a first extreme and a second extreme during a trace interval that is shorter than the vertical interval by a time that varies with the selected scale factor. A retrace signal generator is operable to return the deflection current from the second extreme to the first extreme during a retrace interval that is positioned within a nontrace interval, but not generally positioned adjacent to either end point.

In accordance with a different inventive arrangement, a servo circuit is coupled in the feedback path of a retrace signal generator for positioning a retrace interval within a nontrace interval by means of servo feedback control.

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FIGURES 1a, 1b and 1c illustrate an inventive embodiment of a vertical deflection circuit;

FIGURES 2a-2e illustrate idealized waveforms useful for explaining the timing functions of the arrangement of FIGURES 1a-1c;

FIGURE 3 illustrates current, voltage and timing waveforms useful for explaining the operation of the arrangement of FIGURES 1a-1c when top panning is provided;

FIGURE 4 illustrates comparable selected waveforms useful for explaining the operation of the arrangement of FIGURES 1a-1c when bottom panning is provided.

A sawtooth generator 100, shown in detail in FIGURE 1b, is controlled as to image scale factor and centering via a microprocessor controller and retrace triggering arrangement, as shown in FIGURE 1a, producing vertical deflection signals that are coupled to the vertical deflection coils via an output stage, as shown in FIGURE 1c. Corresponding symbols and numerals are used throughout the figures for corresponding signals, items or functions.

A vertical synchronizing signal SYNC of FIGURE 1a is coupled to a vertical timing generator 10. Signal SYNC is produced by a video detector 9 of a television receiver that processes a baseband television receiver signal SNTSC, for example conforming to the NTSC standard. The elapsed time between consecutive occurrences of SYNC in signal SNTSC accounts for a vertical interval equal to $262 \frac{1}{2}$ horizontal video line intervals that define a given picture image or field.

Generator 10 includes a microprocessor 10a, shown in FIGURE 1a, that generates a vertical cycle synchronizing pulse signal for triggering vertical reset. Under user control, for example via a remote controller, microprocessor 10a generates a pulse signal A, as shown in FIGURE 2a, that is delayed by a controllable amount TD relative to pulse signal SYNC as seen in FIGURE 2e. By delaying the occurrence of vertical reset relative to the SYNC pulse, microprocessor 10a controls panning of the picture on the screen. The delay may be, for example, a small fraction of the vertical interval between occurrences of SYNC for top panning, or a larger

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fraction less than a full interval, for bottom panning, or anywhere in between. The amount by which pulse signal A of FIGURE 2a is delayed varies in accordance with the degree of panning that is required by the user.

5 Signal A of FIGURE 1a is coupled by a resistor R73 to the trigger input of a pulse stretcher flip-flop U07, and generates the leading edge of a vertical reset signal VRESET in the normal non-zoom mode of operation. A logical OR
10 function with an input signal D is provided by a transistor Q04, for controlling the timing of the leading edge of the vertical reset signal VRESET in the zoom mode of operation. The base of transistor Q04 is coupled to input signal D, generated according to FIGURE 1c, from a current IERROR. Current IERROR represents the difference between a
15 reference current level and an average vertical deflection current generated from a power supply powering the vertical output stage. As explained more fully below, the current error IERROR provides a ramping input voltage, represented by signal D, at the leading edge of vertical blanking pulse B
20 (see FIGURES 2b, 2d and 3e).

 When the ramping input voltage reaches the threshold of the triggering input of flip-flop U07, the leading edge of signal VRESET is generated at a signal line C. The leading edge LEVRESET of the VRESET pulse, shown in FIGURE 2c,
25 initiates vertical retrace. Vertical retrace is thus controlled to occur earlier or later as a function of the difference between the deflection current produced by the power supply and a reference level. The circuit minimizes the DC current loading of the half supply arrangement by equalizing the time during
30 which the vertical deflection current is at its extremes following the vertical trace, and responds adaptively to variations in the amount of time between the end of the current vertical trace ramp and the beginning of the next cycle trace ramp, that results from variations in the amount
35 of zoom and the corresponding variations in the slope of the vertical trace ramp.

 Immediately after the trailing edge TEVRESET of signal VRESET, a transistor U01A of FIGURE 1b becomes

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nonconductive. A DC current IURAMP through the collector of a transistor U06A of a voltage-to-current (V/I) converter 21, then charges a capacitor C03 to produce a voltage ramp that defines the trace portion TRACE of the vertical deflection signal VSAW, shown in FIGURE 1b. The slope of ramp TRACE of deflection signal VSAW is determined by the magnitude of controllable collector current IURAMP of transistor U06A.

V/I converter 21 is controlled by an analog voltage ZOOM which services as an image scale factor control signal. Voltage ZOOM is generated by a digital-to-analog (D/A) converter 10a1 coupled to the microprocessor 10a as shown in FIGURE 1a. Voltage ZOOM represents the degree of zoom required by the user, and is arranged in the circuit to vary the rate of change of a vertical deflection current i_y applied to a vertical deflection coil L_y as shown in FIGURE 1c.

Voltage ZOOM of FIGURE 1b is coupled via a resistor R49 of FIGURE 1b to the emitter of a current control transistor Q07. An adjustable voltage V-SIZE, that may be adjusted manually using a potentiometer (not shown), is coupled via a resistor R22 to the emitter of transistor Q07 for picture height service adjustment purposes. In addition, a DC supply voltage of +12V is coupled to the emitter of transistor Q07 via a resistor R21. The base of transistor Q07 is coupled to a diode CR02 that develops a temperature compensating base voltage equal to the forward biased voltage of diode CR02. The voltages that are coupled via resistors R21, R22 and R49 produce a collector current in transistor Q07 that controls the voltage at the base of current source transistor U06A. The base voltage of transistor U06A, determined by the collector current of transistor Q07, is developed in a series arrangement of a temperature compensating transistor U06C, whose base and collector are coupled to function as a diode, and a resistor R14 that is coupled to a -9V supply.

A resistor R16 is coupled between the emitter of transistor U06A and the -9V supply voltage. A transistor U06B has a base voltage that is equal to the base voltage of transistor U06A. A potentiometer resistor R43 is coupled between the emitter of transistor U06B and the -9V voltage

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supply. A resistor R18 is coupled between the emitter of transistor U06A and an adjustable moveable contact TAP of resistor R43.

5 When contact TAP is moved close to the junction of the emitter of transistor U06B and resistor R43, resistor R18 has no effect on the emitter current in transistor U06A because the emitter voltage of transistor U06B is equal to that of transistor U06A. On the other hand, when contact TAP is adjusted closer to the -9V supply, resistor R18 is coupled
10 more in parallel with resistor R16. Potentiometer resistor R43 thereby adjusts the current gain of V/I converter 21 to enable compensation for tolerances of capacitor C03, producing the sawtooth voltage as current is drawn by transistor U06A.

15 Voltage VSAW from capacitor C03 is coupled to the base of a transistor U01B. Transistor U01B is coupled with a transistor U01C to form a differential pair. The base of transistor U01C is coupled to one terminal of a resistor R09, having an opposite terminal at ground potential. A transistor
20 U02A draws a current I0, setting the voltage at the base of transistor U01C through resistor R09. The base voltage of transistor U01C tracks variation of height adjustment voltage V-SIZE so as to maintain vertical centering. Current I0 provides a zero current reference, setting voltage VSAW to a
25 level that produces a correctly timed zero point to the vertical deflection current, as explained later on.

To develop current I0 through transistor U02A in FIGURE 1b, a second V/I converter 21A, similar to V/I
30 convertor 21, is utilized. A transistor Q09 produces a collector current that tracks the collector current in transistor Q07, when an adjustment in height adjustment voltage V-SIZE is made. Voltage V-SIZE is coupled to the emitters of transistors Q07 and Q09 via resistors R22 and R56, respectively. The bases of transistors Q09 and Q07 are
35 coupled at the cathode of diode CR02 and are at equal voltage. Transistor U02B and resistor R06 form a temperature compensated main load with respect to the collector current of transistor Q09. A similar load with

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respect to the collector current of transistor Q07 is formed by the network of transistor U06C and resistor R14. Transistor U02A of V/I converter 21A produces current I0.

5 Advantageously, current I0 tracks variations in current IURAMP of transistor U06A in a way to maintain vertical centering unaffected when a change in height adjustment voltage V-SIZE occurs. The tracking occurs because of circuit symmetry, for example, the symmetry with respect to transistors U06A and U02A. A transistor U02C produces the
10 emitter currents of transistors U01C and U01B. An emitter resistor R17 establishes the value of a base voltage-to-collector current ratio in transistor U02A. A resistor R49A couples a voltage CENTER, generated in a D/A converter 10a2 of FIGURE 1a, to the emitter of transistor Q09. Voltage
15 CENTER is controlled in a manner to produce approximately equal collector currents in transistors Q09 and Q07 when the zoom mode is not selected. Voltage CENTER compensates for a non-zero offset value of voltage ZOOM when the zoom mode is not selected.

20 The base voltage of transistor U01C of FIGURE 1b is controlled by current I0. The values of resistor R09 and current I0 are selected such that the base voltage of transistor U01C is equal to the level of voltage VSAW at the base of transistor U01B at the time of the midpoint of the
25 image interval, when the regular (non-zoom) mode is selected. Advantageously, as a result of tracking between V/I converters 21 and 21A, any change in size adjustment voltage V-SIZE and in the 12V supply voltage does not affect a ratio between currents I0 and IURAMP. The resulting
30 variations in currents I0 and IURAMP maintain the base voltage of transistor U01C at the level of sawtooth voltage VSAW that corresponds to vertical center for each level of voltage V-SIZE and of the 12V supply voltage, until saturation occurs. Therefore, vertical centering is,
35 advantageously, unaffected by adjustment of voltage V-SIZE that is used for adjusting picture height. The emitters of transistors U01B and U01C are coupled via emitter resistors R07 and R08, respectively, to the collector of transistor U02C

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that controls the sum of the ~~emitter currents~~. The base voltage of transistor U02C is the same as that of transistor U02A. The emitter voltage of transistor U02C, that is approximately equal to that of transistor U02B, produces an emitter current in transistor U02C that is determined by a resistor R05.

During vertical trace in the zoom mode, such as during interval t0-t1 in FIGURE 3b, transistors U01B and U01C form a differential amplifier. The collector currents of transistors U01B and U01C develop, in corresponding collector resistors, voltages that are coupled via emitter follower transistors 71 and 70 to develop sawtooth signals VRAMP2 and VRAMP1, respectively.

FIGURES 3a-3f illustrate waveforms useful for explaining the operation of the arrangement of FIGURES 1a-1c. Blanking signal B, vertical reset signal VRESET and retrace timing signal D are shown again in FIGURE 3e for comparison with the current and voltage waveforms of FIGURES 2a-2d and the functional timing diagram of FIGURE 3f, and in connection with the amount of zoom shown in FIGURES 3a-3d.

Signals VRAMP1 and VRAMP2 of FIGURES 3b and 3c, respectively, are complementary signals that change in opposite directions during the vertical trace interval t0-t1. The waveforms of FIGURES 3b and 3c that are drawn in solid line occur in the zoom mode of operation, for comparison with the waveforms in dashed line, occurring in the regular or non-zoom mode of operation. An even greater degree of zoom is shown in dash-dot line. Vertical trace occurs between, for example, time t0 and t1 when the zoom mode is selected, and between time t0 and time t2 when the zoom mode is not selected, as shown in the waveforms of FIGURES 3a-3d.

A DC coupled deflection circuit 11 of FIGURE 1c, is controlled by signals VRAMP1 and VRAMP2. In circuit 11, a deflection winding Ly provides vertical deflection in a cathode ray tube, CRT 22, for example of the type W86EDV093X710, having an aspect ratio of 16 x 9.

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Winding Ly is coupled in series with a deflection current sampling resistor R80. Winding Ly and resistor R80 of FIGURE 1c form a series arrangement that is coupled between an output terminal 11b of an amplifier 11a and a junction terminal 11c of a power supply decoupling capacitor Cb. A resistor R70 couples a supply voltage V+, for example +26 volts, to terminal 11c via an emitter follower transistor Q46. Transistor Q46 produces a DC voltage $+V/2$ at terminal 11c that is equal to about one half of voltage V+, in particular about +12.4 volts. The half supply voltage is determined by coupling the base of transistor Q46 to the junction of voltage dividing resistors R91 and R92. A junction terminal 11d, coupled between winding Ly and resistor R80, is coupled via a feedback resistor R60 to an inverting input terminal of amplifier 11a. Terminal 11c of resistor R80 is coupled via a resistor R30 to a noninverting input terminal of amplifier 11a. A negative feedback voltage is developed across resistor R80, representing the current in deflection coil Ly, and is applied to the input terminals of amplifier 11a. Amplifier 11a develops an output voltage as needed to cause the deflection coil current to track the voltage drive signal applied to the amplifier, as derived from sawtooth voltage signal VSAW by way of complementary voltages VRAMP1 and VRAMP2.

Complementary sawtooth signals VRAMP1 and VRAMP2 are coupled via resistors R40 and R50, to the noninverting and inverting input terminals, respectively, of amplifier 11a for controlling deflection current i_y . Differences between signals VRAMP1 and VRAMP2 due to component mismatch or offset voltage tolerances, for example, are compensated by a potentiometer 88 that is coupled between the collectors of transistors U01B and U01C. The vertical trace portion of deflection current i_y begins at time t_0 , shown in FIGURES 3e and 3f, when signals VRAMP1 and VRAMP2 begin to ramp from one extreme toward the other.

When top panning is utilized, signal VRESET of FIGURE 2c, is produced from or synchronized to the vertical

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synchronization pulse signal SYNC, shown in FIGURE 2e. Signal SYNC is associated with the picture information that follows signal SYNC in signal SNTSC, and occurs immediately prior to an image interval IMAGE of signal SNTSC. Image interval IMAGE of FIGURE 2e contains the picture information that is to be presently displayed on CRT 22 of FIGURE 1c. The vertical trace portion of deflection current i_y begins after the same delay time relative to the vertical sync pulse (which can be changeable when varying the extent of vertical panning), in each successive field or image interval. As a result, deflection current i_y of FIGURE 1c is properly synchronized in each period. Therefore, advantageously, field-to-field variations of sync signal SYNC will not cause vertical position jitter of the displayed picture.

FIGURE 3a illustrates in solid line the deflection current i_y waveform when a first exemplary amount of zoom is selected, and in dash-dot line the deflection current for a higher degree of zoom. The non-zoom regular mode is shown by a dashed line wherein the trace portion of the deflection current occupies most (≈ 15.7 mS) of the 16.7mS interval between successive occurrences of SYNC. FIGURES 3b-3d illustrate respective voltages using the same line conventions, and FIGURE 3e is specific to the amount of zoom shown in solid line in FIGURES 3a-3d. FIGURE 3f illustrates schematically an example of the timing diagram of signal SNTSC of FIGURE 1a, for the first exemplary amount of zoom. Interval 301 of interval IMAGE in FIGURE 3f would contain the picture information for the top half of the picture displayed in a non-zoom mode of operation. An interval 300 contains the picture information of the bottom portion of such picture; however, interval 300 is not used because the picture is zoomed such that interval 301 is used for the whole vertical display area. During interval 300, the video is blanked.

Signal SYNC, occurring at the time shown in FIGURE 3f, controls the beginning time of vertical trace in this top-panning mode. Vertical trace therefore begins, in each vertical field, at time t_0 . A top panning mode of operation is

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obtained when a bottom portion of the displayed picture is cropped by a greater amount than a top portion. Thus, the example of FIGURES 3a-3f depicts maximum top panning. This is so because a video line TOP that is the first video line of interval 301 of FIGURE 3f capable of providing picture information in the non-zoom mode of operation is also the first video line to provide the picture information in the maximum top panning mode. As discussed below, it is also possible to use a bottom panning or a centered arrangement. However, top panning is discussed first for purposes of simplicity.

In regular, non-zoom operation, the beginning time t_0 of a trace portion of current i_y of FIGURE 3a, shown in dashed line, may be delayed slightly less in order to keep the same video picture element at the top of the screen. The difference in delay compensates for the difference that occurs in the beginning of vertical trace, between the rate of change of current i_y of FIGURE 3a in the zoom mode of operation and that in the regular, non-zoom mode of operation.

The example of FIGURES 4a and 4b illustrates a comparable case wherein the last video line BOTTOM of interval 300 of image interval IMAGE is arranged to occupy the bottom of the display screen, i.e., at maximum bottom panning. Similar symbols and numerals in FIGURES 4a, 4b, 3a-3f, 2a-2e and 1a-1c are used for similar items or functions. The delay between SYNC and the commencement of the trace ramp in current i_y of FIGURE 4a with respect to signal SNTSC of FIGURE 4b is significantly longer than the delay according to FIGURE 3a, as needed to expand or zoom the bottom portion of the picture rather than the top. It will be appreciated that by choice of an appropriate delay, which can be by horizontal line counting or the like, a top pan or bottom pan, or any position in between may be selected.

It is advantageous for purposes of circuit simplicity to utilize a deflection circuit 11 as in FIGURE 1c, relying on a positive supply voltage V_+ and not requiring a negative supply voltage for generating an alternating deflection current i_y . A half supply voltage $+V/2$ is derived from the

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full supply voltage $V+$, e.g., 26 volts, for driving the deflection circuit. Current limiting resistor R70 is coupled to voltage $V+$ for generating, via transistor Q46, the half supply voltage at terminal 11c.

5 It is desirable to reduce the average or DC current through current limiting resistor R70 so that a large resistance can be used. The large value of resistor R70 is desirable to provide for current limitation so that excessive deflection current i_y may be prevented if a fault condition
10 occurs. Such fault condition may occur, for example, if output terminal 11b of amplifier 11a is shorted to ground. It may also be desirable to prevent excessive deflection current i_y in order to avoid damage to the neck of CRT 22 by a beam current strike.

15 In accordance with an inventive feature, the average value of the deflection current i_y is reduced or limited, in the zoom mode of operation. Referring to FIGURE 3a, this is accomplished by adjusting the timing of the leading edge of VRESET so that retrace commences at or near the midpoint of
20 the interval between time t_1 , when trace is completed, and time t_2 , immediately prior to the beginning of the next vertical trace. Thus, the vertical retrace interval t_a - t_b is positioned within the nontrace interval t_1 - t_2 , but is not generally adjacent to either end point t_1 or t_2 . By balancing
25 the time at which the deflection current is at its opposite extremes, the average value of the deflection current is minimized.

 As shown in FIGURE 1c, the collector of half supply transistor Q46 is coupled to the positive supply $V+$ through
30 resistor R70, and the base of transistor Q46 is coupled to a voltage divider having equal value resistors, R91 and R92, thus setting the base voltage of transistor Q46 at half the level of $V+$. The emitter of transistor Q46 is thereby regulated to half the voltage at $V+$, less the forward biased
35 base-emitter voltage of transistor Q46. The current I_s supplied by the half supply, flowing through resistor R70, produces a voltage signal at the collector of transistor Q46 representing the level of current I_s . This voltage signal is

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filtered by the network including capacitor C71 and resistors R71 and R73, and applied to the base of an error amplifier transistor Q73. The network of capacitor C71 and resistors R71 and R73 form an integrator applying to error amplifier Q73 a voltage that varies with the average current supplied through half supply transistor Q46. The output of the error amplifier transistor Q73 is a current proportional to the amount by which the half supply current exceeds a reference level of about 13 mA according to the circuit values of the embodiment shown. The half supply emitter resistor R79 sinks about 21 mA. Feedback via diode CR71 causes the circuit to regulate near 21 mA, keeping supply transistor Q46 in conduction during at least a portion of the vertical interval.

Referring to FIGURE 1a, the current output IERROR of error amplifier transistor Q73 is coupled to a timing capacitor C17. The timing capacitor is disabled by a timer switch Q02 and an inverter Q01, except when signal B is high. Signal B is the vertical blanking signal generated by microprocessor 10a, and is at the high blanking level except during vertical trace. It is used by blanking circuitry, not shown, to blank the screen of CRT 22. In the zoom mode, the leading edge of blanking occurs earlier than the vertical timing signal A, generated by the microprocessor to initiate a new vertical trace in the non-zoom mode.

Current signal IERROR from error amplifier Q73 in FIGURE 1c is coupled to capacitor C17, charging the capacitor to produce a voltage signal D as shown in FIGURE 2d (see also FIGURE 3e), that ramps upwardly at a rate proportional to IERROR. This timing signal D is coupled to the base of transistor Q04, which forms a buffer between capacitor C17 and the threshold input of flip-flop IC U07. The threshold input of IC U07 is one input to a comparator U7a, the other input being coupled internally to a voltage divider setting a threshold of about 3.4 volts. When the buffered ramp exceeds the threshold level, the set input of the flip-flop FF in IC U07 triggers, causing the Q output of flip-flop FF to go high and the low-true output at pin 3 to go low. This low-true output is coupled to the base of a transistor

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Q10, which clamps the VRESET signal C high, initiating a fast vertical retrace by clamping voltage signal VSAW via transistors U01A and U01B in FIGURE 1b. Simultaneously, the output of the flip-flop in IC U07 turns on a transistor Q11 to discharge timing capacitor C17.

The amount of current IERROR produced by the error amplifier of Q73 in FIGURE 1c is determined by the emitter voltage set by the voltage divider of resistors R75 and R77, and by the voltage signal at the base of transistor Q73, coupled from the collector of the half supply regulator transistor Q46 by resistor R71. The gain of the current amplifier is set in conjunction with the value of timing capacitor C17 (FIGURE 1a) and the threshold defined by the internal voltage divider in IC U07 such that the threshold is reached and retrace is initiated at a time causing the deflection current during retrace to cross zero current near the midpoint of the blanking interval, as shown in FIGURE 3a. As a result, the DC component of the deflection current is appropriately small, and can be zero or a small absolute value.

The timer IC U07 remains in a state clamping VRESET high, until the vertical blanking signal B from microprocessor 10a drops below the trigger input voltage of IC U07. The trigger input of IC U07 is also arranged to be coupled to a comparator U7b which triggers at about 1.7 volts. When this occurs, signalling the beginning of a new vertical trace, output pin 3 of IC U07 again goes high, releasing the clamping of VRESET and allowing VSAW to begin a new trace ramp. Simultaneously, IC U07 releases discharge pin 7, enabling timer capacitor C17 for timing during the next vertical blanking pulse B.

Vertical timing signal A from microprocessor 10a is OR'ed with timing ramp signal D via resistor R73, coupled to the threshold input of IC U07 and the emitter of buffer transistor Q04. In the normal (non-zoom) mode of operation, timing ramp signal D may not reach the threshold level at the input of IC U07 before the leading edge of vertical timing signal A. In that mode, the leading edge of timing signal A

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sets the flip-flop in IC U07 and initiates clamping of VRESET and retrace of VSAW synchronously with the leading edge of timing signal A.

5 The circuit as thus described causes the leading edge of VRESET in the zoom mode, and the initiation of vertical retrace by clamping signal VSAW, to occur after the beginning of blanking (i.e., after the change of state of signal B), by an amount determined by the ramping voltage on signal D. The circuit responds adaptively to changes in the
10 amount of zoom, to minimize the DC current loading of the half supply. As discussed above, the error amplifier of transistor Q73 produces a current representing the amount by which the half supply current varies from a reference level.

15 Assume the amount of zoom and the slope of the trace ramp are increased suddenly, for example from the amount shown in solid line in FIGURE 3a to the amount shown in dash-dot line, so that the deflection current reaches its negative maximum sooner. Before further servo adjustment
20 is initiated, the longer dwell time, for example at the negative maximum, for a greater proportion of the vertical interval, produces a DC deflection current offset and a change in DC current loading of the half supply. This results in the current output of error amplifier Q73 being likewise changed as a
25 function of the difference in supplied current from the reference level. A larger current IERROR then causes a faster rising ramp in signal D, making VRESET occur earlier in the vertical blanking period defined by signal B.

30 In this manner, if the amount of zoom is increased and the deflection current reaches its negative peak sooner, the delay between the blanking signal and the vertical reset is increased and the retrace is advanced in a feedback servo manner. Similarly, if the amount of zoom is decreased, such that the negative peak occurs later, retrace is retarded
35 to a later point in the vertical blanking period. As illustrated by the dashed line waveform of FIGURE 3a, at the latest, retrace occurs between times $t_2'-t_2$, with the vertical synchronizing signal A, defining the normal, non-zoom mode.

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For any amount of zoom, the timing of retrace is adjusted automatically to occur at or near the midpoint of retrace, by the advantageous feedback control circuit, wherein DC current loading of the half supply is sensed and controlled by adjusting the timing of the leading edge of VRESET.

Signal VSAW as shown in FIGURE 3d continues to ramp downwardly during the beginning of the blanking interval; however, VRAMP1 and VRAMP2 level out at the saturation voltages of the differential amplifier arrangement of FIGURE 1b, e.g., at about 2.3 and 4.3 volts, respectively. At the leading edge of VRESET, signal VSAW is clamped high by transistor U01A, causing VRAMP1 and VRAMP2 to switch to their opposite states. Deflection amplifier 11a in FIGURE 1c then ceases operating in a linear feedback mode and a voltage VB at supply terminal 6 of amplifier 11a is applied to deflection winding Ly via output terminal 11b. A retrace voltage V11b is produced immediately after time ta in FIGURE 3a, to enable deflection current iy to complete retrace by time tb. Switch 11f1 in FIGURE 1c of a boost stage 11f causes a capacitor 11g to be coupled in series with a boost capacitor 11e. Capacitor 11e is charged via a diode X and a switch 11f2 from the +26V supply voltage V+, during vertical trace. A supply voltage, developed across filter capacitor 11g, is summed up with a voltage developed across boost capacitor 11e so as to form boost voltage VB. Voltage VB is decoupled from the +26V supply voltage V+ via a diode DR, when boost voltage VB is formed. During the short interval ta-tb in FIGURES 3a and 3e, retrace portion RETRACE of current iy is produced. Electromagnetic energy stored in deflection winding Ly of FIGURE 1c due to current iy is used in the boost circuit, shown schematically as switch 11f1, to generate the vertical retrace voltage V11b at terminal 11b of FIGURE 1c that is larger than voltage V+, causing a fast retrace.

Near time tb, deflection current iy has increased in value to a point which permits linear operation of amplifier 11a. Feedback from resistor R80 enables the deflection current to follow the flat top portions of VRAMP1 and

VRAMP2 between times t_b and t_2 . At the end of vertical retrace, at time t_2 deflection amplifier 11a of FIGURE 1c, operating in its linear feedback mode, again produces the sawtooth trace portion of deflection current i_y .

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WHAT IS CLAIMED IS:

1. A video display apparatus, comprising:
 - a cathode ray tube (22);
 - a vertical deflection winding (L_y) on said cathode ray tube;
 - a source (10a1) of an image control signal (ZOOM) representing an image scale factor selected from a range of values;
 - a source (9) of a vertical synchronization signal (SYNC);
 - a deflection ramp generator (100) responsive to said synchronization and image control signals for generating a ramp (VSAW) with a slope that varies with the selected scale factor; characterized by
 - a deflection amplifier (11a) responsive to said ramp for generating in said deflection winding a cyclical deflection current (i_y) having a period of a vertical interval, the deflection current ranging between a first extreme (+IP) and a second extreme (-IP) during a trace interval (t_0-t_1) that is shorter than the vertical interval (t_0-t_2) by a time (t_1-t_2) that varies with the selected scale factor; and
 - a retrace signal (VRESET) generator (10a, Q73, C17, U07) operable to return the deflection current from the second extreme to the first extreme during a retrace interval (t_a-t_b) that is positioned within a nontrace interval (t_1-t_2), but not generally positioned adjacent to either end point of the trace interval.
2. The video display apparatus according to Claim 1, characterized in that a timing means (10a, Q73, C17) of the retrace signal generator is operable to generate said retrace interval substantially centered about a midpoint of the time by which the trace interval (t_0-t_1) is shorter than the vertical interval (t_0-t_2).
3. The video display apparatus according to Claim 1, characterized in that the ramp generator, the deflection amplifier and the deflection winding form a DC-coupled vertical deflection circuit (11), and the retrace signal



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generator reduces a DC average current (I_s) in said deflection winding.

4. The video display apparatus according to Claim 3, characterized in that the retrace signal generator is coupled in a feedback loop to the vertical deflection circuit to advance or retard the retrace interval to minimize the DC average current.

5. The video display apparatus according to Claim 4, characterized in that the retrace signal generator includes a current error amplifier (Q73) coupled to the vertical deflection circuit and operable to produce an error current signal as a function of a difference between the DC average current and a reference level, the error current signal being coupled to charge a capacitor (C17), and further comprising a threshold detector (U7a) operable to trigger the initiation of the retrace interval when a timing ramp signal (D) on the capacitor reaches a threshold.

6. The video display apparatus according to Claim 4, further characterized by a power supply (V_+ , Q46) for generating a first supply voltage (V_+) and a second supply ($+V/2$) voltage having the same polarity as said first supply voltage, the first and second supply voltages being coupled to opposite ends of the deflection winding.

7. The video display apparatus according to Claim 6, further characterized by a current limiting resistor (R80) coupled to the deflection circuit, a lower ($+V/2$) voltage one of the first and second supply voltages being coupled to a terminal (11c) of said resistor remote from said deflection amplifier.

8. The video display apparatus according to Claim 4, further characterized by a current limiting resistor (R80) coupled to the deflection circuit, and wherein the retrace



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signal generator is operable to minimize a DC current flowing in the current limiting resistor.

9. The video display apparatus according to Claim 4 further characterized by a power supply (V+, Q46) for generating a first supply voltage (V+) and a second supply voltage (+V/2) having the same polarity as said first supply voltage, the first and second supply voltages being coupled to opposite ends of the deflection winding.

10. The video display apparatus according to Claim 1, characterized in that said retrace signal VRESET is time shifted relative to the vertical synchronization signal for panning to a zoomed portion of a picture being displayed.

11. The video display apparatus according to Claim 1, characterized in that said retrace signal generator centers said retrace interval within said nontrace interval.

12. The video display apparatus according to Claim 1, characterized in that said deflection amplifier maintains said deflection current near said second extreme from the end of said trace interval to the beginning of said retrace interval and maintains said deflection current near said first extreme from the end of said retrace interval to the beginning of the next subsequent trace interval.

13. The video display apparatus according to Claim 12, characterized in that said retrace signal generator centers said retrace interval within said nontrace interval.

14. A video display apparatus, comprising:
a cathode ray tube (22);
a vertical deflection winding (L_y) on said cathode ray tube;
a source (9) of a vertical synchronization signal (SYNC);



a deflection ramp generator (100) responsive to said synchronization signal for generating a synchronized ramp (VSAW); characterized by

a deflection amplifier (11a) responsive to said ramp for generating in said deflection winding a cyclical deflection current (I_y) having a period of a vertical interval (t_0 - t_2), the deflection current ranging between a first extreme (+IP) and a second extreme (-IP) during a trace interval (t_0 - t_1) that is shorter than the vertical interval; and

a servo circuit (10a, Q73, C17, U07) coupled to said deflection amplifier for positioning a retrace interval (t_a - t_b) within a nontrace interval (t_1 - t_2) by means of servo feedback control.

15. The video display apparatus according to Claim 14, characterized in that said servo circuit centers said retrace interval within said nontrace interval.

16. The video display apparatus according to Claim 15, characterized in that said deflection amplifier maintains said deflection current near said second extreme (-IP) from the end (t_1) of said trace interval to the beginning (t_a) of said retrace interval and maintains said deflection current near said first extreme (+IP) from the end (t_b) of said retrace interval to the beginning (t_2) of the next subsequent trace interval.

17. The video display apparatus according to Claim 14, characterized in that said servo circuit includes means (R70) for generating a signal (I_s) representative of average deflection current and means (Q73) responsive to said average deflection current representative signal for providing servo feedback control of said average deflection current.

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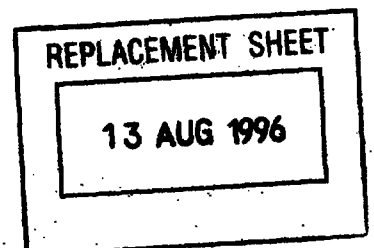
VERTICAL RETRACE WITH ZOOM AND CENTERED FAST RETRACE

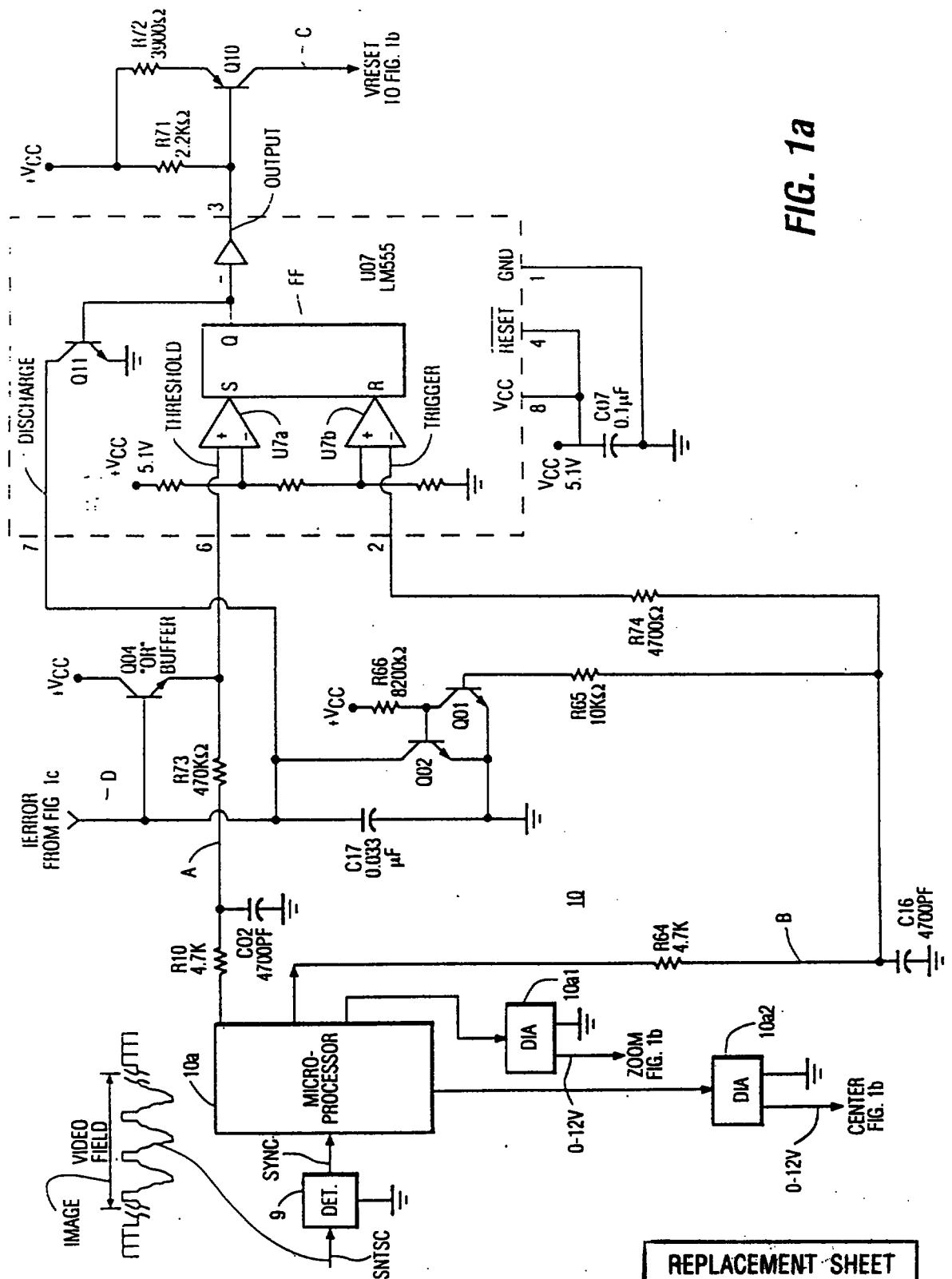
ABSTRACT

A television receiver is controlled as to the degree of vertical zoom via a deflection current ramp that varies in slope and which may be delayed to achieve panning. Due to the increased slope when zoomed, the deflection current and the electron beam complete a trace in less time than the normal vertical interval. The deflection current is maintained at one extreme or the other outside the trace interval, and the beam is blanked. A retrace signal generator (10a, C17, U07) coupled in a feedback (IERROR) loop with the power supply for the deflection circuit determines the midpoint of the blanking period and generates a fast retrace (VRESET) at or near the midpoint. The feedback loop is arranged to minimize the DC average current in the deflection winding by having a current source responsive to the DC average current for charging a timing ramp (C17) that triggers retrace upon reaching a threshold. The slope of the timing ramp varies with DC loading, thus advancing or retarding retrace to center retrace in the blanking interval.

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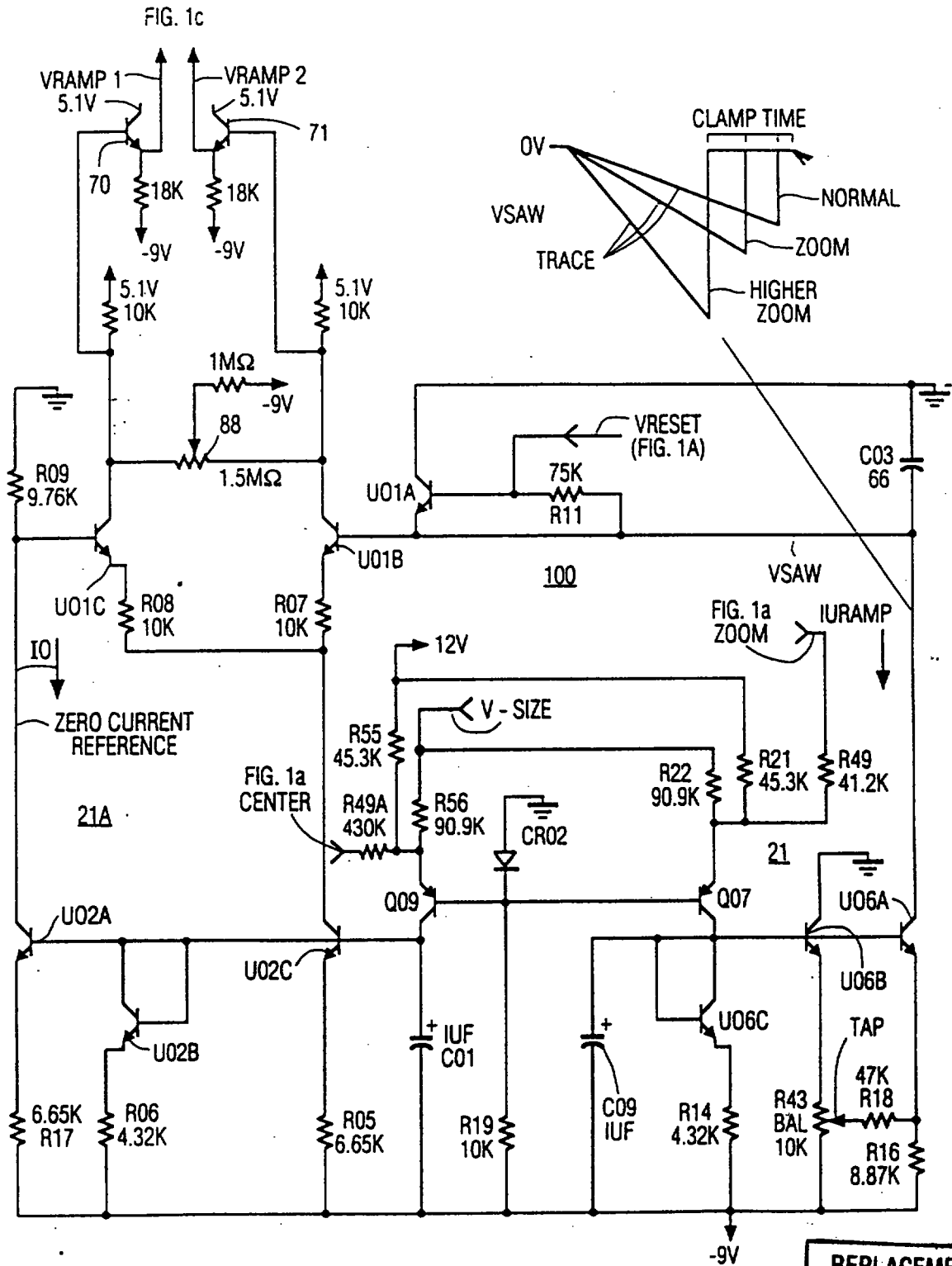
FIGURE 1a





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FIG. 1b

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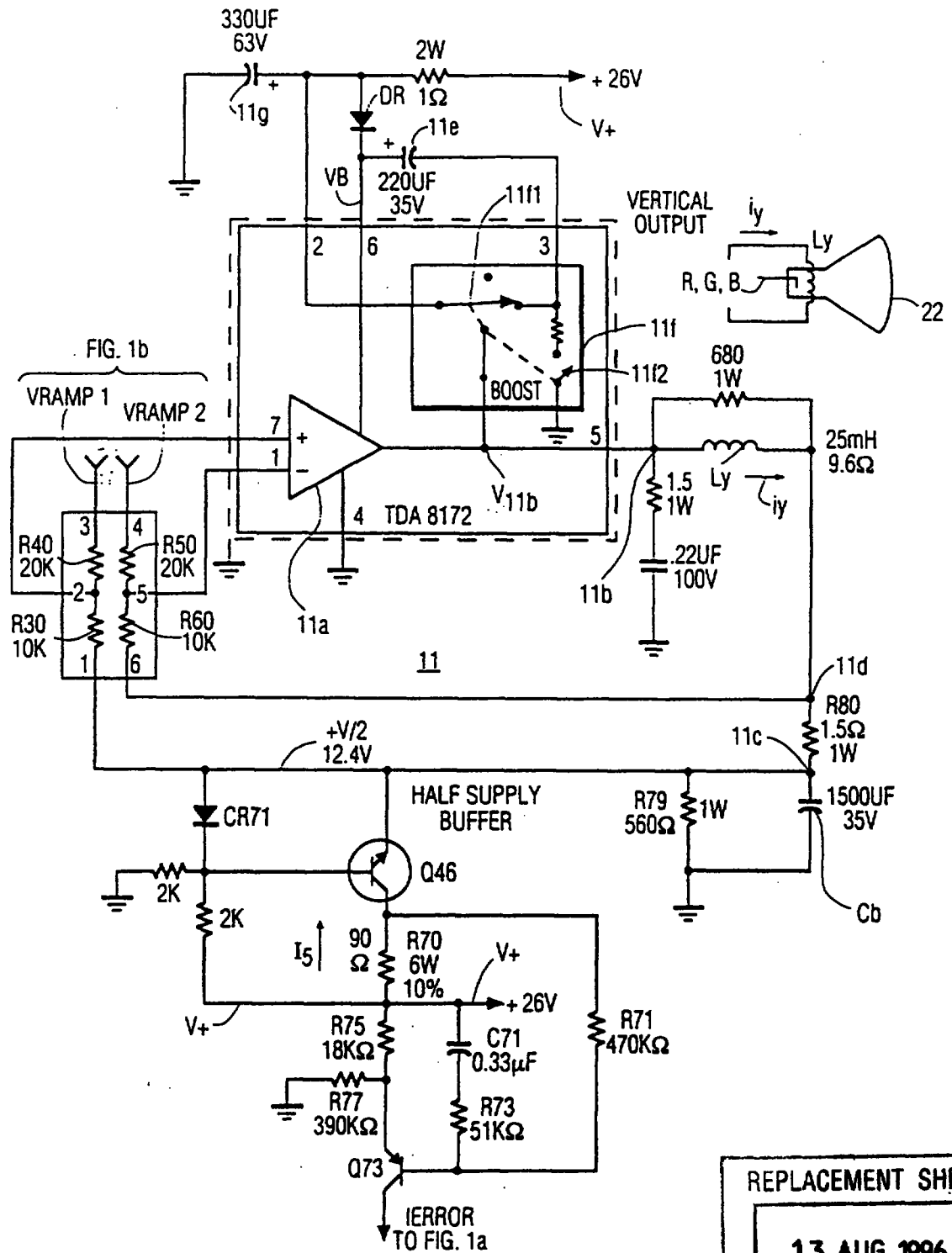


FIG. 1c

FIG. 2e

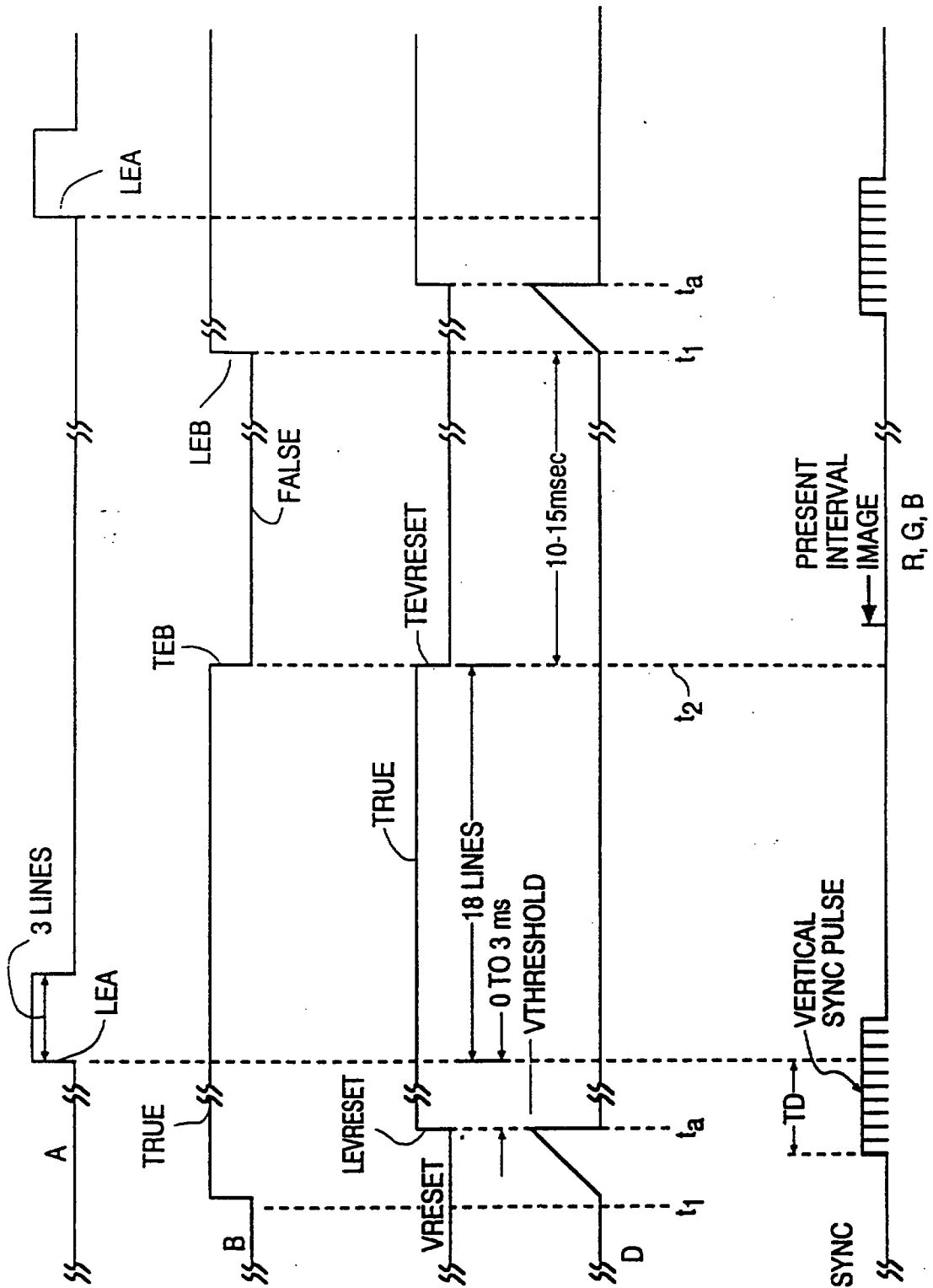
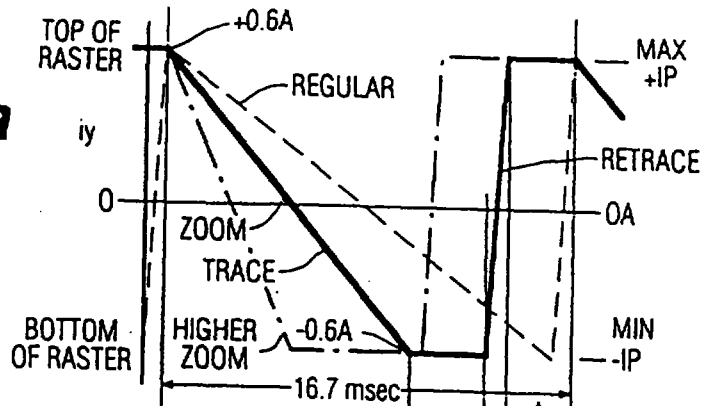
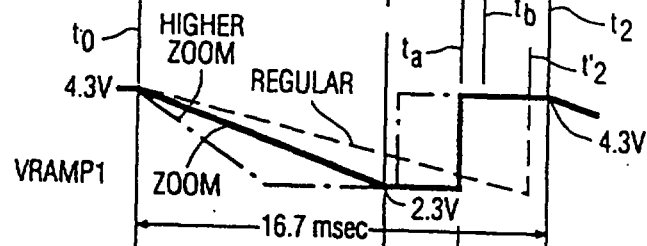
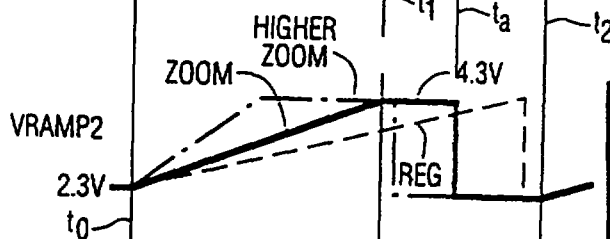
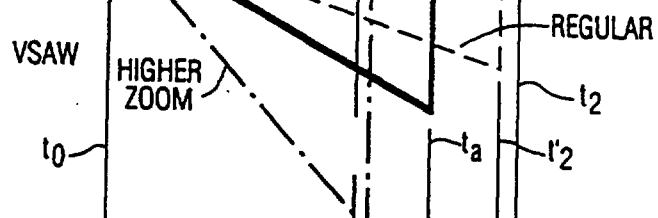
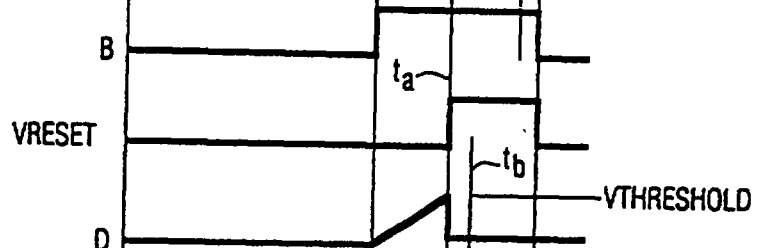
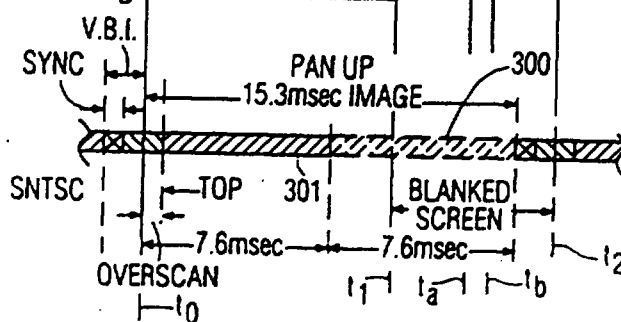
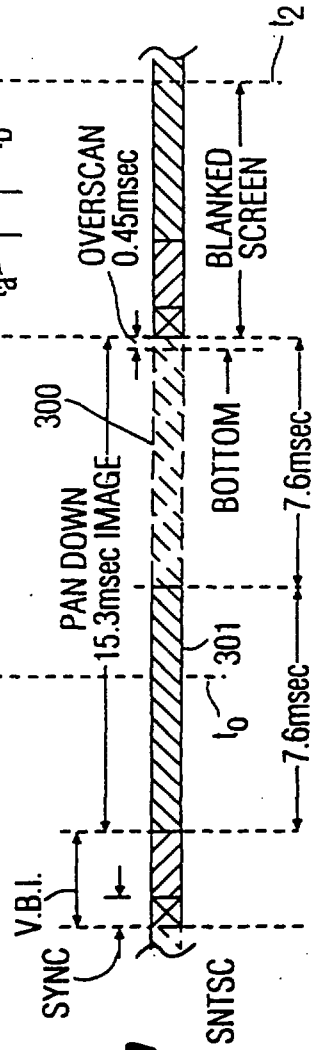
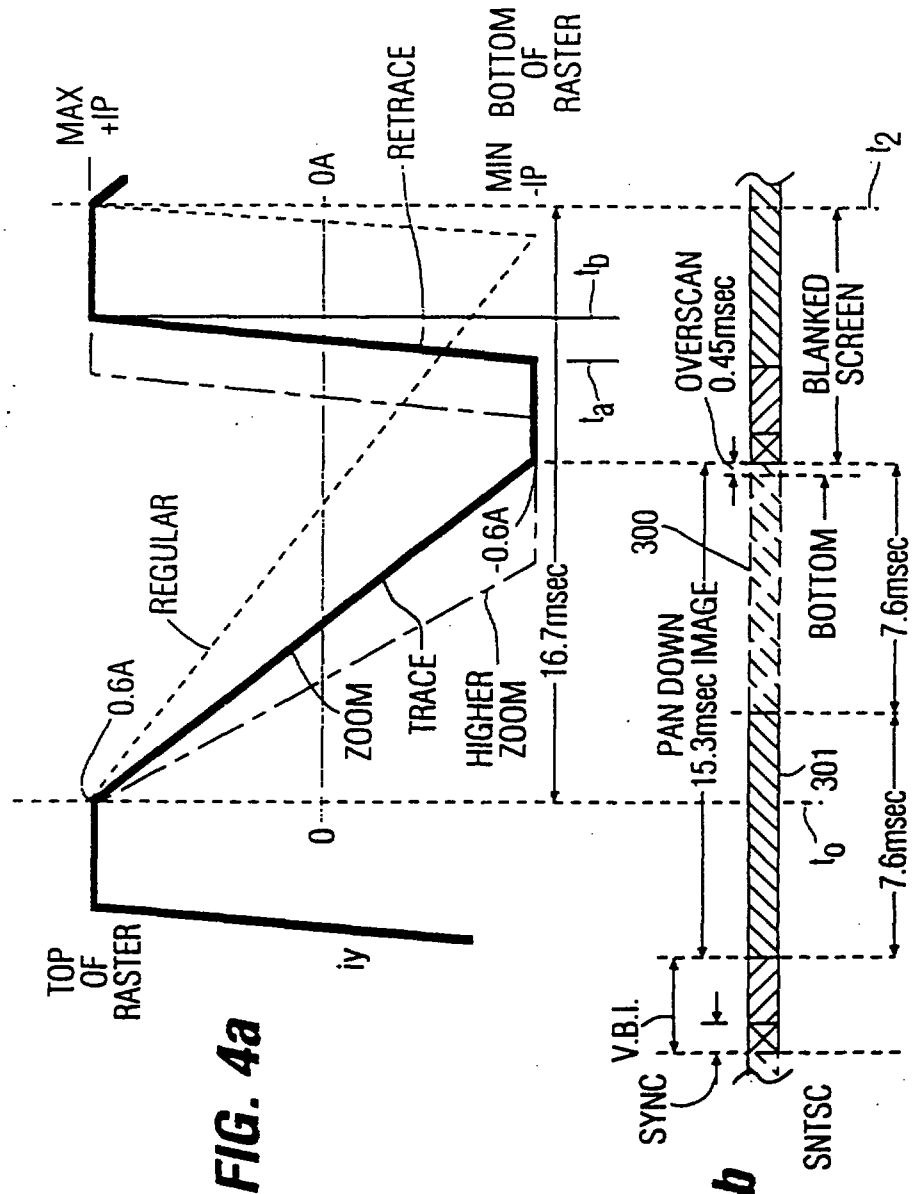


FIG. 3a**FIG. 3b****FIG. 3c****FIG. 3d****FIG. 3e****FIG. 3f**

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