The invention relates to a method of determining in which direction a scanner travels across markings or crosses data tracks on a recording medium, in which there are generated a first error signal and a second error signal shifted in phase relative to the first error signal depending upon the direction of motion of the scanner.

CD-players, video-disc players, DRAW-disc players or magneto-optical recording- and playback devices are equipped, for example, with a tracking control circuit and an optical scanning device.

The construction and function of an optical scanning device, a so-called optical pick-up, are described in "Electronic Components & Applications", Vol. 6, No. 4, 1984 on page 209 - 215.

The light beam emitted by a laser diode is focused by means of lenses onto the CD-disc, from where it is reflected onto a photodetector. The data stored on the CD-disc and the actual value for the focus- and tracking control circuit are obtained from the output signal of the photodetector. In the aforementioned publication the deviation of the actual value from the theoretical value for the focus control circuit is referred to as focusing error, while the term radial tracking error is selected for the deviation of the actual value from the theoretical value of the tracking control circuit.

A coil, via the magnetic field of which an objective lens is moveable along the optical axis, serves as control element for the focus control circuit. By displacing the objective lens the focus control circuit causes the light beam emitted from the laser diode always to be focused onto the CD-disc. By means of the tracking control circuit, which is often also referred to as radial drive means, the optical scanning

device is displaceable in the radial direction relative to the CD-disc. In this way the light beam can be guided over the spiral-shaped data tracks of the CD-disc.

In some devices the radial drive means is constructed from a so-called coarse drive and a so-called fine drive. The coarse drive is constructed, for example, as a spindle by means of which the entire optical scanning device comprising the laser diode, the lenses, the prismatic beam divider and the photodetector, is radially displaceable. By means of the fine drive the light beam is additionally displaceable in the radial direction or can be tilted for example by a predeterminable, small angle. Therefore by means of the fine drive the light beam can be moved by a small amount - approximately 1 mm - along a radius of the CD-disc.

In order to achieve satisfactory reproduction of the data, whether for example picture and sound in the case of a video-disc player or simply sound in the case of a CD-player or the data of a magneto-optical disc, in addition to precise focusing of the light beam onto the disc, precise guidance along the data tracks of the disc is also necessary.

Figure 1 illustrates the photodetector PD of the optical scanning device of a CD-player wherein three laser beams L1, L2 and L3 are focused onto the CD-disc. The laser beams L2 and L3 are the diffraction beams of the +1st and -1st order. Such a scanning device is referred to in the publication mentioned in the introduction as three-beam pick-up since it operates with three light beams.

In the photodetector four square-shaped photo-diodes A, B, C and D are assembled in such manner that they in turn form a square. The square formed by the four photo-diodes A, B, C and D is preceded by a rectangular photo-diode E; the square

is followed by a further photo-diode F. The central laser beam L1, which is focused onto the four photo-diodes A, B, C and D, generates the data signal HF = AS + BS + CS + DS and the focus error signal FE = (AS + CS) - (BS + DS). The two outer light beams L2 and L3, of which the front light beam L3 falls onto the photo-diode E and the rear light beam L2 falls onto the photo-diode F, generate the tracking error signal T = ES - FS. The photo-voltages of the diodes A, B, C, D, E and F are referenced AS, BS, CS, DS, ES and FS respectively.

In Figure 1 the central laser beam L1 accurately follows the centre of a track S. The tracking error signal TE has the value zero.

$$TE = ES - FS = 0.$$

If the central light beam moves away from the centre of a track S, one diffraction beam moves more towards the centre of the track while the other diffraction beam shines onto the interspace between two tracks S. However, because the reflection properties of a track and an interspace are different, one diffraction beam is reflected more strongly than the other.

Figure 2 illustrates the situation in which the laser beams L1, L2 and L3 are displaced towards the right away from the track S. The tracking error signal assumes a negative value:

$$TE = ES - FS < 0.$$

The control element of the tracking control circuit now moves the optical scanning device towards the left until the tracking error signal TE becomes zero.

In the converse situation when the laser beams are displaced towards the left away from the track, the tracking error signal is positive: TE = ES - FS > 0. Now the control element of the tracking control circuit moves the optical scanning device to the right until the tracking error signal TE becomes zero. This situation is shown in Figure 3.

When the light beam L1 and the associated diffraction beams L2 and L3 cross a plurality of data tracks, the tracking error signal TE assumes the sinusoidal course shown in Figure 4.

JP-A-60-10429 has disclosed a tracking control circuit wherein it is recognised at the lower and upper envelopes of the HF-signal whether the light beam is crossing data tracks. When the light beam travels across a plurality of data tracks, the HF-signal regularly breaks down between two tracks.

In order to determine the number of tracks travelled across by the light beam, the envelope of the HF-signal is formed and converted into a pulse-shaped signal which is fed to the counting input of a forwards-backwards counter. In this way the breaks in HF are counted by the forwards-backwards counter.

In order to determine in which direction the light beam is moved, radially inwards or outwards, a so-called direction determining logic circuit is required which evaluates the phase shift between the tracking error signal TE and the envelope of the HF-signal. The phase shift amounts to either + 90° or - 90° depending upon the direction of motion of the light beam. However, these two values apply only to relatively low speeds of the light beam, as will now be explained.

A rectangular tracking error signal is produced from the sinusoidal tracking error signal TE by means of a RC element. The time constant is therefore equal both for the ascending and the descending edges. However since a rectangular envelope signal is obtained from the envelope of the HF-signal by means of a RC element and by following peak value rectification, the time constants for the ascending and descending edge are different. This difference increases with the speed of the light beam.

For example it is known to supply the tracking error signal TE to the D-input of a D flip-flop and the envelope of the HF-signal to its clock input. Therefore the D flip-flop is always supplied with a pulse at its clock input when the light beam crosses a data track. However, because the sign of the tracking error signal TE is dependent upon the direction in which the light beam leaves a data track, in one direction the D flip-flop is set - its output changes to "HIGH" - whereas in the other direction its output remains at "LOW". The signal at the Q-output of the D flip-flop can therefore serve to determine the counting direction - forwards or backwards - of a forwards-backwards counter. Therefore the forwards-backwards counter counts forwards in the case of the one direction whereas it counts backwards in the case of the other direction.

A disadvantage consists in that at high search speeds when the light beam is moved very rapidly across the tracks, because of the different time constant the phase shift between the envelope of the HF-signal and the tracking error signal no longer amounts to + 90° or - 90 °; therefore since the phase shift now assumes an undefined state, at high speeds the direction of motion of the light beam can no longer be determined.

Because the rectangular signal obtained from the envelope of the HF signal is affected by bounce, debouncing measures must additionally be employed.

Therefore the aim of the invention is to contrive a method for determining in which direction a scanner travels across markings or crosses data tracks on a recording medium in such manner that it is indicated in which direction the scanner travels across the markings or crosses the data tracks of a recording medium.

The invention fulfils this aim in that the phase shift between the first error signal and the second error signal is evaluated for the determination of the direction of motion of the scanner only when the speed at which the scanner travels across markings or crosses data tracks is below a predeterminable threshold value, and that otherwise however the direction last determined is maintained as a valid measured value.

The invention is based upon the recognition that the speed of the scanning light beam cannot change suddenly. When the light beam is moved across the tracks, its speed increases not suddenly but steadily from zero to the highest value. Therefore at least at the start of the motion, the phase shift between the pulse-shaped tracking error signal TZ and the pulse-shaped envelope signal HP amounts to + 90° or -90° depending upon the direction of motion. If the speed of the light beam now reaches such a high value that the edges of the pulse-shaped envelope signal HP and of the pulse-shaped tracking error signal TE no longer occur in an alternating sequence, the direction determining logic circuit RL maintains the last determined direction. However, since the light beam cannot change suddenly from one direction of motion into the other, but is firstly decelerated to a halt, the edges of the pulse-shaped envelope signal HP and of the

pulse-shaped tracking error signal again occur in alternating sequence. The phase shift again becomes up to + 90° or - 90° depending upon whether the light beam is moved radially inwards or outwards. The direction determining logic circuit RL now evaluates the phase shift again and can thus determine the direction of motion of the light beam. When the light beam now reverses its direction of motion, the sign of the phase shift is likewise reversed. The direction determining logic circuit RL thereby recognises the change in the direction of motion.

If the light beam moves in one direction, an ascending or descending edge of the pulse-shaped envelope signal HP is always followed respectively by a descending or ascending edge of the pulse-shaped tracking error signal TZ. An edge of the one type in the one signal is followed by an edge of the opposite type in the other signal.

If, conversely, an edge of the pulse-shaped envelope signal HP is always followed by a like edge of the pulse-shaped tracking error signal TZ, the direction determining logic circuit recognises that the light beam is moving in the other direction. An edge of the one type in the one signal is followed by an edge of the same type in the other signal.

If the speed of the light beam - now in the opposite direction to previously - attains such a high value that the edges no longer occur in alternating sequence, the direction determining logic circuit maintains the direction last determined.

Figure 5 illustrates a first exemplary embodiment of the invention;

Figure 6 illustrates a second exemplary embodiment of the invention;

Figures 7, 8 and 9 are pulse diagrams in explanation of the invention.

In Figure 5 the direction determining logic circuit has been referenced RL, while the detection circuit, which indicates by means of a signal when the light beam is crossing a track, has been referenced Z.

The first exemplary embodiment of the invention shown in Figure 5 will now be described and explained.

The output of an inverter I1 is connected to the first input of an AND gate U1 and an AND gate U3. The input of the inverter I1 is connected to the first input of an AND gate U2 and an AND gate U4. The output of an inverter I2 is connected to the second input of the AND gate U2 and the AND gate U3. The input of the inverter I2 is connected to the second input of the AND gate U1 and the AND gate U4. The output of the AND gate U1 is connected to the set input of a RS flip-flop F1, the reset input of which is connected to the output of the AND gate U2. The output of the AND gate U3 is connected to the set input of a RS flip-flop F2, the reset input of which is connected to the output of the AND gate U4. The Q-output of the RS flip-flop F1 is connected to the first input of an AND gate U6 and via a delay element V1 to the clock input of a D flip-flop F3, the Q-output of which is connected to the first input of an AND gate U5. The $\overline{Q}$-output of the RS flip-flop F1 is connected to the reset input of the D flip-flop F3 and to the data input of a D flip-flop F4, the Q-output of which is connected to the second input of the AND gate U6. The Q-output of the RS flip-flop F2 is connected to the second input of the AND gate U5 and via a delay element V2 to the clock input of the D flip-flop F4, the reset input of which is connected to the $\overline{Q}$-output of the RS flip-flop F2 and to the data input of the RS flip-flop F3. The output of the AND gate U5 is connected

to the set input of a RS flip-flop F5, the reset input of which is connected to the output of the AND gate U6. The Q-output of the RS flip-flop F5 is connected to the first input of an AND gate U7, the $\overline{Q}$-output of which is connected to the first input of an AND gate U8. The output of a detection circuit Z is connected to the second input of the AND gates U7 and U8.

The input of the inverter I1 is supplied with the pulse-shaped envelope signal HP obtained from the envelope of the HF signal HF, whereas the input of the inverter I2 is supplied with the pulse-shaped tracking error signal TZ formed from the sinusoidal tracking error signal TE. The RS flip-flop F5 emits a logical 1 from its Q-output when the light beam crosses tracks in one direction; conversely a logical zero occurs at the Q-output of the RS flip-flop F5 when the light beam crosses tracks in the other direction. The detection circuit Z determines when the light beam leaves a track. It emits a logical one from its output when the light beam falls not onto a track, but onto the space between two tracks for which the technical term is "grass" ("Rasen"). If the light beam is directed onto a track, a logical zero occurs at the output of the detection circuit Z. The AND gates U7 and U8 are therefore disabled for such time as the light beam shines onto a track. The AND gate U7 emits a counting pulse when the light beam scanning the data crosses a track on the recording medium for example from right to left; conversely the AND gate U8 emits a counting pulse when the light beam crosses a data track in the opposite direction, thus from left to right.

The counting pulses at the output of the AND gate U7 can for example be supplied to a forwards counter or the forwards counting input of a forwards-backwards counter. The counting pulses at the output of the AND gate U8 are then

counted by a backwards counter or the backwards counting input of the forwards-backwards counter.

When the speed of the light beam attains such a high value that the edges of the pulse-shaped envelope signal HP and of the pulse-shaped tracking error signal TZ no longer occur in alternating sequence, the RS flip-flop F5 maintains its state. It remains set or reset depending upon the last determined direction of motion of the light beam. Therefore the RS flip-flop F5 changes its state when a change occurs in the sequence of the edges of the pulse-shaped envelope signal HP and the pulse-shaped tracking error signal TZ. If a plurality of edges of the same signal occur in succession, no change occurs in the state of the RS flip-flop F5.

The second exemplary embodiment illustrated in Figure 6 shows the construction of the detection circuit Z and the manner in which it is connected to the direction determining logic circuit RL.

The pulse-shaped envelope signal HP is fed to the input of a monoflop M1 which is triggerable by a descending edge and the output of which is connected to the first input of an AND gate U9. The pulse-shaped tracking error signal TZ is fed to a monoflop M2 which is likewise triggerable by a descending edge and to the first input of an OR gate 01. The inverted pulse-shaped tracking error signal $\overline{TZ}$ is fed to a monoflop M3 triggerable by an ascending edge and to the first input of an OR gate 02. The outputs of the monoflops M2 and M3 are connected to the inputs of an OR gate 03, the output of which is connected to the reset input of a RS flip-flop F6. The output of the AND gate U9 is connected to the set input of the RS flip-flop F6. The outputs of the OR gates 01 and 02 are connected to the inputs of an AND gate U10, the output of which is connected to the second input of the AND gate U9. The output of the AND gate U8 of the

direction determining logic circuit RL is connected to the second input of the OR gate 02, while the output of the AND gate U7 is connected to the second input of the OR gate 01. The Q-output of the RS flip-flop F6 and the output of the detection circuit Z are connected to the second input of the AND gates U7 and U8.

The function of the first and second exemplary embodiments will now be explained making reference to the pulse diagrams shown in Figures 7, 8 and 9.

In Figure 7 it is indicated in the HF signal HF that the light beam travels from the track 0 across the tracks 1 and 2 to the track 3 where it reverses its direction and travels back to the track 0 via the tracks 2 and 1. The signals for this assumed example have been shown in Figure 7.

The signals HP, $\overline{HP}$, TZ and $\overline{TZ}$ are linked to one another in the AND gates U1, U2, U3 and U4. The signals at the outputs of the AND gates U1, U2, U3 and U4 formed as a result of the linking, which are still affected by bounce, have been referenced U1, U2, U3 and U4 in the pulse diagrams in Figure 8. From these signals the signal H is formed at the Q-output of the RS flip-flop F1 and the signal $\overline{H}$ is formed at the $\overline{Q}$-output. The signal at the Q-output of the RS flip-flop F2 has been referenced G, while the signal at its $\overline{Q}$-output has been referenced $\overline{G}$. From the bounce-free signals H, $\overline{H}$, G and $\overline{G}$, the signal K is formed at the Q-output of the D flip-flop F3 and the signal L is formed at the Q-output of the D flip-flop F4. The signals at the outputs of the monoflops M1, M2 and M3, which react to the bounce in the signal TZ, $\overline{TZ}$ and HP, have been referenced by the same letters in Figure 9 as the monoflops. The signals at the AND gates U7, U8, U9 and U10, at the OR gate 03 and at the RS flip-flop F6 have likewise been provided in the diagram

in Figure 9 with the same letters as the associated components.

The second exemplary embodiment shown in Figure 6 can be constructed for example in accordance with I^2L technology.

The invention is generally suitable for counting devices for the counting of markings or for control circuits for the positioning of a unit, for example a scanner, wherein the positioning is effected by the scanning of markings. The form of scanning - mechanical or contactless - is of no significance. The invention is particularly suitable for tracking control circuits such as are to be found for example in CD-players, video-disc players, DRAW-disc players or magneto-optical devices.

Claims

1. A method for determining in which direction a scanner travels across markings or crosses data tracks on a recording medium, in which there are generated a first error signal (HP) and a second error signal (TE) shifted in phase relative to the first error signal (HP) depending upon the direction of motion of the scanner, characterised in that the phase shift between the first error signal (HP) and the second error signal (TE) is evaluated for the determination of the direction of motion of the scanner only when the speed at which the scanner travels across markings or crosses data tracks is below a predeterminable threshold value, and in that otherwise the direction last determined is maintained as a valid measured value.

2. A method according to Claim 1 for a tracking control circuit, characterised in that a pulse-shaped tracking error signal (TZ) is generated from a sinusoidal tracking error signal (TE), in that a pulse-shaped envelope signal (HP) is generated from the envelope of the HF signal (HF) which a light beam generates on reading the data from the recording medium, in that the phase shift between the tracking error signal (TE) and the pulse-shaped envelope signal (HP) of the HF signal (HF) is evaluated for the determination of the direction of motion of the light beam only when the speed at which the light beam crosses data tracks is below the predeterminable threshold value.

3. A method according to Claim 2, characterised in that the pulse-shaped tracking error signal (TZ), the pulse-shaped envelope signal (HP) as well as their inverse signals ($\overline{TZ}$, $\overline{HP}$) are fed to a direction determining logic circuit, in that the direction determining logic circuit emits a first signal which indicates that the light beam is crossing data tracks in one direction when an edge of the pulse-

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shaped envelope signal (HP) is always followed by an edge of opposite direction of the pulse-shaped tracking error signal (TZ), in that, conversely, the direction determining logic circuit emits a second signal, which indicates that the light beam is crossing data tracks in the other direction when an edge of the pulse-shaped tracking error signal (TZ) is always followed by a like edge of the pulse-shaped envelope signal (HP), and in that the direction determining logic circuit maintains the last emitted signal when the edges of the pulse-shaped envelope signal (HP) and of the pulse-shaped tracking error signal (TZ) no longer occur in an alternating sequence.

4. A method according to Claim 2 or 3, characterised in that the pulse-shaped tracking error signal (TZ), the pulse-shaped envelope signal (HP) as well as their inverse signals ($\overline{TZ}$, $\overline{HP}$) are fed to a detection circuit (Z) which outputs a counting pulse each time the light beam scanning the data stored on the recording medium crosses a data track.

5. A direction determining logic circuit for executing the method according to Claim 1, 2, 3 or 4, characterised in that the output of a first inverter (I1) is connected to the first input of a first AND gate (U1) and of a third AND gate (U3), that the input of the first inverter (I1), to which the pulse-shaped envelope signal (HP) is supplied, is connected to the first input of a second AND gate (U2) and of a fourth AND gate (U4), in that the output of a second inverter (I2) is connected to the second input of the second AND gate (U2) and of the third AND gate (U3), in that the input of the second inverter (I2), to which is supplied the pulse-shaped tracking error signal (TZ), is connected to the second input of the first AND gate (U1) and of the fourth AND gate (U4), in that the output of the first AND gate (U1) is connected to the set input of a first RS flip-flop (F1), the reset input of which is connected to the output of the

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second AND gate (U2), in that the output of the third AND gate (U3) is connected to the set input of a second RS flip-flop (F2), the reset input of which is connected to the output of the fourth AND-gate (U4), in that the Q-output of the first RS flip-flop (F1) is connected to the first input of a fifth AND gate (U6) and, via a first delay element (V1), to the clock input of a first D flip-flop (F3), the Q-output of which is connected to the first input of a sixth AND gate (U5), in that the $\overline{Q}$-output of the first RS flip-flop (F1) is connected to the reset input of the first D flip-flop (F3) and to the data input of the second D flip-flop (F4), the Q-output of which is connected to the second input of the fifth AND gate (U6), in that the Q-output of the second RS flip-flop (F2) is connected to the second input of the sixth AND gate (U5) and, via a second delay element (V2), to the clock input of the second D flip-flop (F4), the reset input of which is connected to the $\overline{Q}$-output of the second RS flip-flop (F2) and to the data input of the first D flip-flop (F3), in that the output of the sixth AND gate (U5) is connected to the set input of the third RS flip-flop (F5), the reset input of which is connected to the output of the fifth AND gate (U6), in that the first input of a seventh AND gate (U7) is connected to the Q-output of the third RS flip-flop (F5), in that the $\overline{Q}$-output of the third RS flip-flop (F5) is connected to the first input of an eighth AND gate (U8), in that the second input of the seventh and eighth AND gate (U7, U8) is connected to the detection circuit (Z), which emits a logical one when the light beam leaves a track, so that the seventh AND gate (U7) emits a counting pulse when the light beam crosses a data track in one direction, and in that the eighth AND gate (U8) emits a counting pulse when the light beam crosses a data track in the opposite direction.

6. A detection circuit for a direction determining logic circuit according to Claim 5, characterised in that the

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pulse-shaped envelope signal (HP) is fed to the input of a first monoflop (M1) triggerable by a descending edge, in that the pulse-shaped tracking error signal (TZ) is fed to a second monoflop (M2) triggerable by a descending edge and to the first input of a first OR gate (01), in that the inverted pulse-shaped tracking error signal ($\overline{TZ}$) is fed to a third monoflop (M3) triggerable by an ascending edge and to the first input of a second OR gate (02), in that the output of the first monoflop (M1) is connected to the first input of a ninth AND gate (U9), the second input of which is connected to the output of a tenth AND gate (U10), in that the output of the second and third monoflops (M2, M3) is respectively connected to an input of a third OR gate (03), in that the output of the first and second OR gate (01, 02) is respectively connected to an input of the tenth AND gate (U10), in that the output of the ninth AND gate (U9) is connected to the set input and the output of the third OR gate (03) to the reset input of a fourth RS flip-flop (F6), the Q-output of which is connected to the second input of the seventh and eighth AND gate (U7, U8) of the direction determining logic circuit, in that the output of the eighth AND gate (U8) is connected to the second input of the second OR gate (02), and in that the output of the seventh AND gate (U7) is connected to the second input of the first OR gate (01).

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