FIG. 1

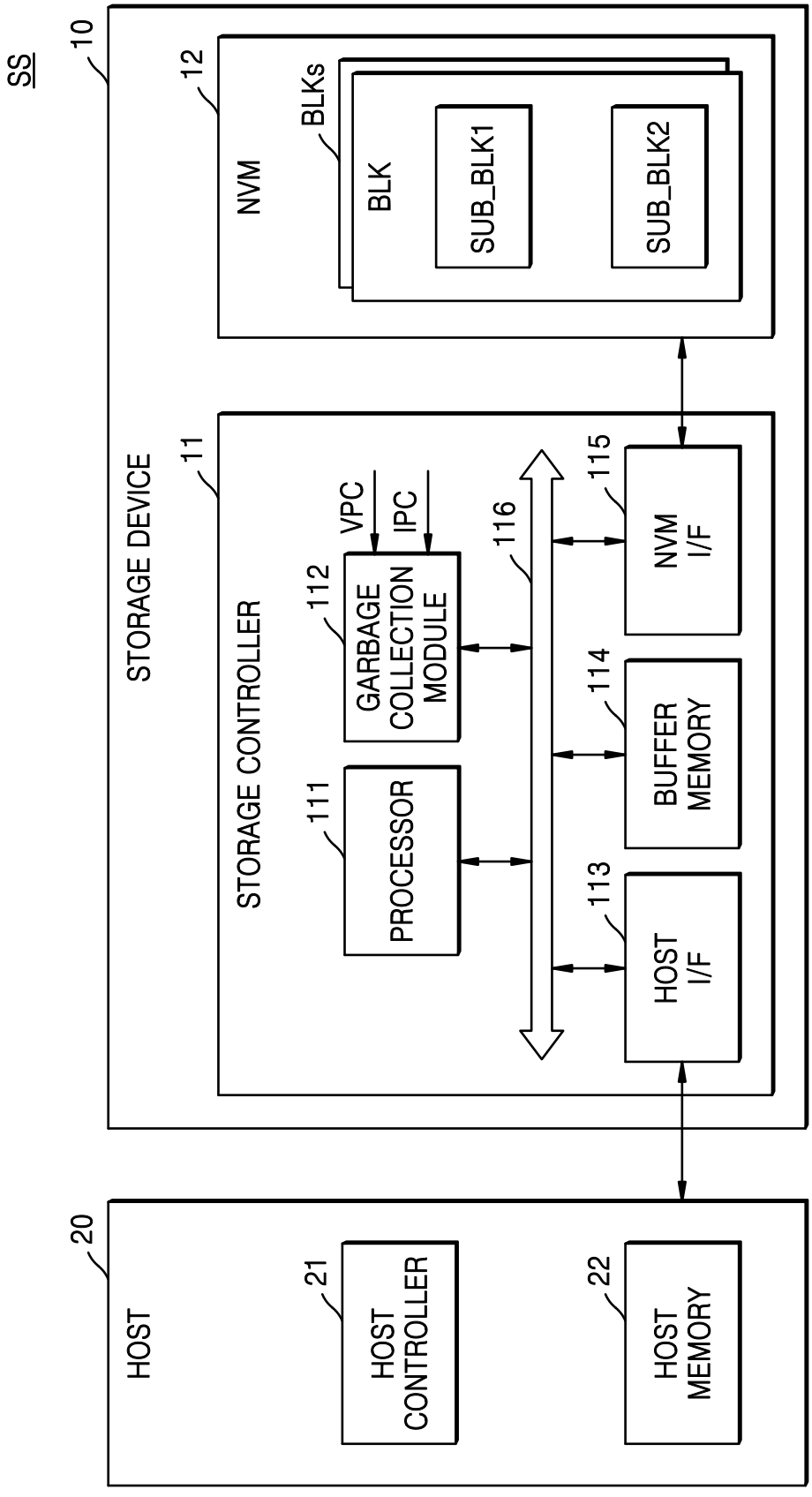

SS
10
STORAGE DEVICE
12
NVM
BLKs
BLK
SUB_BLK1
SUB_BLK2
11
STORAGE CONTROLLER
VPC
IPC
112
GARBAGE COLLECTION MODULE
111
PROCESSOR
116
115
NVM I/F
114
BUFFER MEMORY
113
HOST I/F
20
HOST
21
HOST CONTROLLER
22
HOST MEMORY

FIG. 2

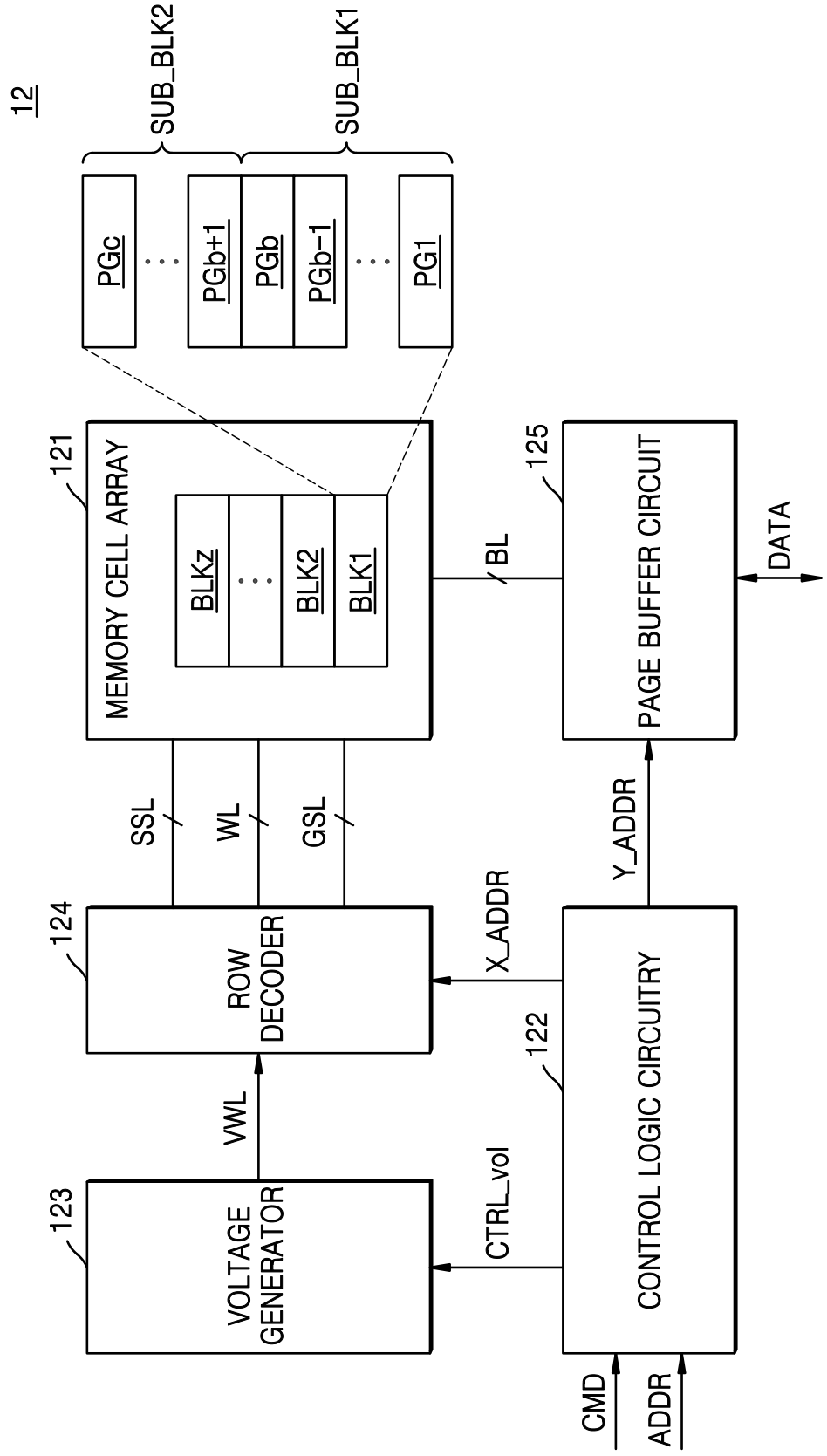

12
SUB_BLK2
SUB_BLK1
PGc
PGb+1
PGb
PGb-1
PG1
121
MEMORY CELL ARRAY
BLKz
BLK2
BLK1
BL
125
PAGE BUFFER CIRCUIT
DATA
SSL
WL
GSL
124
ROW DECODER
X_ADDR
Y_ADDR
VWL
123
VOLTAGE GENERATOR
CTRL_vol
122
CONTROL LOGIC CIRCUITRY
CMD
ADDR

FIG. 3

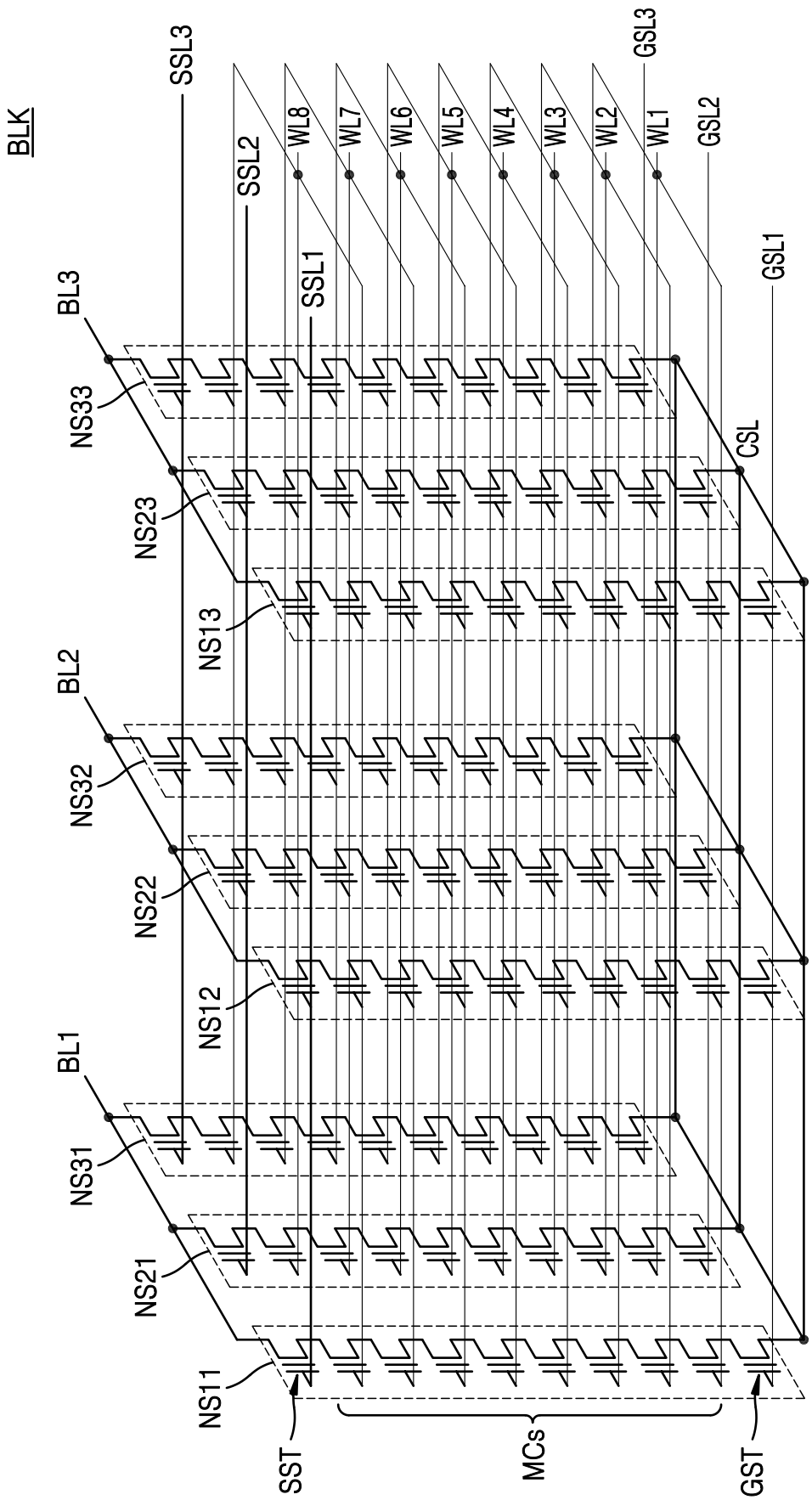

BLK
SSL3
SSL2
SSL1
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL3
GSL2
GSL1
CSL
BL3
BL2
BL1
NS33
NS23
NS13
NS32
NS22
NS12
NS31
NS21
NS11
SST
MCs
GST

FIG. 4A

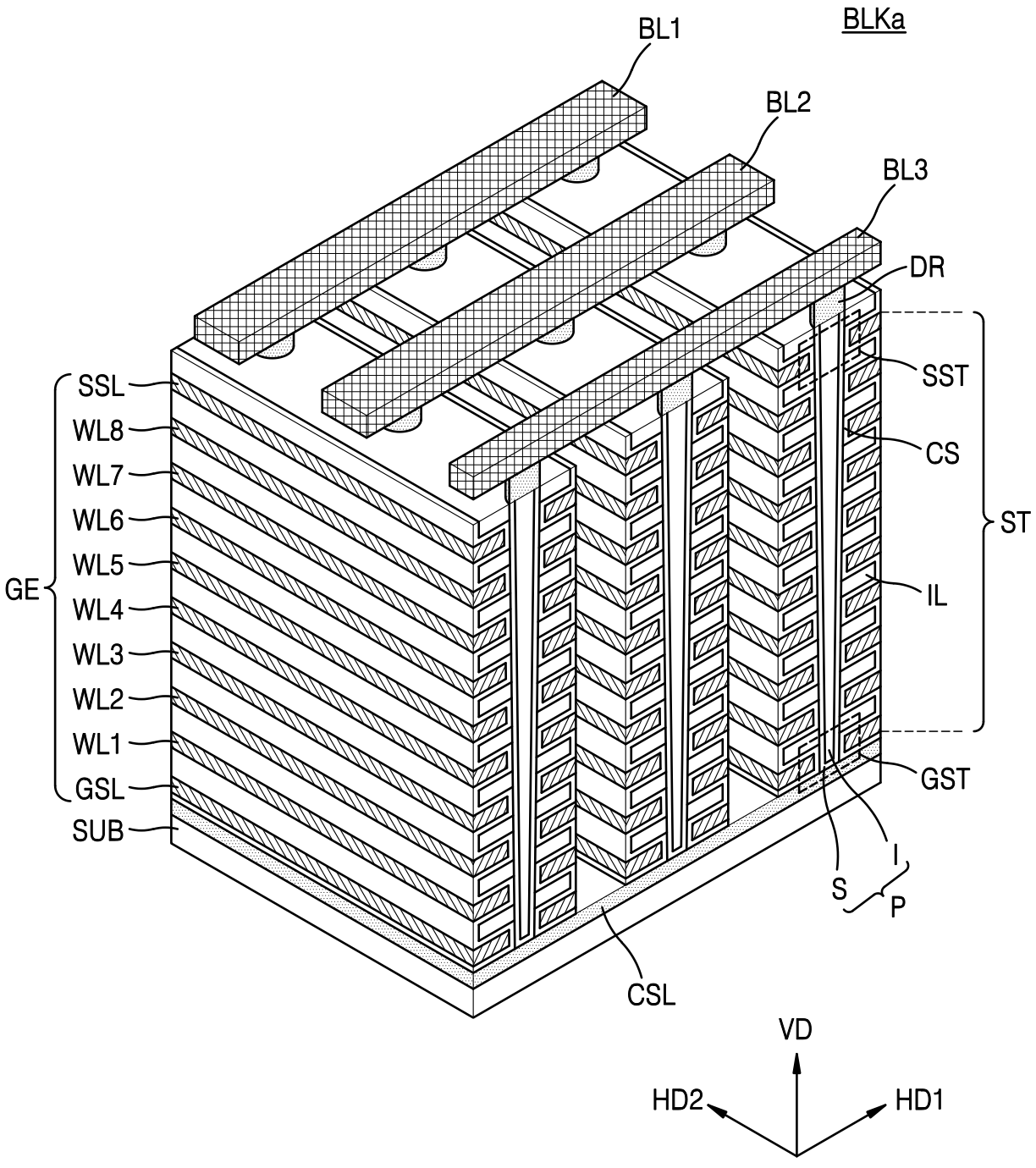

BLKa
BL1
BL2
BL3
DR
SST
CS
ST
IL
GST
I
S
P
CSL
SSL
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL
SUB
GE
VD
HD2
HD1

FIG. 4B

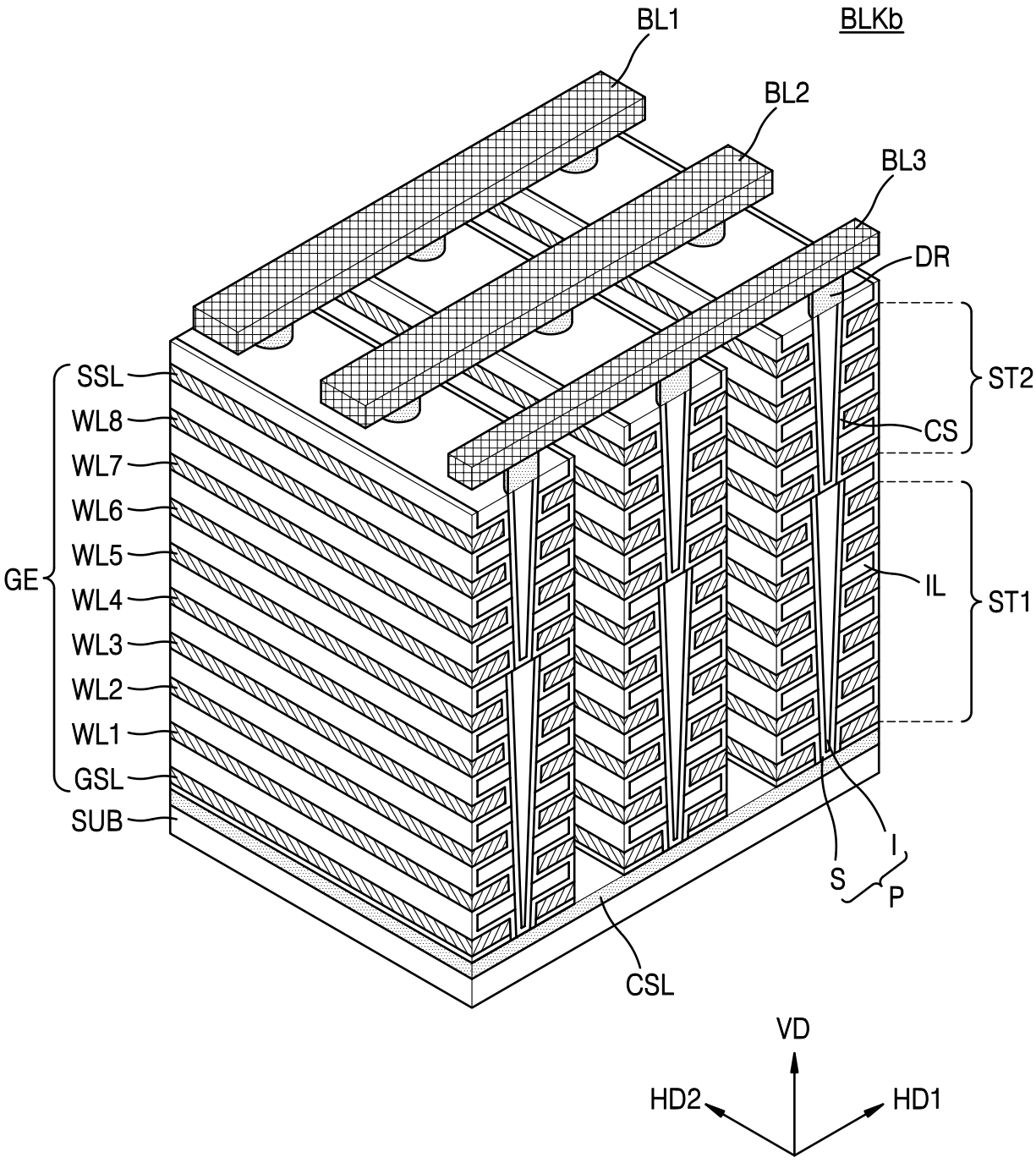

BL1
BLKb
BL2
BL3
DR
SSL
WL8
WL7
WL6
WL5
WL4
WL3
WL2
WL1
GSL
SUB
GE
ST2
CS
IL
ST1
I
S
P
CSL
VD
HD2
HD1

FIG. 5

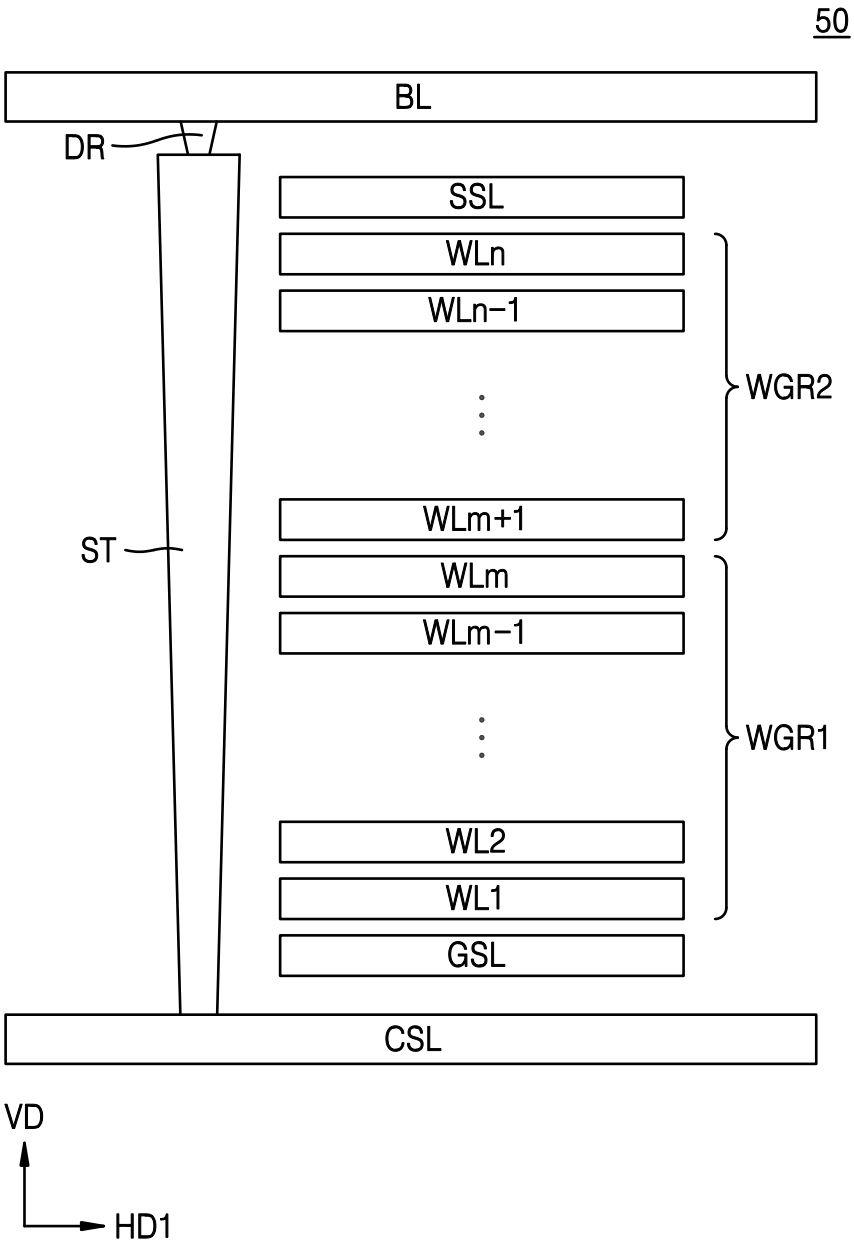

50
BL
DR
SSL
WLn
WLn-1
WGR2
WLm+1
ST
WLm
WLm-1
WGR1
WL2
WL1
GSL
CSL
VD
HD1

FIG. 6

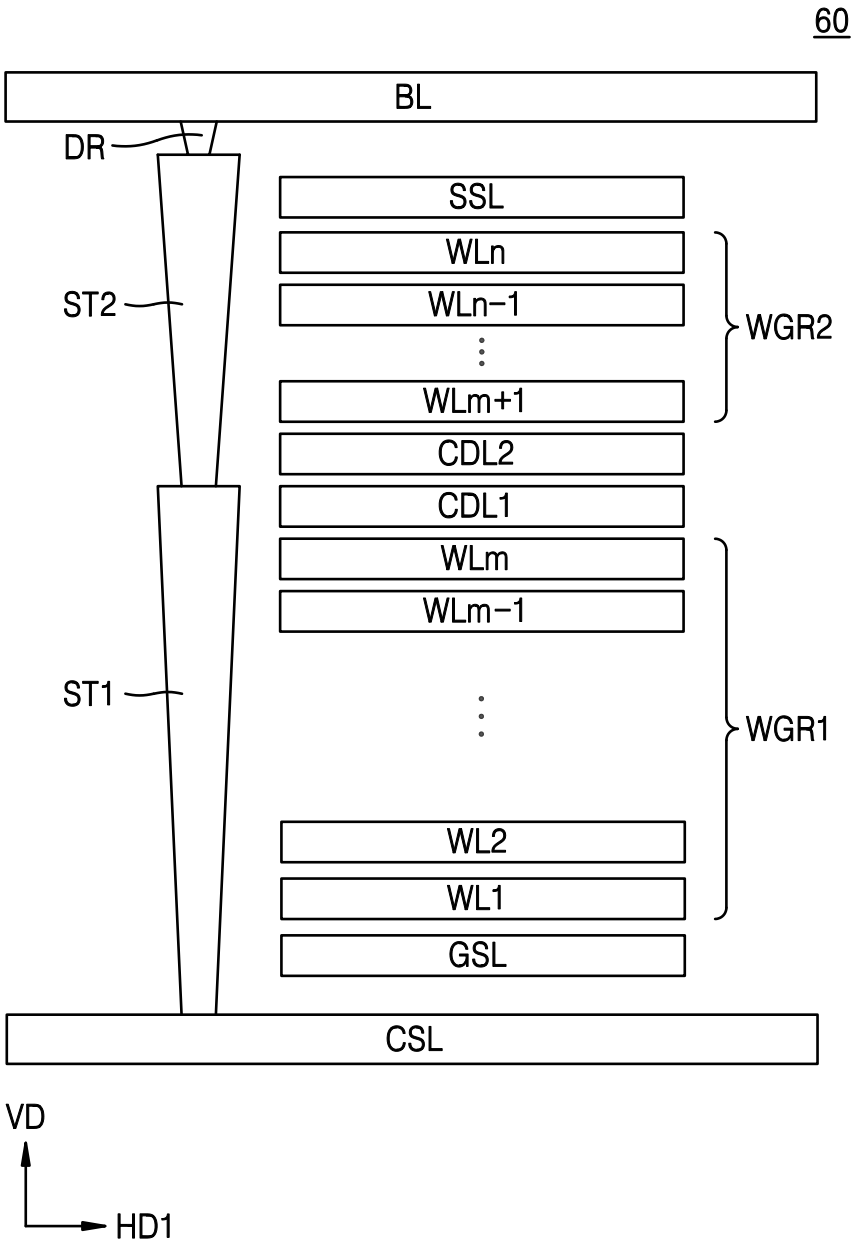

60
BL
DR
SSL
WLn
WLn-1
WGR2
ST2
WLm+1
CDL2
CDL1
WLm
WLm-1
ST1
WGR1
WL2
WL1
GSL
CSL
VD
HD1

FIG. 7

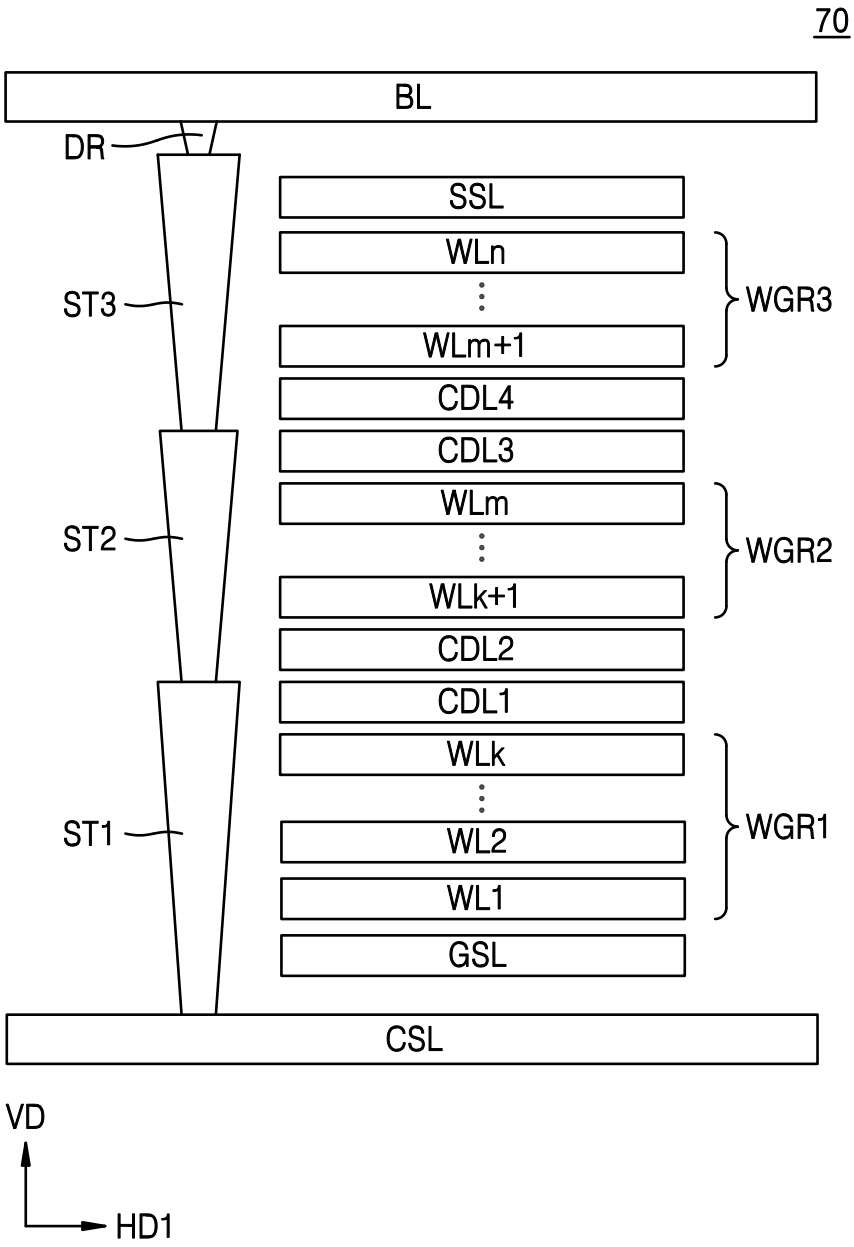

70
BL
DR
SSL
WLn
WLm+1
WGR3
ST3
CDL4
CDL3
WLm
WLk+1
WGR2
ST2
CDL2
CDL1
WLk
WL2
WL1
WGR1
ST1
GSL
CSL
VD
HD1

FIG. 8

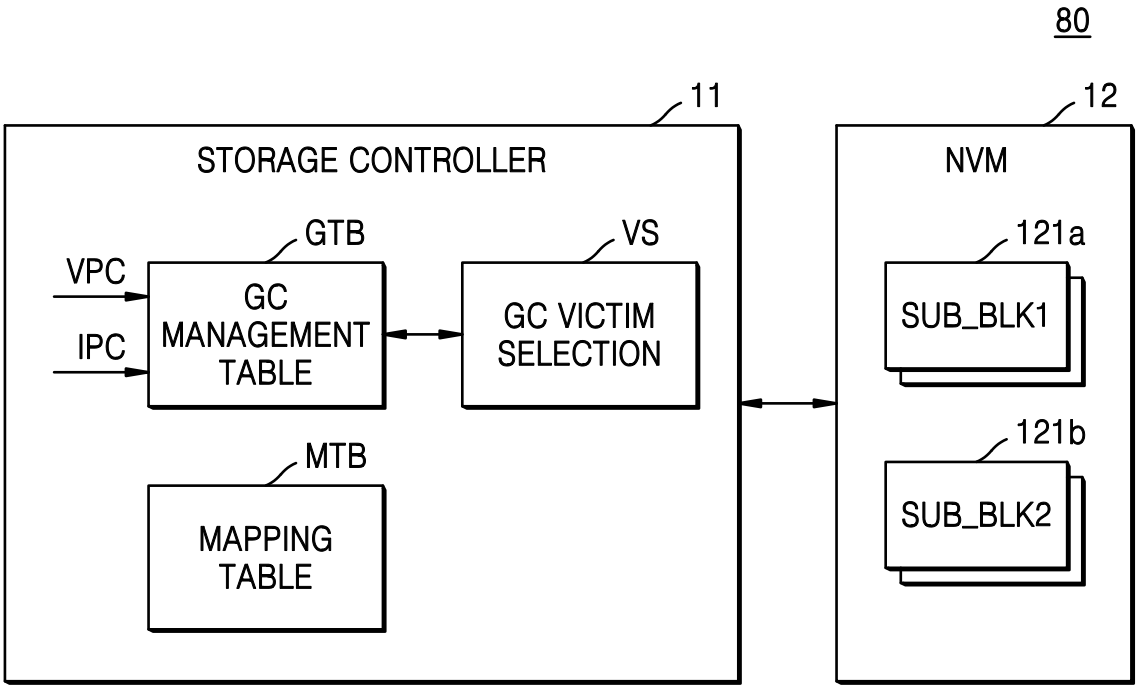

80
11
STORAGE CONTROLLER
GTB
VS
VPC
IPC
GC MANAGEMENT TABLE
GC VICTIM SELECTION
MTB
MAPPING TABLE
12
NVM
121a
SUB_BLK1
121b
SUB_BLK2

FIG. 9

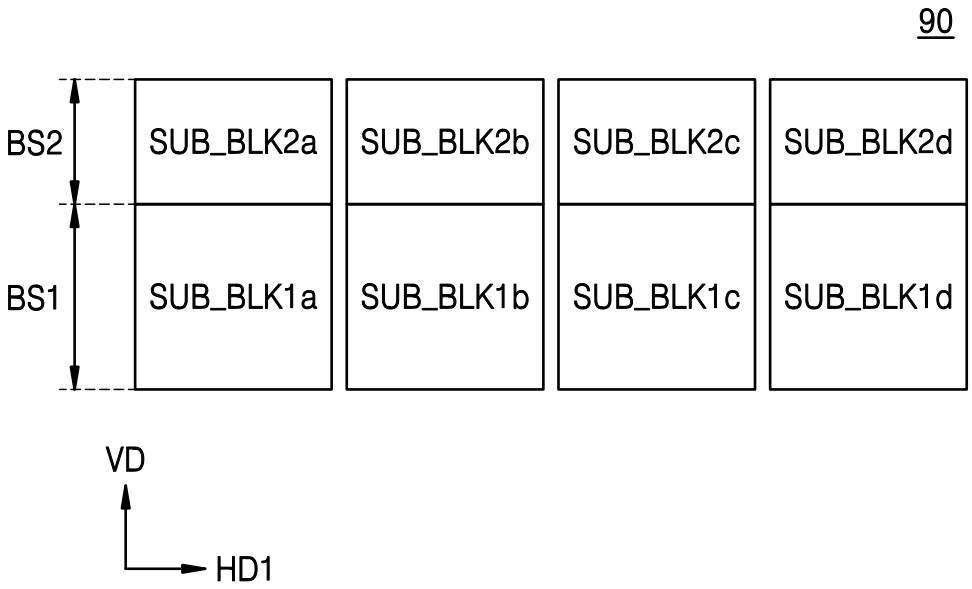

90
BS2
BS1
SUB_BLK2a
SUB_BLK2b
SUB_BLK2c
SUB_BLK2d
SUB_BLK1a
SUB_BLK1b
SUB_BLK1c
SUB_BLK1d
VD
HD1

FIG. 10

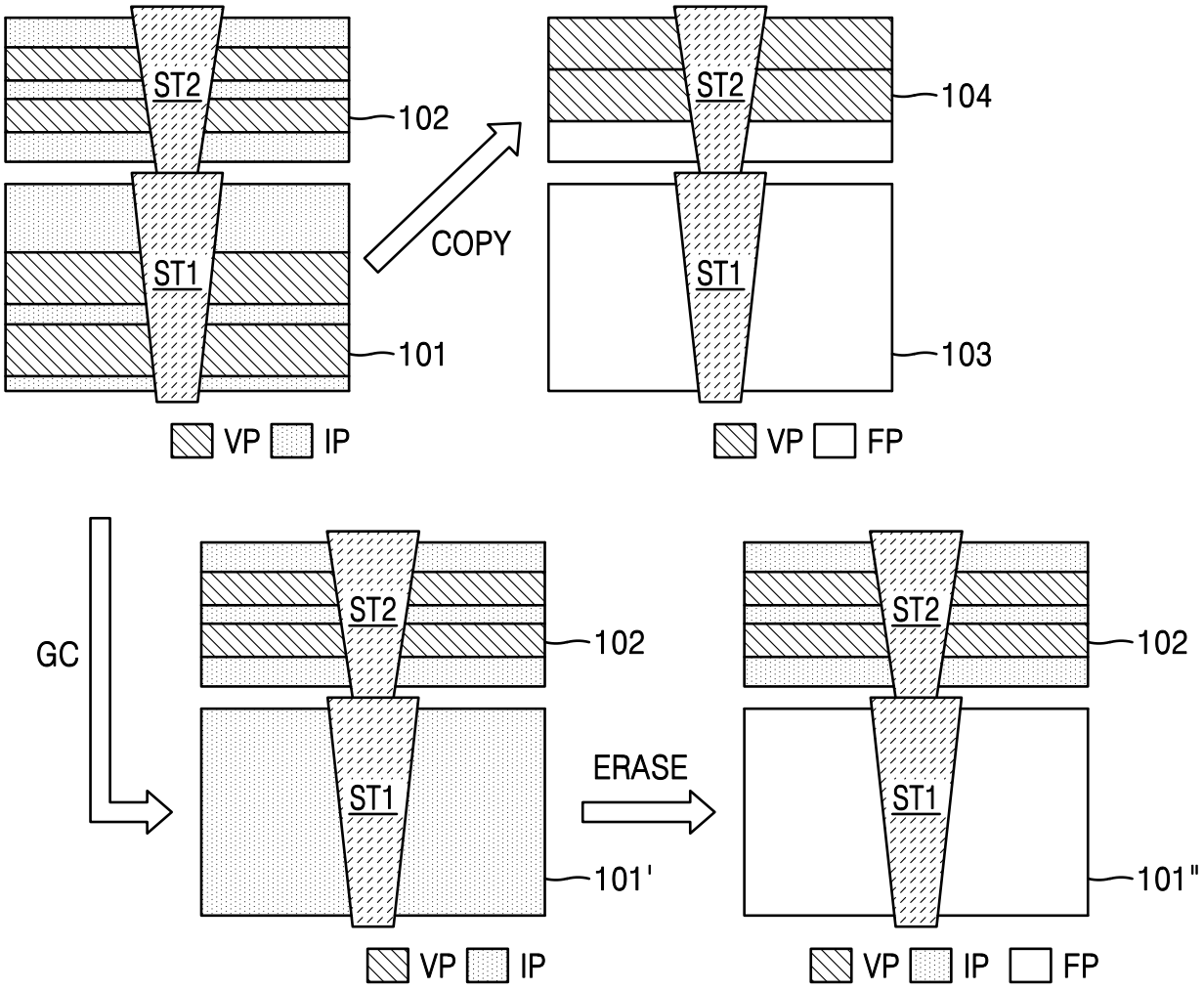

ST2
102
ST1
101
COPY
ST2
104
ST1
103
VP
IP
VP
FP
GC
ST2
102
ST1
101'
ERASE
ST2
102
ST1
101"
VP
IP
VP
IP
FP

FIG. 11A

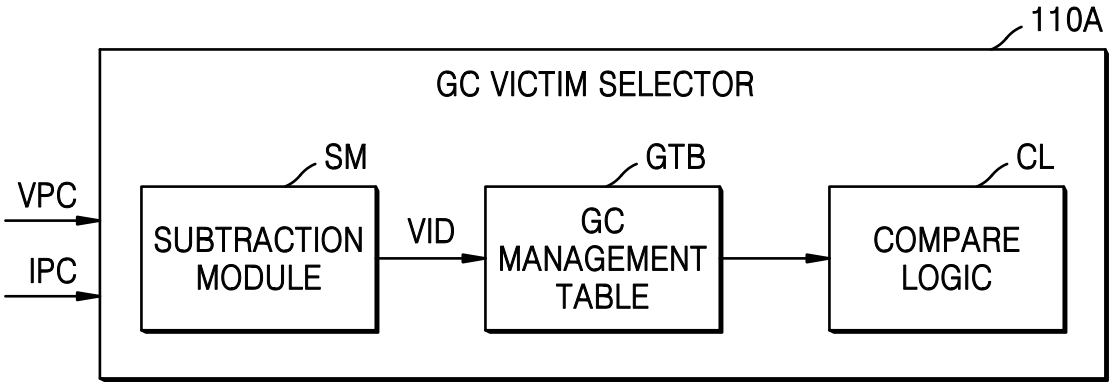

110A
GC VICTIM SELECTOR
SM
GTB
CL
VPC
IPC
SUBTRACTION MODULE
VID
GC MANAGEMENT TABLE
COMPARE LOGIC

FIG. 11B

110B

	SUB_BLK1	SUB_BLK2
VPC	VPCa	VPCb
IPC	IPCa	IPCb
VID	VIDa	VIDb

FIG. 12A

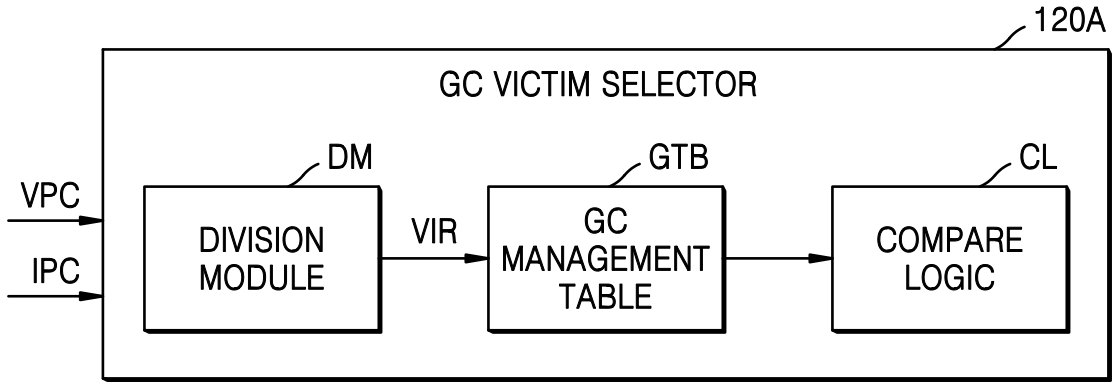

120A
GC VICTIM SELECTOR
DM
GTB
CL
VPC
IPC
DIVISION MODULE
VIR
GC MANAGEMENT TABLE
COMPARE LOGIC

FIG. 12B

120B

	SUB_BLK1	SUB_BLK2
VPC	VPCa	VPCb
IPC	IPCa	IPCb
VIR	VIRa	VIRb

FIG. 13A

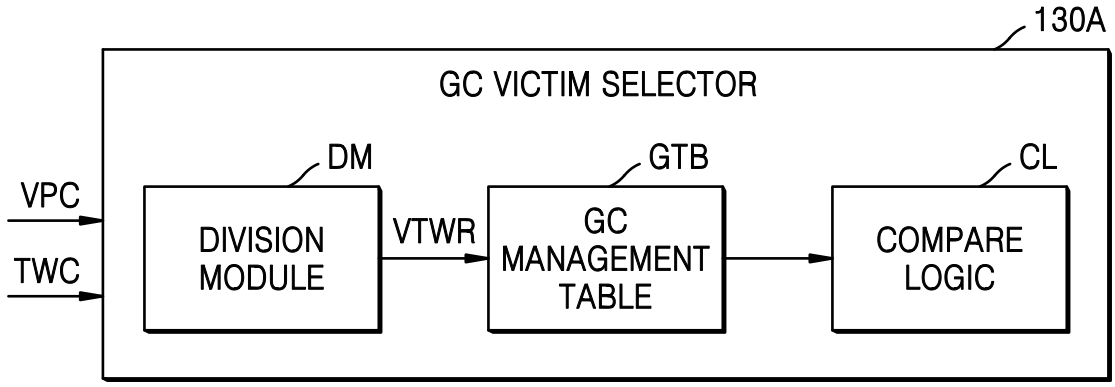

130A
GC VICTIM SELECTOR
DM
GTB
CL
VPC
TWC
DIVISION MODULE
VTWR
GC MANAGEMENT TABLE
COMPARE LOGIC

FIG. 13B

130B

	SUB_BLK1	SUB_BLK2
VPC	VPCa	VPCb
TWC	TWCa	TWCb
VTWR	VTWRa	VTWRb

FIG. 14A

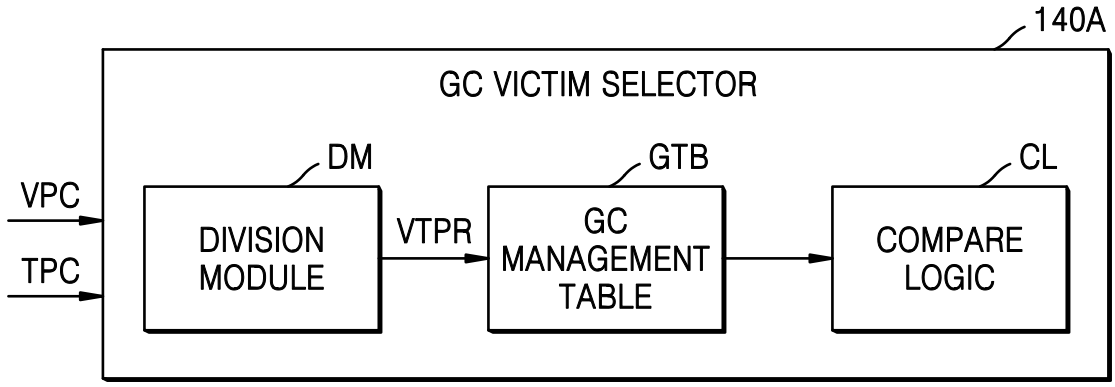

140A
GC VICTIM SELECTOR
DM
GTB
CL
VPC
TPC
DIVISION MODULE
VTPR
GC MANAGEMENT TABLE
COMPARE LOGIC

FIG. 14B

140B

	SUB_BLK1	SUB_BLK2
VPC	VPCa	VPCb
TPC	TPCa	TPCb
VTPR	VTPRa	VTPRb

FIG. 15

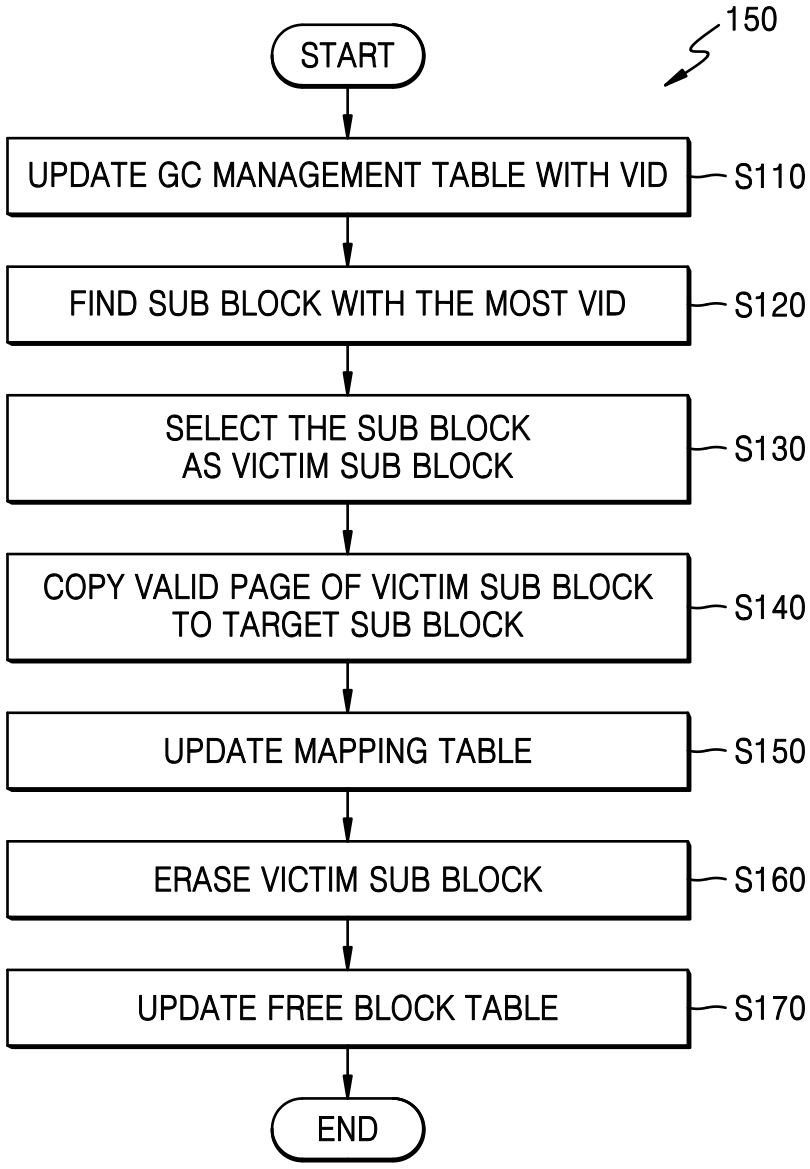

150
START
UPDATE GC MANAGEMENT TABLE WITH VID
S110
FIND SUB BLOCK WITH THE MOST VID
S120
SELECT THE SUB BLOCK AS VICTIM SUB BLOCK
S130
COPY VALID PAGE OF VICTIM SUB BLOCK TO TARGET SUB BLOCK
S140
UPDATE MAPPING TABLE
S150
ERASE VICTIM SUB BLOCK
S160
UPDATE FREE BLOCK TABLE
S170
END

FIG. 16

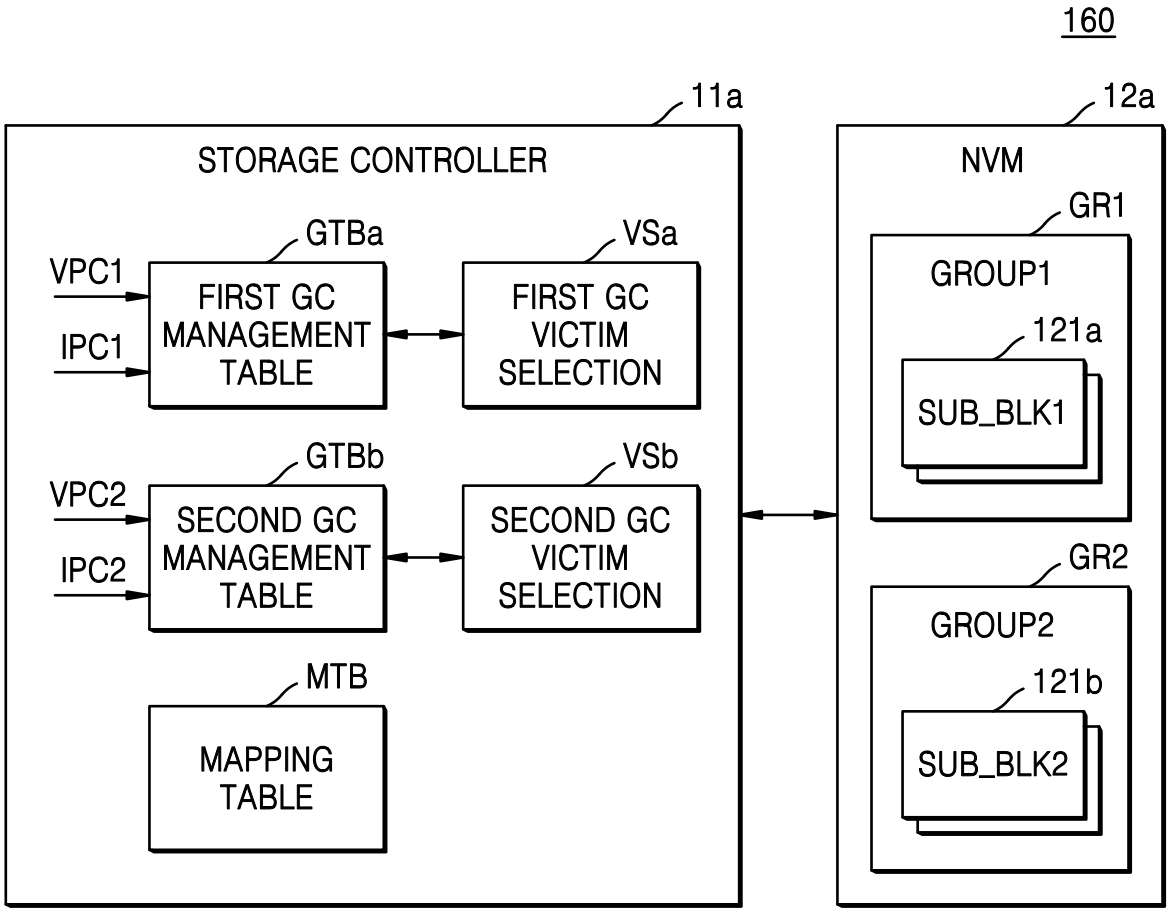

160
11a
STORAGE CONTROLLER
GTBa
VPC1
IPC1
FIRST GC MANAGEMENT TABLE
VSa
FIRST GC VICTIM SELECTION
GTBb
VPC2
IPC2
SECOND GC MANAGEMENT TABLE
VSb
SECOND GC VICTIM SELECTION
MTB
MAPPING TABLE
12a
NVM
GR1
GROUP1
121a
SUB_BLK1
GR2
GROUP2
121b
SUB_BLK2

FIG. 17

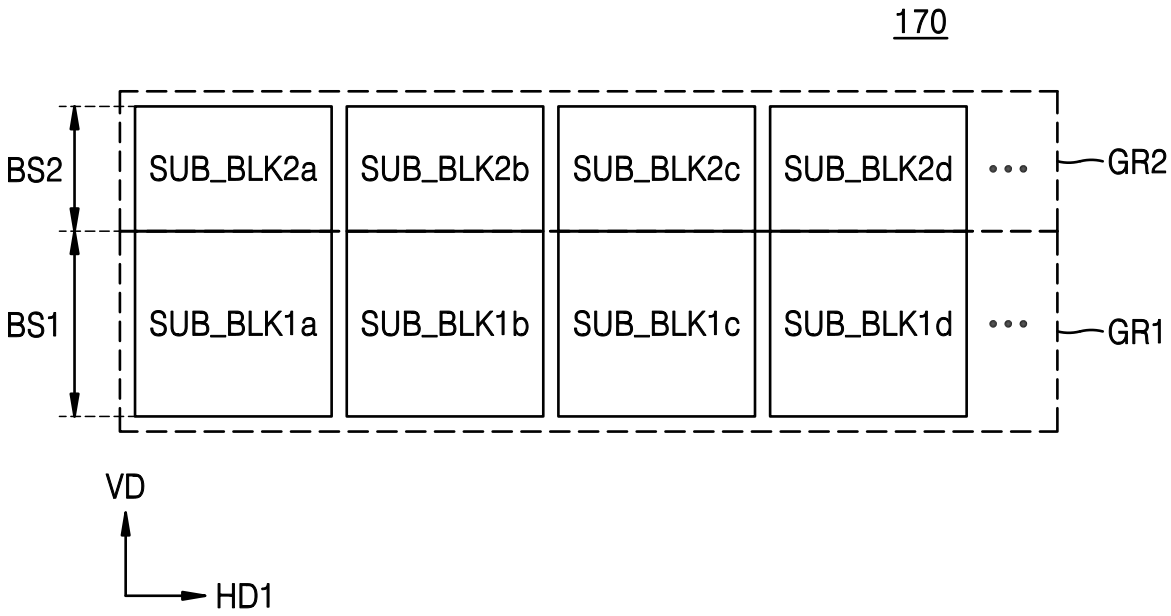

170
BS2
BS1
SUB_BLK2a
SUB_BLK2b
SUB_BLK2c
SUB_BLK2d
SUB_BLK1a
SUB_BLK1b
SUB_BLK1c
SUB_BLK1d
GR2
GR1
VD
HD1

FIG. 18

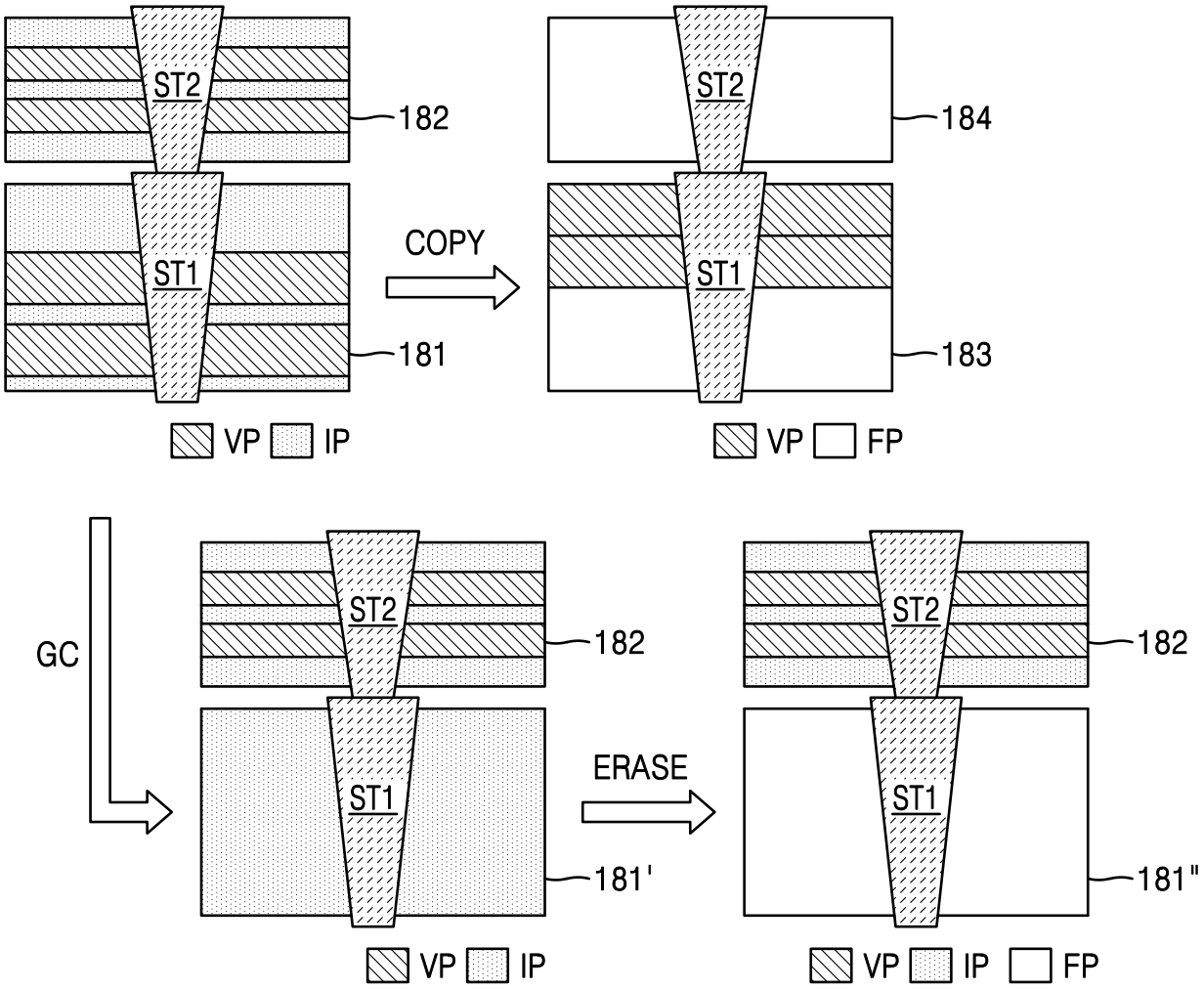

ST2
182
ST1
181
COPY
ST2
184
ST1
183
VP
IP
VP
FP
GC
ST2
182
ST1
181'
ERASE
ST2
182
ST1
181"
VP
IP
VP
IP
FP

FIG. 19A

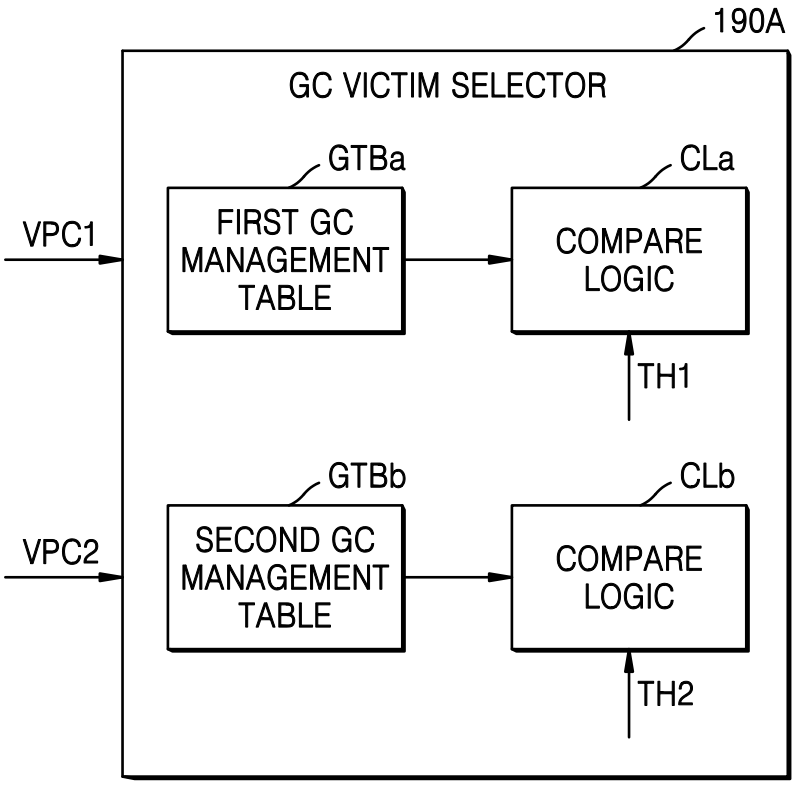

190A
GC VICTIM SELECTOR
GTBa
CLa
VPC1
FIRST GC MANAGEMENT TABLE
COMPARE LOGIC
TH1
GTBb
CLb
VPC2
SECOND GC MANAGEMENT TABLE
COMPARE LOGIC
TH2

FIG. 19B

190B

GROUP1	VPC
SUB_BLK1a	VPC1a
SUB_BLK1b	VPC1b
…	…

190C

GROUP2	VPC
SUB_BLK2a	VPC2a
SUB_BLK2b	VPC2b
…	…

FIG. 20A

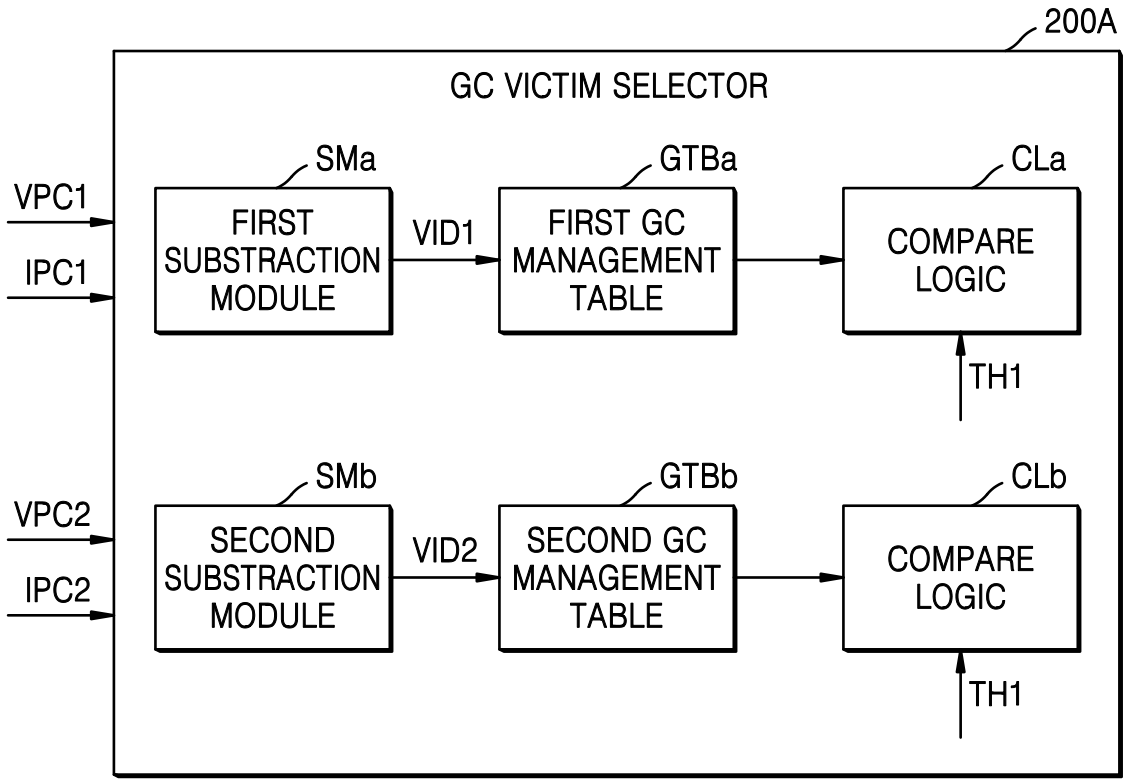

200A
GC VICTIM SELECTOR
VPC1
IPC1
SMa
FIRST SUBSTRACTION MODULE
VID1
GTBa
FIRST GC MANAGEMENT TABLE
CLa
COMPARE LOGIC
TH1
VPC2
IPC2
SMb
SECOND SUBSTRACTION MODULE
VID2
GTBb
SECOND GC MANAGEMENT TABLE
CLb
COMPARE LOGIC
TH1

FIG. 20B

200B

GROUP1	VPC	IPC	VID
SUB_BLK1a	VPC1a	IPC1a	VID1a
SUB_BLK1b	VPC1b	IPC1b	VID1b
…	…	…	…

200C

GROUP2	VPC	IPC	VID
SUB_BLK2a	VPC2a	IPC2a	VID2a
SUB_BLK2b	VPC2b	IPC2b	VID2b
…	…	…	…

FIG. 21

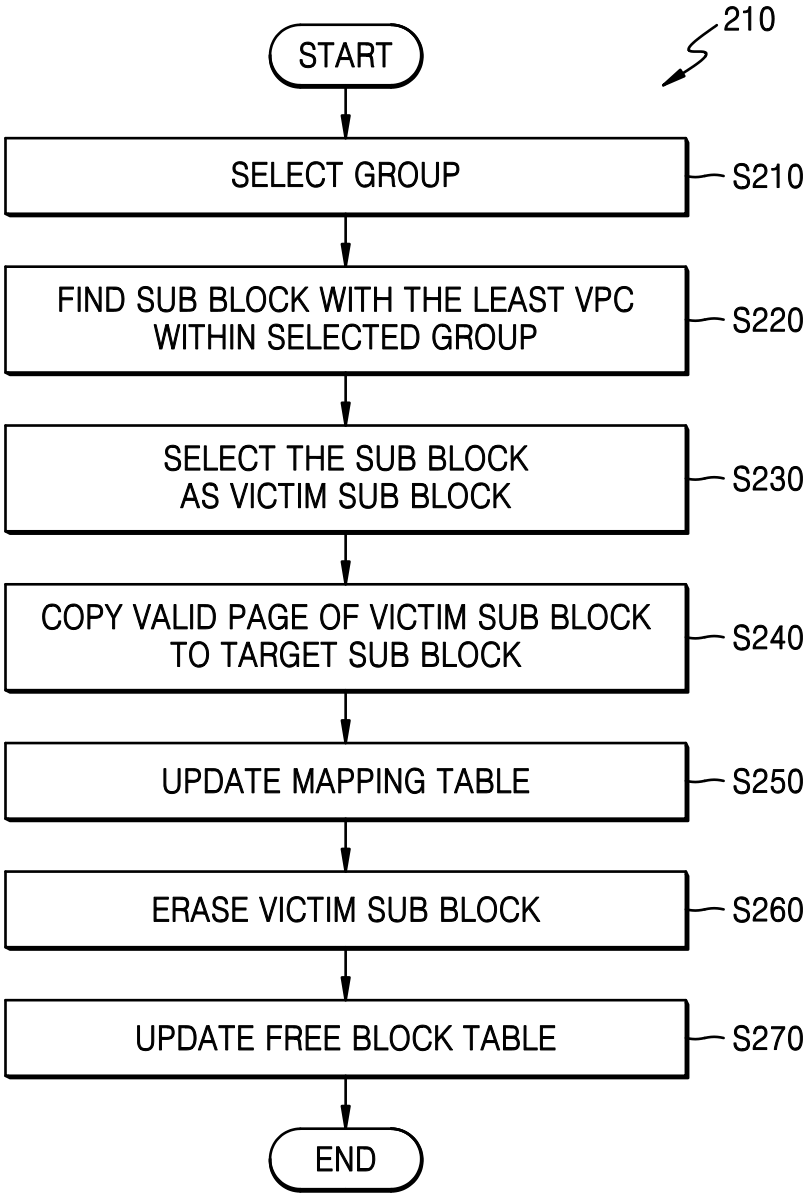
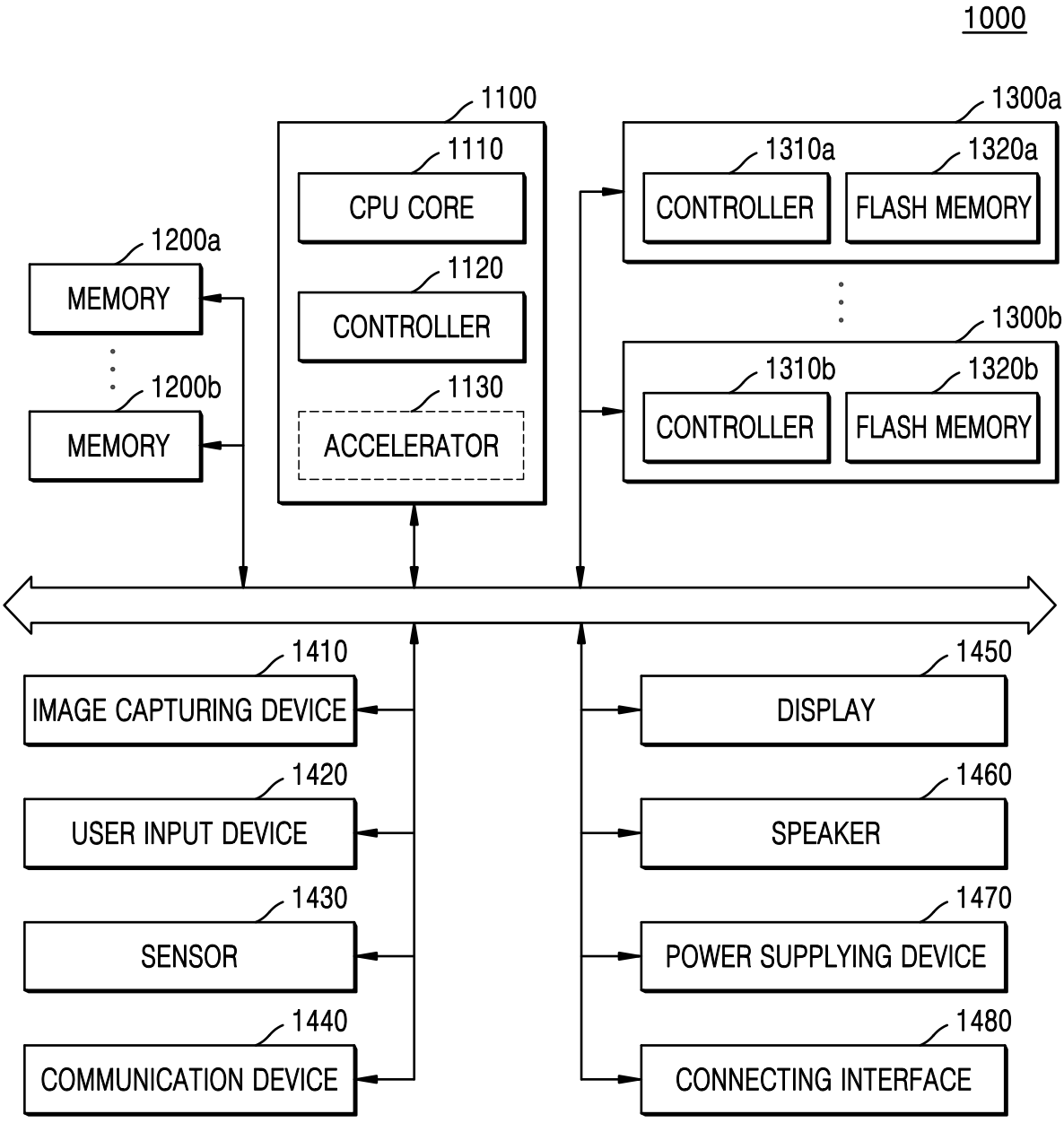

210
START
SELECT GROUP
S210
FIND SUB BLOCK WITH THE LEAST VPC WITHIN SELECTED GROUP
S220
SELECT THE SUB BLOCK AS VICTIM SUB BLOCK
S230
COPY VALID PAGE OF VICTIM SUB BLOCK TO TARGET SUB BLOCK
S240
UPDATE MAPPING TABLE
S250
ERASE VICTIM SUB BLOCK
S260
UPDATE FREE BLOCK TABLE
S270
END

FIG. 22


1000
1100
1110
CPU CORE
1120
CONTROLLER
1130
ACCELERATOR
1200a
MEMORY
1200b
MEMORY
1300a
1310a
CONTROLLER
1320a
FLASH MEMORY
1300b
1310b
CONTROLLER
1320b
FLASH MEMORY
1410
IMAGE CAPTURING DEVICE
1420
USER INPUT DEVICE
1430
SENSOR
1440
COMMUNICATION DEVICE
1450
DISPLAY
1460
SPEAKER
1470
POWER SUPPLYING DEVICE
1480
CONNECTING INTERFACE