ABSTRACT

A memory, a manufacturing method thereof, and an electronic device. The memory includes a first semiconductor structure and a second semiconductor structure coupled to each other. The first semiconductor structure includes a plurality of memory arrays arranged in an array and spaced apart from each other, each memory array includes memory cells, each memory cell includes a vertical transistor and a capacitor, the capacitor includes a first electrode coupled to the vertical transistor and a second electrode opposite to the first electrode; the second semiconductor structure includes a peripheral circuit and is disposed on a side of the vertical transistor away from the capacitor; the first semiconductor structure further includes a common electrode electrically connected to the second electrodes of the capacitors in the memory arrays and a common electrode contact plug, and the common electrode is coupled to the peripheral circuit through the common electrode contact plug.

[FIG. 3a]