(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 June 2000 (15.06.2000)

PCT

(10) International Publication Number
WO 00/34999 A3

(51) International Patent Classification[7]: H01L 21/322, 21/00, 21/205, C30B 25/10

(21) International Application Number: PCT/US99/27359

(22) International Filing Date:
18 November 1999 (18.11.1999)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/111,546 9 December 1998 (09.12.1998) US
09/250,908 16 February 1999 (16.02.1999) US

(71) Applicant *(for all designated States except US)*: MEMC ELECTRONIC MATERIALS, INC. [US/US]; 501 Pearl Drive, P.O. Box 8, St. Peters, MO 63376 (US).

(71) Applicants and
(72) Inventors: WILSON, Gregory, M. [—/US]; MEMC Electronic Materials, Inc., 501 Pearl Drive, P.O. Box 8, St. Peters, MO 63376 (US). ROSSI, Jon, A. [—/US]; MEMC Electronic Materials, Inc., 501 Pearl Drive, P.O. Box 8, St. Peters, MO 63376 (US). YANG, Charles, C. [—/US]; MEMC Electronic Materials, Inc., 501 Pearl Drive, P.O. Box 8, St. Peters, MO 63376 (US).

(74) Agents: HEJLEK, Edward, J. et al.; Senniger, Powers, Leavitt & Roedel, 16th floor, One Metropolitan Square, St. Louis, MO 63102 (US).

(81) Designated States *(national)*: CN, JP, KR, SG, US.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*

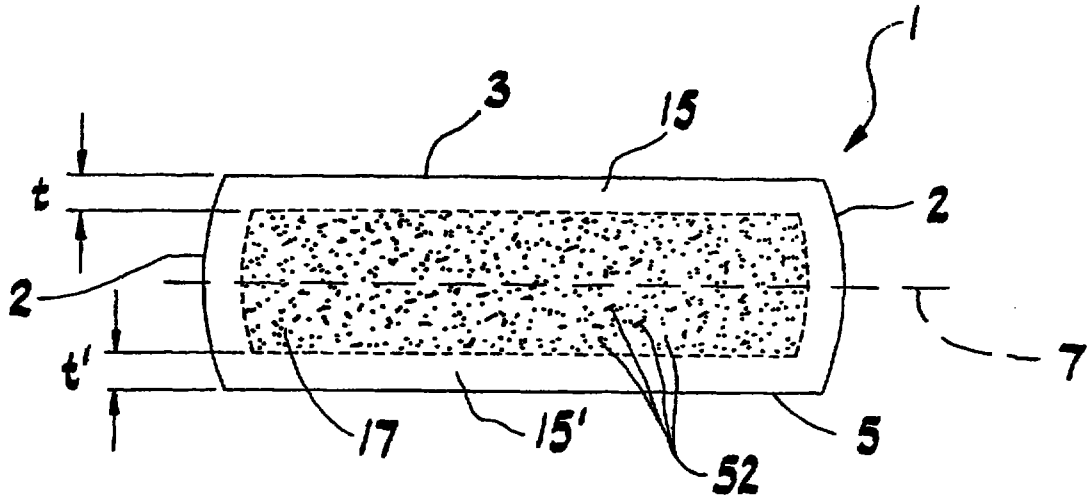
(88) Date of publication of the international search report:
16 November 2000

(48) Date of publication of this corrected version:
19 April 2001

(15) Information about Correction:
see PCT Gazette No. 16/2001 of 19 April 2001, Section II

[Continued on next page]

(54) Title: AN EPITAXIAL SILICON WAFER WITH INTRINSIC GETTERING AND A METHOD FOR THE PREPARATION THEREOF



(57) Abstract: This invention is directed to a novel process for the preparation of a silicon wafer comprising a surface having an epitaxial layer deposited thereon. In one embodiment, the process comprising heating a surface of a wafer starting material to remove a silicon oxide layer from the surface. Within about 30 seconds after removing the silicon oxide layer from the surface, the surface is exposed to an atmosphere comprising silicon to deposit a silicon epitaxial layer onto the surface to form an epitaxial wafer. The epitaxial wafer is then heated to a soak temperature of at least about 1175 °C while exposing the epitaxial layer to an oxidizing atmosphere comprising an oxidant. Afterwards, the heated epitaxial wafer is cooled at a rate of at least about 10 °C/sec.

WO 00/34999 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.