

ABSTRACT

Disclosed are semiconductor devices and fabrication methods thereof. The semiconductor device includes a substrate including first and second regions, a device isolation pattern in the substrate, a lower separation dielectric pattern on the first region of the substrate, first channel patterns on the lower separation dielectric pattern, a first gate electrode on the first channel patterns and including a first gate part between the lower separation dielectric pattern and a lowermost first channel pattern, and first source/drain patterns on opposite sides of the first gate electrode and in contact with lateral surfaces of the first channel patterns. A bottom surface of the lower separation dielectric pattern is at a level higher than or equal to that of a bottom surface of the device isolation pattern. A top end of the lower separation dielectric pattern is at a level higher than that of a bottom surface of the first gate part.

FIG. 2A