

A FEEDBACK ARRANGEMENT IN A DEFLECTION CIRCUIT

The invention relates to a deflection circuit output stage of a cathode ray tube (CRT) in a television receiver or other such display device. In particular, the invention relates to a feedback network in a horizontal deflection circuit output stage in which a switching output transistor, operating in a switching mode, produces a deflection current in a horizontal deflection winding of the CRT.

A typical horizontal deflection circuit that is used in various color television receivers includes a driver or drive stage having a transformer coupled to a control terminal of the output transistor of the deflection circuit output stage. The driver stage further includes a second switching transistor having a collector electrode that is coupled to a primary winding of the transformer. When the switching transistor of the driver stage is conductive, magnetic energy is stored in the inductance of the primary winding. At the same time, a transformer coupled voltage developed across a secondary winding of the transformer causes the switching output transistor of the output stage, driven by the voltage developed in the secondary winding of the transformer, to be non-conductive. When the second switching transistor of the driver stage becomes non-conductive, the stored magnetic energy in the coupling transformer produces, in a flyback manner, a winding current that flows in the secondary winding of the coupling transformer to form a forward base current. The forward base current drives the deflection output transistor into saturation prior to the beginning time of the upramping collector current in the output transistor.

In one prior art circuit, the transformer has a winding that is coupled in a current path of the collector current of the switching output transistor. In the second half of trace, the collector current in the output transistor increases in an upramping manner. The upramping collector current is coupled via the transformer to the base of the output transistor, in a positive feedback manner. The result is that an upramping base current is generated.

In such prior art circuit, the deflection circuit might operate in an abnormal stable state, should the value of the

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Description : paged 1 to paged 7
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 Description : paged 1 to paged 7
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JONATHAN CHEN

current gain parameter, h_{FE} , of the output transistor be greater than, for example, 6. In the abnormal stable state, the peak amplitude of the collector current is larger than in normal steady state operating condition, in alternate trace intervals, and smaller than in normal steady state operation, in the other alternate trace intervals. It may be desirable to prevent such abnormal steady state operation.

A television deflection apparatus, embodying an aspect of the invention, includes a deflection winding coupled to a retrace capacitance to form a retrace resonant circuit, during a retrace interval of a deflection cycle. A first switching transistor is responsive to a control signal at a frequency that is related to a deflection frequency developed at a control terminal of the transistor. The transistor has a main current conducting terminal that is coupled to the retrace resonant circuit for generating a deflection current in the deflection winding. During a portion of a trace interval of the deflection cycle, at least a portion of the deflection current flows in the main current conducting terminal. A transformer has a first winding that is coupled to the control terminal of the first switching transistor and a second winding responsive to a signal produced by the first switching transistor. The transformer develops a ramping portion of the control signal in a positive feedback manner with respect to the current in the main current conducting terminal of the first switching transistor. A feedback network responsive to a signal produced by the first switching transistor develops a feedback signal that is applied to a control terminal of the first switching transistor in a negative feedback manner with respect to the current in the main current conducting terminal.

In accordance with an inventive feature, the feedback signal prevents the aforementioned abnormal steady state operation.

FIGURE 1 illustrates a horizontal deflection circuit output stage including a feedback network, embodying an aspect of the invention, coupled from a trace capacitor to a driver stage;

FIGURES 2a-2d illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1 in normal operation; and



FIGURES 3a-3e illustrate waveforms in abnormal steady state operation for a deflection such as in Figure 1 but without the feedback network of FIGURE 1.

FIGURE 1 illustrates a driver stage 100 for driving a switching output transistor Q2 of a horizontal deflection circuit output stage 101 of a television receiver, embodying an aspect of the invention. A conventional horizontal oscillator 102 produces an output signal V_{OSC} . Signal V_{OSC} is at a horizontal frequency of $2xf_H$ that is approximately 32 KHZ. Signal V_{OSC} is coupled via an emitter follower, not shown, to a base electrode of a driver transistor Q1. Frequency f_H , that is about 16 KHZ, is the horizontal deflection frequency in, for example, the NTSC standard. Thus, frequency $2xf_H$ is substantially higher than 16 KHZ.

Oscillator 102 is controlled by an on/off control signal. Signal on/off causes transistor Q1 to be turned on when signal on/off is at the "OFF" state, throughout standby operation. A collector of transistor Q1 is coupled to one end terminal of a primary winding W1 of a coupling transformer T1. The other end terminal of winding W1 is bypassed to ground by a filter capacitor C1 and coupled via a current limiting resistor R1 to a source of supply voltage $V+$ such that resistor R1 and capacitor C1 form a ripple filter.

A secondary winding W2 of transformer T1 is coupled across a base-emitter junction of transistor Q2 and across a resistor R4. A junction terminal 101a that is coupled at a junction of winding W2, resistor R4 and the emitter of transistor Q2 is coupled to one end terminal of a winding W3 of transformer T1. The other end terminal of winding W3 is coupled to ground.

The collector of transistor Q2 is coupled in series with a diode D3 to a conventional damper diode D2 of a horizontal deflection circuit 103. Circuit 103 includes a horizontal deflection winding L_H , a retrace capacitor C4, a trace capacitor C_S , a linearity inductor LIN, and a linearity resistor R5 that are coupled in a well-known manner. Diode D3 prevents reverse collector current from flowing in transistor Q2 and in winding W2 or W3. A supply voltage $B+$ is coupled to circuit 103 via a winding T2a of a horizontal flyback transformer T2. During retrace, circuit 103 forms a retrace resonant circuit that includes capacitor C4,





winding L_H and winding L_{IN} . During trace, circuit 103 forms a trace resonant circuit that includes trace capacitor C_s and winding L_H . Voltages $B+$ and $V+$ are produced both in standby and in run mode operations.

5 FIGURES 2a-2d illustrate idealized or approximated waveforms useful for explaining the normal operation of the circuit of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2d indicate similar items or functions.

10 In operation, driver transistor Q1 of FIGURE 1 is conductive as a result of signal V_{OSC} of FIGURE 2a being positive until time t_1 of FIGURE 2a that causes transistor Q2 to be nonconductive. The magnetic energy supplied by a collector current I_{c1} of transistor Q1 is stored in winding W1 of FIGURE 1. When transistor Q1 is turned off, during interval t_1-t_3 of FIGURE
15 2a, the stored energy produces in winding W2 of FIGURE 1 a forward base current I_{b2} of transistor Q2. Current I_{b2} is sufficient to turn on deflection transistor Q2 and to maintain it in saturation prior to time t_2 of FIGURE 2b.

20 The amplitude of current I_{b2} of FIGURE 2b remains substantially constant during a latter portion of the first half of trace, interval t_1-t_2 . This is so because windings W2 and W3 are heavily loaded by the low impedance of the base-emitter junction of transistor Q2. At time t_2 , a deflection current I_H in deflection winding L_H of FIGURE 1 reverses polarity. As a result of current
25 reversals in deflection winding L_H of circuit 103 of FIGURE 1 and in a flyback transformer winding T2a, collector current I_{c2} starts flowing in transistor Q2 of FIGURE 1 after time t_2 of FIGURE 2c in an upramping manner.

30 Upamping collector current I_{c2} that flows as an emitter current through winding W3 of FIGURE 1 is transformer-coupled through current transformer T1 to the base of transistor Q2 in accordance with a turns ratio $N2:N3$ of windings W2 and W3, respectively. Transformer coupled current I_{c2} provides a major portion of upramping forward base current I_{b2} of transistor Q2,
35 during the second half of trace, interval t_2-t_3 , when collector current I_{c2} is upramping. The base-emitter junction of transistor Q2 forms a very low impedance across winding W2. Therefore, a performance similar to that of an ideal current transformer



operation is obtained in transformer T1 for coupling the current in winding W3 to winding W2. The required turn ratio between windings W2 and W3 is determined by the current gain h_{FE} of transistor Q2. Current gain h_{FE} is within a tolerance range of, for example, 4 and 7.

Upamping base current that is proportional to current I_{c2} is induced in winding W2 of FIGURE 1 only after time t_2 of FIGURE 2b. Transformer coupled upamping current I_{c2} of FIGURE 2c is added to the aforementioned current already provided by the stored magnetic energy in transformer T1 of FIGURE 1 to form upamping base current I_{b2} of FIGURE 2b. During interval t_2 - t_3 , base current I_{b2} is produced mainly from current I_{c2} of FIGURE 2c. The rate of change of current I_{b2} of FIGURE 2b closely tracks the base current requirement of deflection transistor Q2 of FIGURE 1 having upamping collector current I_{c2} of FIGURE 2c. Thus, with respect to collector current I_{c2} , base current I_{b2} varies in a positive feedback manner. Therefore, the conductivity of transistor Q2 of FIGURE 1 is controlled in a manner that maintains transistor Q2 in saturation without significantly overdriving the base of transistor Q2, during the second half of trace interval, t_2 - t_3 of FIGURE 2b. Cut-off of transistor Q2 of FIGURE 1 is initiated at time t_3 of FIGURE 2c, when transistor Q1 of FIGURE 1 is switched into saturation, as explained in a copending U.S. Patent Application Serial No. 481,426 entitled, A DEFLECTION DRIVER IN A VIDEO APPARATUS, in the name of Bruno E. Hennig, that is incorporated by reference herein.

A feedback network 200, embodying an inventive feature, includes a capacitor 202 coupled in series with a resistor 201. Network 200 is coupled between a terminal 103a of trace capacitor C_S and the collector electrode of transistor Q1. Terminal 103a is coupled between capacitor C_S and winding L_H . A resistor 203 is coupled in series with a capacitor 204 to form a damping network arrangement that is coupled to the collector electrode of transistor Q1. Network 200 prevents the occurrence of an abnormal steady state operation.

FIGURES 3a-3e illustrate approximate waveforms that occur in such abnormal steady state operation under the conditions that network 200 is removed from the circuit of

FIGURE 1 and the h_{FE} of transistor Q2 is larger than, for example, 6. Similar symbols and numerals in FIGURES 1, 2a-2d and 3a-3c indicate similar items or functions.

When the nominal value of the h_{FE} is larger than, for example, 6, base current I_{b2} of FIGURE 1 is capable of driving transistor Q2 into saturation at a level of collector current I_{c2} , at the end of trace, that is higher than in normal operation. The negative peak amplitude of current I_H at time t_b of FIGURE 3b, at the end of retrace, is approximately equal to the positive peak amplitude of current I_H at time t_a , at the end of trace. During trace, the rate of change of current I_H is predetermined and established by circuit parameters such as voltage B+. The excessively large peak amplitude of current I_H at times t_a and t_b of FIGURE 3b causes the positive peak amplitude of current I_H at time t_c , at the end of the following trace interval, to be smaller than at time t_a , at the end of the preceding trace interval.

Thus, in the abnormal steady state operation, each of peak collector current I_{c2} of FIGURE 3a and of base current I_{b2} of FIGURE 3e of transistor Q2 of FIGURE 1 is larger than in normal steady state operation, in alternate trace intervals. On the other hand, in the other alternate trace intervals, the peaks of collector current I_{c2} of FIGURE 3a and base current I_{b2} of FIGURE 3e are smaller than in normal steady state operation. Also the peak amplitude of each of flyback collector voltage V_{c2} of FIGURE 3d and of deflection current I_H of FIGURE 3b is larger than in normal operation, in alternate deflection cycles.

When collector current I_{c2} of transistor Q2 of FIGURE 1 is at the peak level, at the end of trace, the h_{FE} becomes even smaller than its nominal value. The abnormal steady state does not occur when the nominal value of the h_{FE} is smaller than, for example, 6. It is believed that base current I_{b2} produced in a positive feedback manner through transistor T1 cannot sustain the large peak level of current I_{c2} at the end of trace, when the nominal value of the h_{FE} is smaller than, for example, 6. It follows that only normal steady state operation can be sustained in which the peak level of current I_{c2} of FIGURE 2c is the same in each cycle.



- Network 200 that includes resistor 201, coupled in series with capacitor 202, forms a feedback path between terminal 103a of trace capacitor C_S , that forms with deflection winding L_H a trace resonant circuit, and the collector electrode of drive transistor Q1. A feedback current I_F is produced in network 200, by a differentiation action, from a parabola voltage V_P of FIGURE 3c developed across capacitor C_S of FIGURE 1. Voltage V_P , that is downramping during the second half of trace, produces current I_F of FIGURE 1 that flows in the direction of the arrow.
- 10 Current I_F is applied via winding W1 of transformer T1 in a manner that bypasses winding W2 to the base of transistor Q2.
- Current I_F is applied in a negative feedback manner with respect to the collector current I_{C2} . Current I_F produced by network 200 causes base current I_{B2} to be smaller than what
- 15 would be required for sustaining the abnormal steady state operation. Therefore, it is believed, base current I_{B2} cannot sustain the abnormal steady state operation. Thus, advantageously, only normal operation base and collector currents can be produced in transistor Q2 for any nominal value of the h_{FE}
- 20 of transistor Q2 selected from a tolerance range of values between, for example, 4 and 7. As explained before, without network 200, normal operation can be obtained when the h_{FE} is, for example, smaller than 6, but not when it is greater than 6.



**WHAT IS CLAIMED IS:**

1. A deflection apparatus of a video display apparatus, comprising:

a deflection winding (LH) coupled to a retrace capacitance (C4) to form a retrace resonant circuit, during a retrace interval of a deflection cycle;

a first switching transistor (Q2) responsive to a control signal (I_{b2}) at a frequency that is related to a deflection frequency developed at a control terminal (base) of said transistor and having a main current conducting terminal (collector) that is coupled to said retrace resonant circuit for generating a deflection current (I_H) in said deflection winding such that, during a portion (the second half) of a given trace interval of said deflection cycle, at least a portion of said deflection current flows in said main current conducting terminal;

a transformer (T1) having a first winding (W2) that is coupled to said control terminal of said first switching transistor and a second winding (W3) responsive to a signal produced by said first switching transistor (I_F) for developing a ramping portion of said control signal in a positive feedback manner with respect to the current in said main current conducting terminal of said first switching transistor such that a change in said current that flows in said main current conducting terminal of said first switching transistor, occurring in a ramping manner during said portion of said given trace interval, produces a change in said ramping portion of said control signal during the same portion of said given trace interval; characterized by

a feedback network (201,202) responsive to a signal (V_p) produced by said first switching transistor for developing a feedback signal that is applied to a control terminal (base) of said first switching transistor in a negative feedback manner with respect to the current in said main current conducting terminal.

2. An apparatus according to Claim 1 characterized by, a source (102) of an input signal (V_{OSC}) at a frequency that is related to said deflection frequency and a second switching transistor (Q1) responsive to said input signal and having a main current conducting terminal (collector) that is coupled to a third





winding (W1) of said transformer for generating a switching current (I_{c1}) in said third winding that is transformer coupled via said transformer to said control terminal of said first switching transistor to control timing of the switching in said first switching transistor.

3. A deflection apparatus according to Claim 2 characterized in that said feedback network (202, 201) comprises a first capacitor (202) having a first terminal that is coupled to a junction terminal between said second switching transistor (Q1) and said third winding (W1).

4. A deflection apparatus according to Claim 3 characterized in that said feedback network (202) further comprises a resistor (201) that is coupled in series with said first capacitor (202).

5. A deflection apparatus according to Claim 3 characterized by, a trace capacitor (C_S) coupled to said deflection winding (L_H) wherein a second terminal of said first capacitor is coupled to a junction terminal (103a) between said trace capacitor and said deflection winding (L_H).

6. A deflection apparatus according to Claim 2 characterized by, first switching means (D2) coupled in parallel with said first switching transistor (Q2) for conducting at least a substantial portion of said deflection current (I_H) in a manner that bypasses said first switching transistor during a first half of said trace interval of said deflection cycle such that during a second half of said trace interval, at least a substantial portion of said deflection current is conducted, instead, in said first switching transistor, wherein said second switching transistor (Q1) generates said current in said third winding (W1) prior to an instant within said trace interval when the current is switched over from being conducted in said first switching means to being conducted in said first switching transistor.





7. A deflection apparatus according to Claim 2 characterized in that said second switching transistor (Q1) produces in said transformer (T1) a first portion (trace) of said control signal (I_{b2}) in a flyback manner that initiates turn-on operation in said first switching transistor (Q2) and a second portion (retrace) of said control signal that initiates a turn-off operation in said first switching transistor.

8. A deflection apparatus according to Claim 1 characterized in that said second winding (W3) is coupled in a main current path of said first switching transistor (Q2) such that a current that flows in said main current path is coupled to said control terminal (base) of said first switching transistor via said second winding.

9. A deflection apparatus according to Claim 8 characterized in that said first switching transistor (Q2) comprises a bipolar transistor and wherein said first winding (W2) is coupled to a base electrode of said first switching transistor for generating said control signal (I_{b2}) as a ramping base current, during a second half of said trace interval.

10. A deflection apparatus according to Claim 1 characterized in that said first switching transistor (Q2) comprises a bipolar transistor and wherein said second winding (W3) is coupled to an emitter electrode thereof such that said emitter electrode thereof is interposed between said deflection winding (L_H) and said second winding.

11. A deflection apparatus according to Claim 1 characterized in that said deflection current is at a substantially higher frequency than 16 KHZ.

12. A television deflection apparatus, comprising:
a deflection retrace resonant circuit including a deflection winding (L_H) and a retrace capacitance (C4);
a first switching transistor (Q2) responsive to a control signal (I_{b2}) and coupled to said retrace resonant circuit for





performing a switching operation that generates a deflection current (I_H) in said deflection winding;

a deflection oscillator (102) for generating an input signal (V_{OSC}) at a frequency that is related to a deflection frequency;

a driver stage (Q1) responsive to said input signal for generating a drive signal (I_{c1});

a deflection driver transformer (T1) having a first winding (W1) that is coupled to said driver stage and is responsive to said drive signal, a second winding (W2) that is coupled to a control terminal (base) of said first switching transistor (Q2) and a third winding (W3) that is coupled in a collector current path of said first switching transistor for transformer coupling each of said drive signal and collector current to said control terminal of said first switching transistor to develop corresponding portions of said control signal at said control terminal; characterized by

a feedback network (201, 202) responsive to a signal (V_p) that is produced by said first switching transistor and coupled to said control terminal of said first switching transistor via a signal path (W1, W2) that bypasses said third winding for generating a feedback signal that is coupled to said control terminal of said first switching transistor.

13. A deflection apparatus of a video display apparatus comprising:

a deflection winding (L_H) coupled to a trace capacitor (C_S) to form a trace resonant circuit for developing a parabolic voltage (V_p) in said trace capacitor, during a trace interval of a deflection cycle, said deflection winding being coupled to a retrace capacitance (C_4) to form a retrace resonant circuit, during a retrace interval of said deflection cycle;

a first switching transistor (Q2) responsive to a control signal (I_{b2}) at a frequency that is related to a deflection frequency and coupled to said resonant circuits for performing a switching operation that generates a deflection current (I_H) in said deflection winding;





a source of an input signal (102) at a frequency that is related to a deflection frequency;

a driver stage (Q1) responsive to said input signal and coupled to said first switching transistor for generating said control signal; characterized by

a feedback network (201, 202) having a first terminal that is coupled between said trace capacitor and said deflection winding and a second terminal (collector of Q1) that is coupled to said driver stage, said feedback network including means (202) for differentiating said parabolic voltage to produce a feedback signal that is developed at said second terminal.

14. A deflection apparatus of a video display apparatus comprising:

a deflection winding (L_H) coupled to a trace capacitor (C_S) to form a trace resonant circuit during a trace interval of a deflection cycle and coupled to a retrace capacitance (C_4) to form a retrace resonant circuit, during a retrace interval of said deflection cycle;

a first switching transistor (Q2) responsive to a control signal (I_{b2}) at a frequency that is related to a deflection frequency and coupled to said resonant circuits for performing a switching operation that generates a deflection current (i_H) in said deflection winding;

a transformer (T1) having a first winding (W2) that is coupled to a control terminal (base) of said first switching transistor and a second winding (W3) that is coupled in a current path of a current that flows in a main current conducting terminal (emitter) of said first switching transistor to develop a first portion of said control signal in a positive feedback manner;

a source (102) of an input signal (V_{OSC}) at a frequency that is related to a deflection frequency; and

a second switching transistor (Q1) responsive to said input signal and coupled to a third winding (W1) of said transformer for generating a switching current (i_{c1}) in said second switching transistor and in said third winding of said transformer that is transformer coupled via said transformer to said control terminal of said first switching transistor to develop a second





portion of said control signal at said control terminal;
characterized by

a feedback network (201, 202) having a first terminal
that is coupled to one of said resonant circuits and a second
terminal that is coupled to said third winding of said transformer.

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ABSTRACT

A driver stage of a horizontal deflection output transistor (Q2) includes a transformer (T1) having a first winding (W1) coupled to a collector of a second, driver transistor (Q1) responsive to an input signal (V_{OSC}) at a horizontal deflection frequency. A second winding (W2) of the transformer is coupled across a base-emitter junction of the output transistor and a third winding (W3) is coupled to the emitter of and in series with the output transistor. The third winding couples the emitter current to the base of the output transistor for supplying a substantial portion of the base current during the second half of trace. A feedback network (201, 202) is coupled between a trace capacitor (C_S) coupled to a horizontal deflection winding (L_H) and the collector of the driver transistor for preventing abnormal steady state operation in the output transistor.

Figure 1



FIG. 1

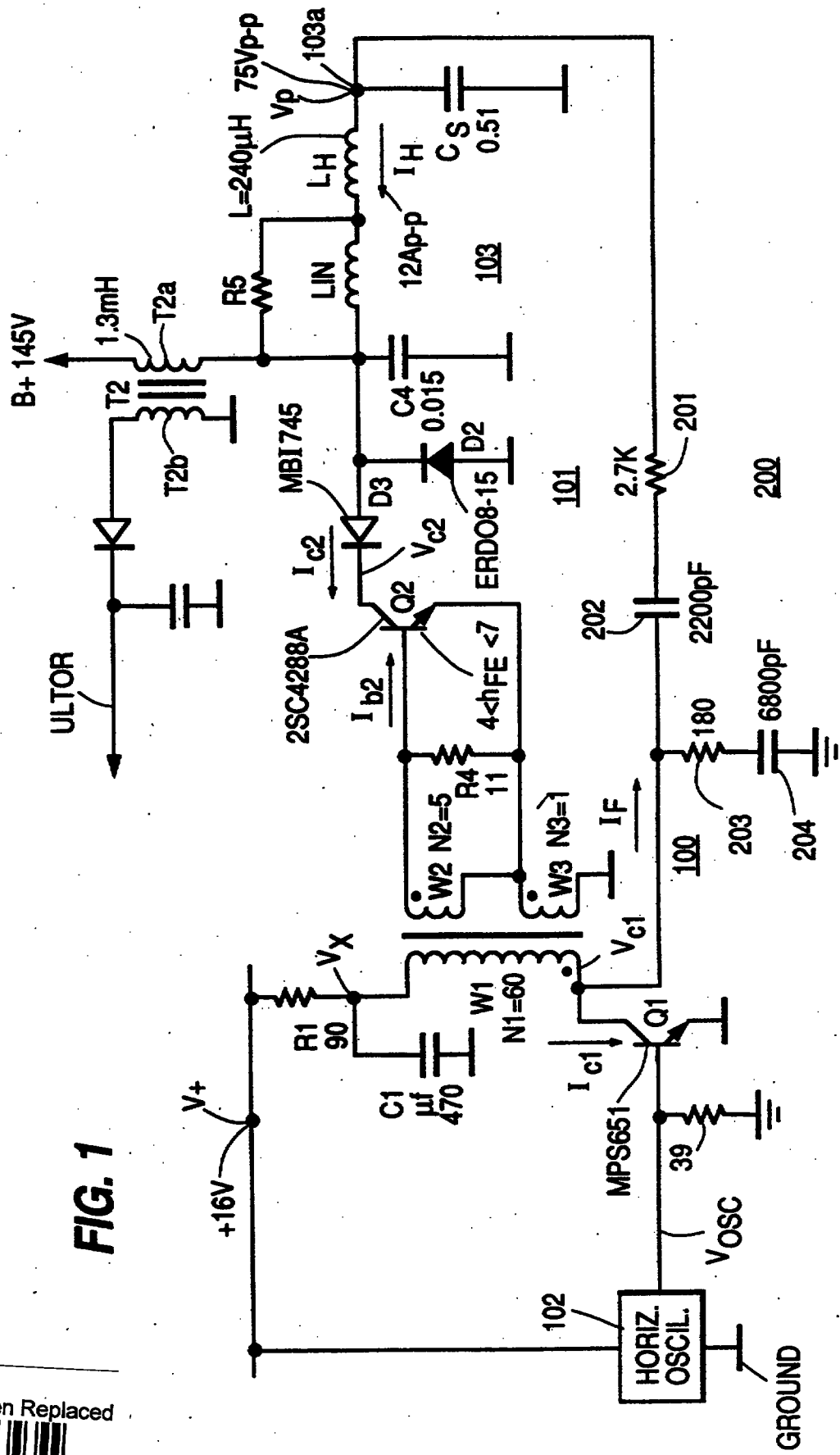


FIG. 2a

FIG. 2b

FIG. 2c

FIG. 2d

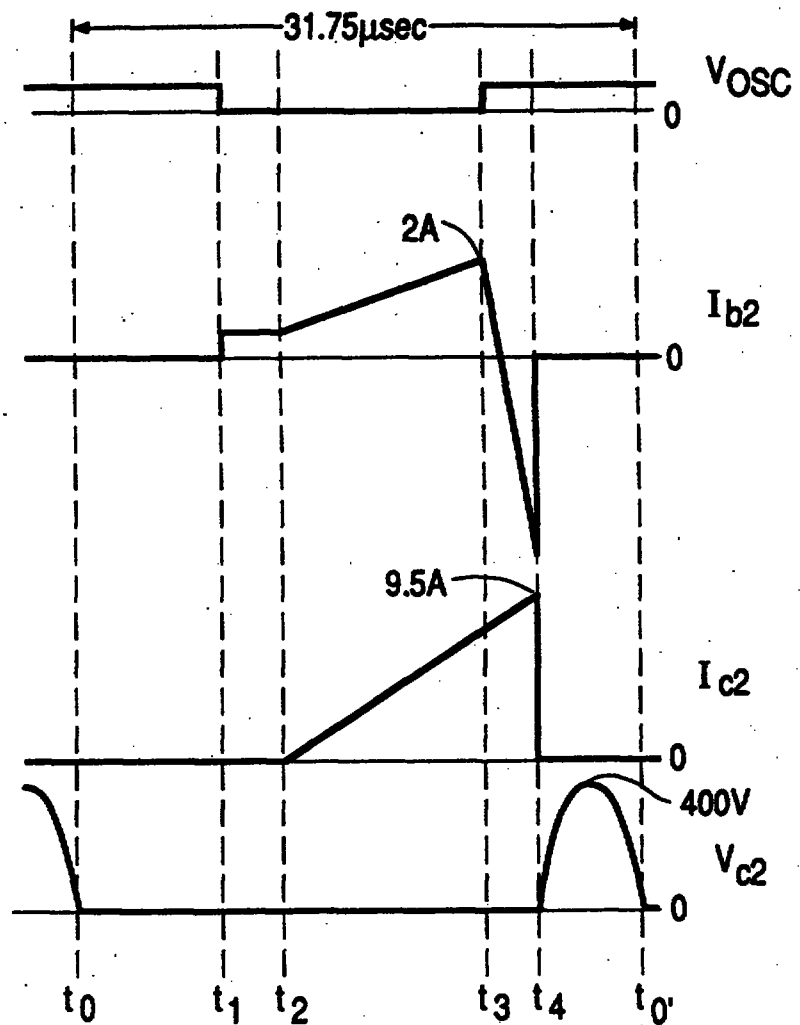


FIG. 3a



FIG. 3b

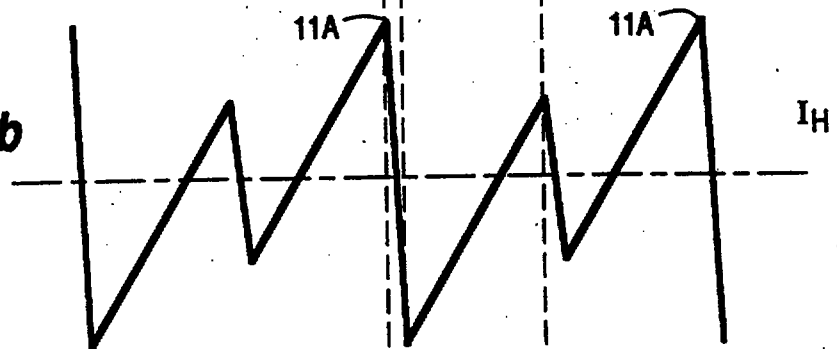


FIG. 3c



FIG. 3d

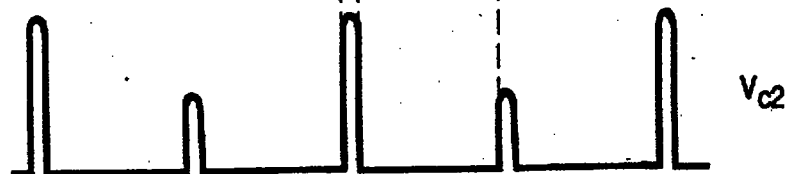
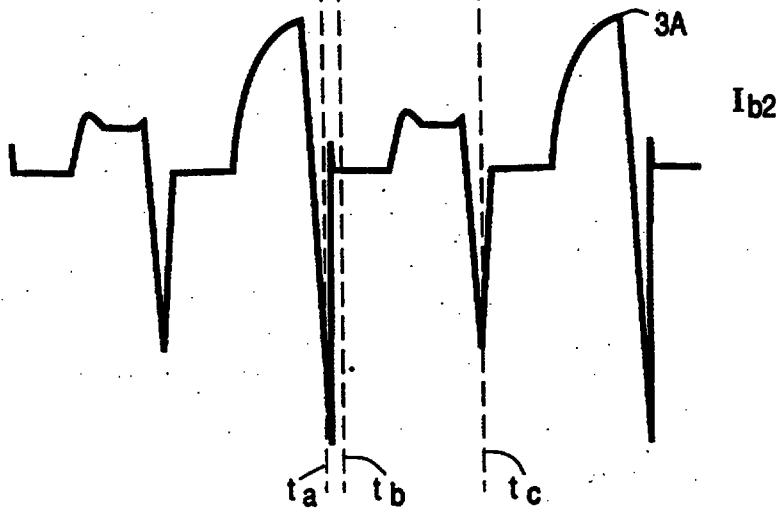


FIG. 3e



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A FEEDBACK ARRANGEMENT IN A DEFLECTION CIRCUIT

The invention relates to a deflection circuit output stage of a cathode ray tube (CRT) in a television receiver or other such display device. In particular, the invention relates to a
 5 feedback network in a horizontal deflection circuit output stage in which a switching output transistor, operating in a switching mode, produces a deflection current in a horizontal deflection winding of the CRT.

A typical horizontal deflection circuit that is used in
 10 various color television receivers includes a driver or drive stage having a transformer coupled to a control terminal of the output transistor of the deflection circuit output stage. The driver stage further includes a second switching transistor having a collector electrode that is coupled to a primary winding of the transformer.
 15 When the switching transistor of the driver stage is conductive, magnetic energy is stored in the inductance of the primary winding. At the same time, a transformer coupled voltage developed across a secondary winding of the transformer causes
 20 the switching output transistor of the output stage, driven by the voltage developed in the secondary winding of the transformer, to be non-conductive. When the second switching transistor of the driver stage becomes non-conductive, the stored magnetic energy in the coupling transformer produces, in a flyback manner, a
 25 winding current that flows in the secondary winding of the coupling transformer to form a forward base current. The forward base current drives the deflection output transistor into saturation prior to the beginning time of the upramping collector current in the output transistor.

In one prior art circuit, the transformer has a winding
 30 that is coupled in a current path of the collector current of the switching output transistor. In the second half of trace, the collector current in the output transistor increases in an upramping manner. The upramping collector current is coupled via the transformer to the base of the output transistor, in a
 35 positive feedback manner. The result is that an upramping base current is generated.

In such prior art circuit, the deflection circuit might operate in an abnormal stable state, should the value of the

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current gain parameter, h_{FE} , of the output transistor be greater than, for example, 6. In the abnormal stable state, the peak amplitude of the collector current is larger than in normal steady state operating condition, in alternate trace intervals, and smaller than in normal steady state operation, in the other alternate trace intervals. It may be desirable to prevent such abnormal steady state operation.

A television deflection apparatus, embodying an aspect of the invention, includes a deflection winding coupled to a retrace capacitance to form a retrace resonant circuit, during a retrace interval of a deflection cycle. A first switching transistor is responsive to a control signal at a frequency that is related to a deflection frequency developed at a control terminal of the transistor. The transistor has a main current conducting terminal that is coupled to the retrace resonant circuit for generating a deflection current in the deflection winding. During a portion of a trace interval of the deflection cycle, at least a portion of the deflection current flows in the main current conducting terminal. A transformer has a first winding that is coupled to the control terminal of the first switching transistor and a second winding responsive to a signal produced by the first switching transistor. The transformer develops a ramping portion of the control signal in a positive feedback manner with respect to the current in the main current conducting terminal of the first switching transistor. A feedback network responsive to a signal produced by the first switching transistor develops a feedback signal that is applied to a control terminal of the first switching transistor in a negative feedback manner with respect to the current in the main current conducting terminal.

In accordance with an inventive feature, the feedback signal prevents the aforementioned abnormal steady state operation.

FIGURE 1 illustrates a horizontal deflection circuit output stage including a feedback network, embodying an aspect of the invention, coupled from a trace capacitor to a driver stage;

FIGURES 2a-2d illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1 in normal operation; and

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FIGURES 3a-3e illustrate waveforms in abnormal steady state operation for a deflection such as in Figure 1 but without the feedback network of FIGURE 1.

FIGURE 1 illustrates a driver stage 100 for driving a switching output transistor Q2 of a horizontal deflection circuit output stage 101 of a television receiver, embodying an aspect of the invention. A conventional horizontal oscillator 102 produces an output signal V_{OSC} . Signal V_{OSC} is at a horizontal frequency of $2xf_H$ that is approximately 32 KHZ. Signal V_{OSC} is coupled via an emitter follower, not shown, to a base electrode of a driver transistor Q1. Frequency f_H , that is about 16 KHZ, is the horizontal deflection frequency in, for example, the NTSC standard. Thus, frequency $2xf_H$ is substantially higher than 16 KHZ.

Oscillator 102 is controlled by an on/off control signal. Signal on/off causes transistor Q1 to be turned on when signal on/off is at the "OFF" state, throughout standby operation. A collector of transistor Q1 is coupled to one end terminal of a primary winding W1 of a coupling transformer T1. The other end terminal of winding W1 is bypassed to ground by a filter capacitor C1 and coupled via a current limiting resistor R1 to a source of supply voltage V+ such that resistor R1 and capacitor C1 form a ripple filter.

A secondary winding W2 of transformer T1 is coupled across a base-emitter junction of transistor Q2 and across a resistor R4. A junction terminal 101a that is coupled at a junction of winding W2, resistor R4 and the emitter of transistor Q2 is coupled to one end terminal of a winding W3 of transformer T1. The other end terminal of winding W3 is coupled to ground.

The collector of transistor Q2 is coupled in series with a diode D3 to a conventional damper diode D2 of a horizontal deflection circuit 103. Circuit 103 includes a horizontal deflection winding L_H , a retrace capacitor C4, a trace capacitor C_S , a linearity inductor LIN, and a linearity resistor R5 that are coupled in a well-known manner. Diode D3 prevents reverse collector current from flowing in transistor Q2 and in winding W2 or W3. A supply voltage B+ is coupled to circuit 103 via a winding T2a of a horizontal flyback transformer T2. During retrace, circuit 103 forms a retrace resonant circuit that includes capacitor C4,

winding L_H and winding LIN. During trace, circuit 103 forms a trace resonant circuit that includes trace capacitor C_s and winding L_H . Voltages B+ and V+ are produced both in standby and in run mode operations.

5 FIGURES 2a-2d illustrate idealized or approximated waveforms useful for explaining the normal operation of the circuit of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2d indicate similar items or functions.

10 In operation, driver transistor Q1 of FIGURE 1 is conductive as a result of signal V_{OSC} of FIGURE 2a being positive until time t_1 of FIGURE 2a that causes transistor Q2 to be nonconductive. The magnetic energy supplied by a collector current I_{c1} of transistor Q1 is stored in winding W1 of FIGURE 1. When transistor Q1 is turned off, during interval t_1 - t_3 of FIGURE 15 2a, the stored energy produces in winding W2 of FIGURE 1 a forward base current I_{b2} of transistor Q2. Current I_{b2} is sufficient to turn on deflection transistor Q2 and to maintain it in saturation prior to time t_2 of FIGURE 2b.

20 The amplitude of current I_{b2} of FIGURE 2b remains substantially constant during a latter portion of the first half of trace, interval t_1 - t_2 . This is so because windings W2 and W3 are heavily loaded by the low impedance of the base-emitter junction of transistor Q2. At time t_2 , a deflection current I_H in deflection winding L_H of FIGURE 1 reverses polarity. As a result of current 25 reversals in deflection winding L_H of circuit 103 of FIGURE 1 and in a flyback transformer winding T2a, collector current I_{c2} starts flowing in transistor Q2 of FIGURE 1 after time t_2 of FIGURE 2c in an upramping manner.

30 Upamping collector current I_{c2} that flows as an emitter current through winding W3 of FIGURE 1 is transformer-coupled through current transformer T1 to the base of transistor Q2 in accordance with a turns ratio $N2:N3$ of windings W2 and W3, respectively. Transformer coupled current I_{c2} provides a major portion of upramping forward base current I_{b2} of transistor Q2, 35 during the second half of trace, interval t_2 - t_3 , when collector current I_{c2} is upramping. The base-emitter junction of transistor Q2 forms a very low impedance across winding W2. Therefore, a performance similar to that of an ideal current transformer

operation is obtained in transformer T1 for coupling the current in winding W3 to winding W2. The required turn ratio between windings W2 and W3 is determined by the current gain h_{FE} of transistor Q2. Current gain h_{FE} is within a tolerance range of, for example, 4 and 7.

Upramping base current that is proportional to current I_{c2} is induced in winding W2 of FIGURE 1 only after time t_2 of FIGURE 2b. Transformer coupled upramping current I_{c2} of FIGURE 2c is added to the aforementioned current already provided by the stored magnetic energy in transformer T1 of FIGURE 1 to form upramping base current I_{b2} of FIGURE 2b. During interval t_2 - t_3 , base current I_{b2} is produced mainly from current I_{c2} of FIGURE 2c. The rate of change of current I_{b2} of FIGURE 2b closely tracks the base current requirement of deflection transistor Q2 of FIGURE 1 having upramping collector current I_{c2} of FIGURE 2c. Thus, with respect to collector current I_{c2} , base current I_{b2} varies in a positive feedback manner. Therefore, the conductivity of transistor Q2 of FIGURE 1 is controlled in a manner that maintains transistor Q2 in saturation without significantly overdriving the base of transistor Q2, during the second half of trace interval, t_2 - t_3 of FIGURE 2b. Cut-off of transistor Q2 of FIGURE 1 is initiated at time t_3 of FIGURE 2c, when transistor Q1 of FIGURE 1 is switched into saturation, as explained in a copending U.S. Patent Application Serial No. 481,426 entitled, A DEFLECTION DRIVER IN A VIDEO APPARATUS, in the name of Bruno E. Hennig, that is incorporated by reference herein.

A feedback network 200, embodying an inventive feature, includes a capacitor 202 coupled in series with a resistor 201. Network 200 is coupled between a terminal 103a of trace capacitor C_S and the collector electrode of transistor Q1. Terminal 103a is coupled between capacitor C_S and winding L_H . A resistor 203 is coupled in series with a capacitor 204 to form a damping network arrangement that is coupled to the collector electrode of transistor Q1. Network 200 prevents the occurrence of an abnormal steady state operation.

FIGURES 3a-3e illustrate approximate waveforms that occur in such abnormal steady state operation under the conditions that network 200 is removed from the circuit of

FIGURE 1 and the h_{FE} of transistor Q2 is larger than, for example, 6. Similar symbols and numerals in FIGURES 1, 2a-2d and 3a-3c indicate similar items or functions.

When the nominal value of the h_{FE} is larger than, for example, 6, base current I_{b2} of FIGURE 1 is capable of driving transistor Q2 into saturation at a level of collector current I_{c2} , at the end of trace, that is higher than in normal operation. The negative peak amplitude of current I_H at time t_b of FIGURE 3b, at the end of retrace, is approximately equal to the positive peak amplitude of current I_H at time t_a , at the end of trace. During trace, the rate of change of current I_H is predetermined and established by circuit parameters such as voltage $B+$. The excessively large peak amplitude of current I_H at times t_a and t_b of FIGURE 3b causes the positive peak amplitude of current I_H at time t_c , at the end of the following trace interval, to be smaller than at time t_a , at the end of the preceding trace interval.

Thus, in the abnormal steady state operation, each of peak collector current I_{c2} of FIGURE 3a and of base current I_{b2} of FIGURE 3e of transistor Q2 of FIGURE 1 is larger than in normal steady state operation, in alternate trace intervals. On the other hand, in the other alternate trace intervals, the peaks of collector current I_{c2} of FIGURE 3a and base current I_{b2} of FIGURE 3e are smaller than in normal steady state operation. Also the peak amplitude of each of flyback collector voltage V_{c2} of FIGURE 3d and of deflection current I_H of FIGURE 3b is larger than in normal operation, in alternate deflection cycles.

When collector current I_{c2} of transistor Q2 of FIGURE 1 is at the peak level, at the end of trace, the h_{FE} becomes even smaller than its nominal value. The abnormal steady state does not occur when the nominal value of the h_{FE} is smaller than, for example, 6. It is believed that base current I_{b2} produced in a positive feedback manner through transistor T1 cannot sustain the large peak level of current I_{c2} at the end of trace, when the nominal value of the h_{FE} is smaller than, for example, 6. It follows that only normal steady state operation can be sustained in which the peak level of current I_{c2} of FIGURE 2c is the same in each cycle.

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Network 200 that includes resistor 201, coupled in series with capacitor 202, forms a feedback path between terminal 103a of trace capacitor C_S , that forms with deflection winding L_H a trace resonant circuit, and the collector electrode of drive transistor Q1. A feedback current I_F is produced in network 200, by a differentiation action, from a parabola voltage V_P of FIGURE 3c developed across capacitor C_S of FIGURE 1. Voltage V_P , that is downramping during the second half of trace, produces current I_F of FIGURE 1 that flows in the direction of the arrow.

10 Current I_F is applied via winding W1 of transformer T1 in a manner that bypasses winding W2 to the base of transistor Q2.

Current I_F is applied in a negative feedback manner with respect to the collector current I_{C2} . Current I_F produced by network 200 causes base current I_{B2} to be smaller than what would be required for sustaining the abnormal steady state operation. Therefore, it is believed, base current I_{B2} cannot sustain the abnormal steady state operation. Thus, advantageously, only normal operation base and collector currents can be produced in transistor Q2 for any nominal value of the h_{FE}

15 of transistor Q2 selected from a tolerance range of values between, for example, 4 and 7. As explained before, without network 200, normal operation can be obtained when the h_{FE} is, for example, smaller than 6, but not when it is greater than 6.

20



WHAT IS CLAIMED IS:

1. A deflection apparatus of a video display apparatus, comprising:

a deflection winding (LH) coupled to a retrace capacitance (C4) to form a retrace resonant circuit, during a retrace interval of a deflection cycle;

a first switching transistor (Q2) responsive to a control signal (I_{b2}) at a frequency that is related to a deflection frequency developed at a control terminal (base) of said transistor and having a main current conducting terminal (collector) that is coupled to said retrace resonant circuit for generating a deflection current (I_H) in said deflection winding such that, during a portion (the second half) of a given trace interval of said deflection cycle, at least a portion of said deflection current flows in said main current conducting terminal;

a transformer (T1) having a first winding (W2) that is coupled to said control terminal of said first switching transistor and a second winding (W3) responsive to a signal produced by said first switching transistor (I_F) for developing a ramping portion of said control signal in a positive feedback manner with respect to the current in said main current conducting terminal of said first switching transistor such that a change in said current that flows in said main current conducting terminal of said first switching transistor, occurring in a ramping manner during said portion of said given trace interval, produces a change in said ramping portion of said control signal during the same portion of said given trace interval; characterized by

a feedback network (201,202) responsive to a signal (V_p) produced by said first switching transistor for developing a feedback signal that is applied to a control terminal (base) of said first switching transistor in a negative feedback manner with respect to the current in said main current conducting terminal.

2. An apparatus according to Claim 1 characterized by, a source (102) of an input signal (V_{OSC}) at a frequency that is related to said deflection frequency and a second switching transistor (Q1) responsive to said input signal and having a main current conducting terminal (collector) that is coupled to a third

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winding (W1) of said transformer for generating a switching current (I_{c1}) in said third winding that is transformer coupled via said transformer to said control terminal of said first switching transistor to control timing of the switching in said first switching transistor.

3. A deflection apparatus according to Claim 2 characterized in that said feedback network (202, 201) comprises a first capacitor (202) having a first terminal that is coupled to a junction terminal between said second switching transistor (Q1) and said third winding (W1).

4. A deflection apparatus according to Claim 3 characterized in that said feedback network (202) further comprises a resistor (201) that is coupled in series with said first capacitor (202).

5. A deflection apparatus according to Claim 3 characterized by, a trace capacitor (C_S) coupled to said deflection winding (L_H) wherein a second terminal of said first capacitor is coupled to a junction terminal (103a) between said trace capacitor and said deflection winding (L_H).

6. A deflection apparatus according to Claim 2 characterized by, first switching means (D2) coupled in parallel with said first switching transistor (Q2) for conducting at least a substantial portion of said deflection current (I_H) in a manner that bypasses said first switching transistor during a first half of said trace interval of said deflection cycle such that during a second half of said trace interval, at least a substantial portion of said deflection current is conducted, instead, in said first switching transistor, wherein said second switching transistor (Q1) generates said current in said third winding (W1) prior to an instant within said trace interval when the current is switched over from being conducted in said first switching means to being conducted in said first switching transistor.

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7. A deflection apparatus according to Claim 2 characterized in that said second switching transistor (Q1) produces in said transformer (T1) a first portion (trace) of said control signal (I_{b2}) in a flyback manner that initiates turn-on operation in said first switching transistor (Q2) and a second portion (retrace) of said control signal that initiates a turn-off operation in said first switching transistor.

8. A deflection apparatus according to Claim 1 characterized in that said second winding (W3) is coupled in a main current path of said first switching transistor (Q2) such that a current that flows in said main current path is coupled to said control terminal (base) of said first switching transistor via said second winding.

9. A deflection apparatus according to Claim 8 characterized in that said first switching transistor (Q2) comprises a bipolar transistor and wherein said first winding (W2) is coupled to a base electrode of said first switching transistor for generating said control signal (I_{b2}) as a ramping base current, during a second half of said trace interval.

10. A deflection apparatus according to Claim 1 characterized in that said first switching transistor (Q2) comprises a bipolar transistor and wherein said second winding (W3) is coupled to an emitter electrode thereof such that said emitter electrode thereof is interposed between said deflection winding (L_H) and said second winding.

11. A deflection apparatus according to Claim 1 characterized in that said deflection current is at a substantially higher frequency than 16 KHZ.

12. A television deflection apparatus, comprising:
a deflection retrace resonant circuit including a deflection winding (L_H) and a retrace capacitance (C4);

a first switching transistor (Q2) responsive to a control signal (I_{b2}) and coupled to said retrace resonant circuit for



performing a switching operation that generates a deflection current (I_H) in said deflection winding;

a deflection oscillator (102) for generating an input signal (V_{OSC}) at a frequency that is related to a deflection frequency;

a driver stage (Q1) responsive to said input signal for generating a drive signal (I_{c1});

a deflection driver transformer (T1) having a first winding (W1) that is coupled to said driver stage and is responsive to said drive signal, a second winding (W2) that is coupled to a control terminal (base) of said first switching transistor (Q2) and a third winding (W3) that is coupled in a collector current path of said first switching transistor for transformer coupling each of said drive signal and collector current to said control terminal of said first switching transistor to develop corresponding portions of said control signal at said control terminal; characterized by

a feedback network (201, 202) responsive to a signal (V_p) that is produced by said first switching transistor and coupled to said control terminal of said first switching transistor via a signal path (W1, W2) that bypasses said third winding for generating a feedback signal that is coupled to said control terminal of said first switching transistor.

13. A deflection apparatus of a video display apparatus comprising:

a deflection winding (L_H) coupled to a trace capacitor (C_3) to form a trace resonant circuit for developing a parabolic voltage (V_p) in said trace capacitor, during a trace interval of a deflection cycle, said deflection winding being coupled to a retrace capacitance (C_4) to form a retrace resonant circuit, during a retrace interval of said deflection cycle;

a first switching transistor (Q2) responsive to a control signal (I_{b2}) at a frequency that is related to a deflection frequency and coupled to said resonant circuits for performing a switching operation that generates a deflection current (I_H) in said deflection winding;

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a source of an input signal (102) at a frequency that is related to a deflection frequency;

a driver stage (Q1) responsive to said input signal and coupled to said first switching transistor for generating said control signal; characterized by

a feedback network (201, 202) having a first terminal that is coupled between said trace capacitor and said deflection winding and a second terminal (collector of Q1) that is coupled to said driver stage, said feedback network including means (202) for differentiating said parabolic voltage to produce a feedback signal that is developed at said second terminal.

14. A deflection apparatus of a video display apparatus comprising:

a deflection winding (L_H) coupled to a trace capacitor (C_S) to form a trace resonant circuit during a trace interval of a deflection cycle and coupled to a retrace capacitance (C_4) to form a retrace resonant circuit, during a retrace interval of said deflection cycle;

a first switching transistor (Q2) responsive to a control signal (I_{b2}) at a frequency that is related to a deflection frequency and coupled to said resonant circuits for performing a switching operation that generates a deflection current (i_H) in said deflection winding;

a transformer (T1) having a first winding (W2) that is coupled to a control terminal (base) of said first switching transistor and a second winding (W3) that is coupled in a current path of a current that flows in a main current concuting terminal (emitter) of said first switching transistor to develop a first portion of said control signal in a positive feedback manner;

a source (102) of an input signal (V_{OSC}) at a frequency that is related to a deflection frequency; and

a second switching transistor (Q1) responsive to said input signal and coupled to a third winding (W1) of said transformer for generating a switching current (i_{c1}) in said second switching transistor and in said third winding of said transformer that is transformer coupled via said transformer to said control terminal of said first switching transistor to develop a second

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portion of said control signal at said control terminal,
characterized by

a feedback network (201, 202) having a first terminal
that is coupled to one of said resonant circuits and a second
terminal that is coupled to said third winding of said transformer.

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A FEEDBACK ARRANGEMENT IN A DEFLECTION CIRCUIT**ABSTRACT**

A driver stage of a horizontal deflection output transistor (Q2) includes a transformer (T1) having a first winding (W1) coupled to a collector of a second, driver transistor (Q1) responsive to an input signal (V_{OSC}) at a horizontal deflection frequency. A second winding (W2) of the transformer is coupled across a base-emitter junction of the output transistor and a third winding (W3) is coupled to the emitter of and in series with the output transistor. The third winding couples the emitter current to the base of the output transistor for supplying a substantial portion of the base current during the second half of trace. A feedback network (201, 202) is coupled between a trace capacitor (C_S) coupled to a horizontal deflection winding (L_H) and the collector of the driver transistor for preventing abnormal steady state operation in the output transistor.

Figure 1



FIG. 1

FIG. 2a

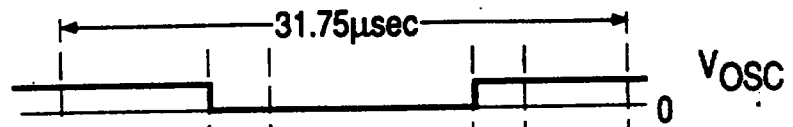


FIG. 2b

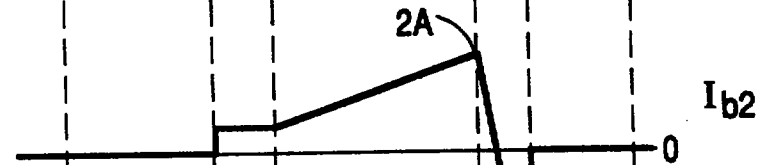


FIG. 2c

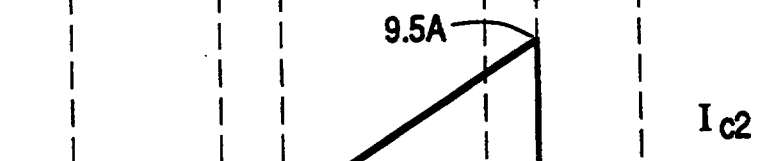
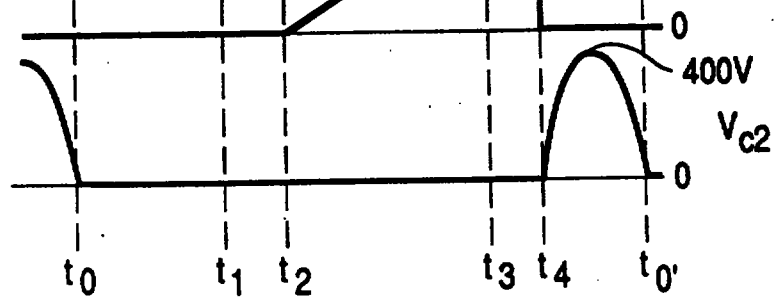
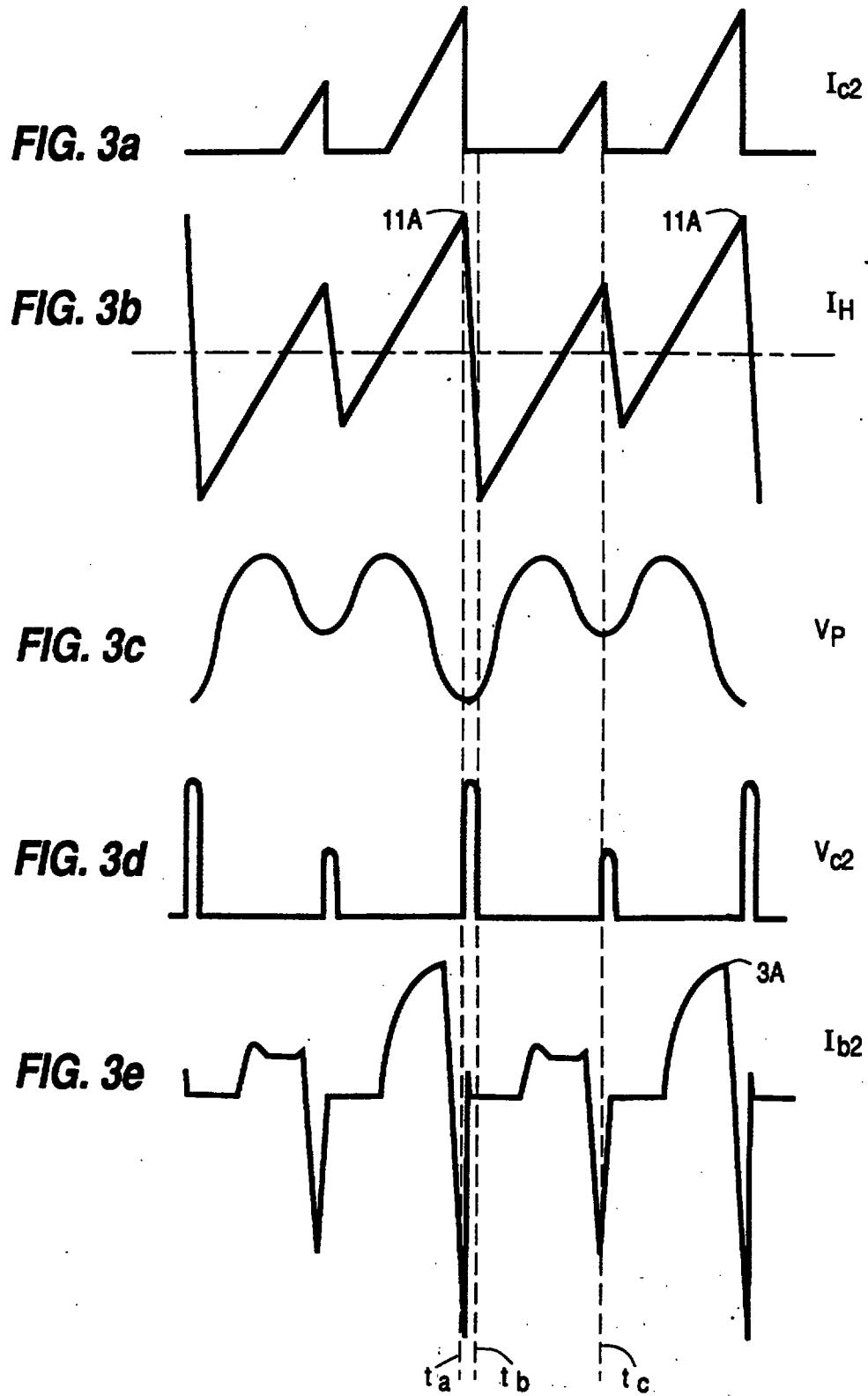


FIG. 2d





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