CLAIMS

1. A magnetoresistive random-access memory (MRAM) structure comprising:

an MRAM cell disposed between bit line and word line circuit elements; and

a vertical-cavity surface-emitting laser (VCSEL) element disposed above the MRAM cell, wherein a laser output of the VCSEL is directed toward the MRAM cell, wherein the VCSEL comprises Gallium Arsenide layers.

2. The MRAM structure according to claim 1 further comprising a capacitor connected to at least one word line circuit element.

3. The MRAM structure according to claim 1, wherein the MRAM cell comprises a magnetic tunnel junction.

4. The MRAM structure according to claim 1, further comprising a capacitor sized to destructively erase MRAM contents.

5. The MRAM structure according to claim 1, wherein at least one of the bit line and word line circuit elements comprises a conductive material.

6. The MRAM structure according to claim 1, wherein the VCSEL comprises a lower Bragg mirror, an upper Bragg mirror, and a quantum well disposed between the lower and upper Bragg mirrors.

7. A magnetoresistive random-access memory (MRAM) structure comprising:

a plurality of MRAM cells disposed between bit line and word line circuit elements;

a vertical-cavity surface-emitting laser (VCSEL) element disposed above the plurality of MRAM cells, wherein the VCSEL comprises Gallium Arsenide layers; and

wherein a laser output of the VCSEL is directed toward the plurality of MRAM cells.

8. The MRAM structure according to claim 7, further comprising a capacitor connected to at least one word line circuit element.

9. The MRAM structure according to claim 7, wherein the MRAM cell comprises a magnetic tunnel junction.

10. The MRAM structure according to claim 7, further comprising a capacitor sized to destructively erase MRAM contents.

11. The MRAM structure according to claim 7, wherein at least one of the bit line and word line circuit elements comprises a conductive material.

12. The MRAM structure according to claim 7, wherein the VCSEL comprises a lower Bragg mirror, an upper Bragg mirror, and a quantum well disposed between the lower and upper Bragg mirrors.

13. A method of fabricating a semiconductor device, the method comprising:

fabricating a plurality of magnetoresistive random-access memory (MRAM) cells electrically connected to one or more bit lines and word lines, the plurality of MRAM cells encapsulated in a dielectric material;

forming a grain filter cavity in the dielectric material;

forming an oriented seed crystal in the grain filter;

forming an amorphous semiconductor layer adjacent to the seed crystal;

crystalizing the amorphous semiconductor layer;

forming a vertical-cavity surface emitting laser (VCSEL) adjacent to the semiconductor layer;

removing the semiconductor layer; and

forming a dielectric layer on and around the VCSEL.

14. The method of fabricating a semiconductor device according to claim 13, further comprising forming a capacitor electrically connected to at least one of the bit line and word line.

15. The method of fabricating a semiconductor device according to claim 13, wherein the VCSEL comprises Gallium-Arsenide layers.

16. The method of fabricating a semiconductor device according to claim 13, wherein the MRAM cell comprises a magnetic tunnel junction.

17. The method of fabricating a semiconductor device according to claim 13, wherein at least one of the bit line and word line circuit elements comprises a conductive material.

18. The method of fabricating a semiconductor device according to claim 13, wherein the VCSEL comprises a lower Bragg mirror, an upper Bragg mirror, and a quantum well disposed between the lower and upper Bragg mirrors.