DISCONTINUOUS/NON-UNIFORM METAL CAP STRUCTURE AND PROCESS FOR INTERCONNECT INTEGRATION

Field of the Invention

[0001] The present invention relates to semiconductor interconnect structures, and a method of fabricating the same. More particularly, the present invention relates to semiconductor interconnect structures having enhanced electromigration (EM) resistance without degrading time dependent dielectric breakdown reliability.

Background of the Invention

[0002] Generally, semiconductor devices include a plurality of circuits that form an integrated circuit (IC) fabricated on a semiconductor substrate. A complex network of signal paths will normally be routed to connect the circuit elements distributed on the surface of the substrate. Efficient routing of these signals across the device requires formation of multilevel or multilayered schemes, such as, for example, single or dual damascene wiring structures. The wiring structure typically includes copper, Cu, since Cu based interconnects provide higher speed signal transmission between large numbers of transistors on a complex semiconductor chip as compared with aluminum, Al, based interconnects.

[0003] Within a typical interconnect structure, metal vias run perpendicular to the semiconductor substrate and metal lines run parallel to the semiconductor substrate. Further enhancement of the signal speed and reduction of signals in adjacent metal lines (known as "crosstalk") are achieved in today's IC product chips by embedding the metal lines and metal vias (e.g., conductive features) in a dielectric material having a dielectric constant of less than 4.0.

[0004] In semiconductor interconnect structures, electromigration (EM) has been identified as one metal failure mechanism. Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. The effect is important in applications where high direct

current densities are used, such as in microelectronics and related structures. As the structure size decreases, the practical significance of EM increases.

[0005] EM is one of the worst reliability concerns for very large scale integrated (VLSI) circuits and manufacturing since the 1960's. The problem not only needs to be overcome during the process development period in order to qualify the process, but it also persists through the lifetime of the chip. Voids are created inside the metal conductors of an interconnect structure due to metal ion movement caused by the high density of current flow.

[0006] Although the fast diffusion path in metal interconnects varies depending on the overall integration scheme and materials used for chip fabrication, it has been observed that metal atoms, such as Cu atoms, transported along the metal/post planarized dielectric cap interface play an important role on the EM lifetime projection. The EM initial voids first nucleate at the metal/dielectric cap interface and then grow in the direction to the bottom of the interconnect, which eventually results in a circuit dead opening.

[0007] FIGS. 1A-1D are pictorial representations of a prior art interconnect structure at various stages of an EM failure. In these drawings, reference numeral 12 denotes the dielectric cap, and reference numeral 10 denotes the metal interconnect feature; all other components of the prior art interconnect structure are not labeled to avoid obscuring the EM problem. FIG. 1A is at an initial stress stage. FIG. 1B is at a time when void 14 nucleation initiates at the metal interconnect feature 10/dielectric cap 12 interface. FIG. 1C is at a time when the void 14 grows towards the bottom of the conductive feature 10, and FIG. 1D is at a time in which the void 14 growth crosses the metal interconnect feature 10 causing a circuit dead opening.

[0008] It has been demonstrated that by replacing the Cu/dielectric interface with a Cu/metal interface can enhance electromigration resistance by greater than 100x. Prior art metal caps are typically comprised of a Co-containing alloy such as, for example, CoWP, which is selectively deposited atop of the Cu conductor region of the interconnect structure. One problem with utilizing such selective deposited metal caps is that some of the metal cap extends onto the

adjoining surface of the interconnect dielectric material and, as such, electrical shorts between adjacent interconnects may arise. This is seen, for example, in FIG. 2 wherein reference numeral 20 denotes a dielectric material, reference numeral 22 denotes a conductive material embedded within the dielectric material 20, reference numeral 24 denotes a Co-containing alloy metal cap, and reference numeral 25 denotes metal residues from the Co-containing alloy cap process.

[0009] In addition to the above, it is known to provide a metal cap directly on the surface of an interconnect conductive material, such as, for example, Cu, by recessing the interconnect conductive material below a surface of the interconnect dielectric material. Such a structure is shown, for example, in FIG. 3. In this figure, reference numeral 20 denotes the interconnect dielectric material, reference numeral 22 denotes the interconnect conductive material embedded within the dielectric material 20, reference numeral 23 denotes a dielectric cap, and reference numeral 24 denotes the metal cap. Although this prior art recess process provides a metal cap that is located only on a surface of the recessed conductive material, such a process is problematic since there is high process cost associated therewith.

[0010] It is also worth mentioning that during a clean in dilute hydrofluoric acid, which is generally used to clean the surface of the interconnect dielectric material, corrosion of metal caps may occur. This is particularly observed when CoWP is used as the metal cap material.

[0011] In view of the above, there is a continued need for providing an interconnect structure in which the EM resistance is enhanced without degrading the time dependent dielectric breakdown reliability of the interconnect structure.

Summary of the Invention

[0012] The present invention provides semiconductor interconnect structures that have improved EM reliability. The improved EM reliability is obtained without degrading the time dependent dielectric breakdown reliability of the interconnect structures. The present invention further

provides interconnect structures that have better reliability and technology extendibility for the semiconductor industry.

[0013] In one embodiment, the present invention provides an interconnect structure in which a discontinuous noble metal-containing cap is present on portions of an exposed upper surface of a non-recessed conductive material which is embedded within a low k dielectric material. The term "discontinuous" when referring to the noble metal-containing cap denotes that the cap exists as nuclei or islands atop some portions of an exposed upper surface of the non-recessed conductive material.

[0014] In another embodiment of the present invention, an interconnect structure is provided that includes a non-uniform noble metal-containing cap present on an exposed upper surface of a non-recessed conductive material which is embedded within a low k dielectric material. The term "non-uniform" when referring to the noble metal-containing cap denotes that the cap has a rough source defined by a variable thickness across the exposed upper surface of the embedded conductive material.

[0015] In both of the embodiments mentioned above, the noble metal-containing cap of the invention does not extend onto an exposed upper surface of the low k dielectric material. Preferably, the noble metal-containing cap of the invention does not extend onto an upper surface of a diffusion barrier that is used in separating the conductive material from the low k dielectric material. The latter embodiment in which the inventive noble metal-containing cap does not extend onto an upper surface of a diffusion barrier provides a structure that has improved leakage control as compared with prior art interconnect structures.

[0016] In general terms, the present invention provides an interconnect structure including:

a dielectric material having a dielectric constant of about 3.0 or less and at least one conductive material embedded therein, the at least one conductive material having an upper surface that is coplanar with an upper surface of the dielectric material; and

a noble metal-containing cap present at least on some portion of the upper surface of the at least one conductive material, wherein said noble metal-containing cap is discontinuous or has a non-uniform thickness.

[0017] In the inventive structure, there is no "residues" from the noble metal-containing cap deposited on the dielectric surface. By "residues" it is meant that no fragments of noble metal material form on the dielectric material surface. In some embodiments, the noble metal-containing cap is not present on an upper surface of a diffusion barrier that separates the at least one conductive material from the dielectric material.

[0018] The dielectric material which is present in the inventive interconnect structure may be any interconnect dielectric material having a dielectric constant of about 3.0 or less. Illustratively, the dielectric material employed in the present invention comprises a silsesquioxane, a C doped oxide (i.e., an organosilicate) that includes at least atoms of Si, C, O and H, a thermosetting polyarylene ether, or multilayers thereof. The dielectric material may be porous, non-porous or contain regions and/or surfaces that are porous and other regions and/or surfaces that are non-porous.

[0019] The conductive material which forms an embedded conductive region within the interconnect structure includes any material that has the ability to transfer electricity. Examples of conductive material that can be present in the conductive region include, for example, polySi, a conductive metal, a conductive metal alloy, a conductive metal silicide or combinations and multilayers thereof. In one embodiment of the present invention, the conductive material includes a conductive metal such as, for example, Cu, W, and/or Al. In a highly preferred embodiment of the present invention, the conductive material includes a Cu-containing conductive material such as, for example, Cu, or a Cu alloy (such as AlCu).

[0020] As mentioned above, the conductive material is separated from the dielectric material by a diffusion barrier. The diffusion barrier prevents diffusion of the conductive material into the dielectric material. Examples of diffusion barriers that can be present within the conductive

region include, for example, Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, IrTa, IrTaN, W, WN or combinations and multilayers thereof.

[0021] The conductive material may be present within a via opening, a line opening, a combined via and line opening or any combination thereof.

[0022] The term "noble metal-containing" when referring to the cap located directly atop the at least one conductive material includes any metal that is resistant to corrosion or oxidation. The preferred noble metals that can be used in the present invention are selected from the group consisting of Ru, Ir, Rh, Pt, Co, W and alloys thereof. More preferably, the noble metal employed as the noble metal-containing cap comprises Ru or a Ru alloy.

[0023] In addition to the interconnect structure mentioned above, the present invention also provides a method of fabricating the same. In general terms, the inventive method includes:

providing a dielectric material having a dielectric constant of about 3.0 or less and at least one conductive material embedded therein, the at least one conductive material has an upper surface that is coplanar with an upper surface of the dielectric material; and

forming a noble metal-containing cap directly on the upper surface of the at least one conductive material, wherein the noble metal cap is discontinuous or non-uniform.

Brief Description of the Drawings

[0024] FIGS. 1A-1D are pictorial representations (through cross sectional views) illustrating the formation of a circuit dead opening in a prior art interconnect structure which is caused by EM failure.

[0025] FIG. 2 is a prior art interconnect structure (through a cross sectional view) including a Co-containing alloy metal cap located atop a conductive material that is embedded within a

dielectric material, and metal residues from the Co-containing alloy cap process are present on the dielectric surface.

[0026] FIG. 3 is a prior interconnect structure (through a cross sectional view) including a recessed conductive material embedded within a dielectric material, said recessed conductive material having a metal capping layer located thereon.

[0027] FIGS. 4A-4E are pictorial representations (through cross-sectional views) illustrating an interconnect structure that can be formed in the present invention containing a discontinuous noble metal-containing cap atop a conductive material embedded within a dielectric material. It is noted that FIGS. 4B-4E are cross-sectional views that are parallel to the opening formed into the dielectric material.

[0028] FIG. 5 is a pictorial representation (through a cross-sectional view that is parallel to the opening formed into the dielectric material) illustrating an alternative interconnect structure that can be formed in the present invention containing a non-uniform noble metal-containing cap atop a conductive material embedded within a dielectric material.

Detailed Description of the Invention

[0029] The present invention, which provides interconnect structures having enhanced electromigration (EM) resistance without degrading time dependent dielectric breakdown reliability and a method of forming the same, will now be described in greater detail by referring to the following discussion and drawings that accompany the present application. It is noted that the drawings of the present application are provided for illustrative purposes only and, as such, the drawings are not drawn to scale.

[0030] In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, in order to provide a thorough understanding of the present invention. However, it will be appreciated by

one of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well-known structures or processing steps have not been described in detail in order to avoid obscuring the invention.

[0031] It will be understood that when an element as a layer, region or substrate is referred to as being "on" or "over" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0032] As stated above, the present invention provides an interconnect structure (See, for example, FIG. 4E and FIG. 5) including a dielectric material having a dielectric constant of about 3.0 or less and having at least one conductive material embedded therein. The at least one conductive material has an upper surface that is coplanar with an upper surface of the dielectric material. The inventive interconnect structure also includes a noble metal-containing cap that is present at least on some portion of the upper surface of the at least one conductive material. In one embodiment, the noble metal-containing cap is discontinuous, e.g., exists as nuclei or islands on the surface of the at least one conductive material. In another embodiment, the noble metal-containing cap has a non-uniform thickness across the surface of the at least one conductive material.

[0033] In the inventive structure, there is no "residues" from the noble metal-containing cap deposited on the dielectric surface. By "residues" it is meant that no fragments of noble metal material form on the dielectric material surface. In some embodiments, the noble metal-containing cap is not present on an upper surface of a diffusion barrier that separates the at least one conductive material from the dielectric material.

[0034] The present invention also provides a method of fabricating an interconnect structure which includes a discontinuous/non-uniform noble metal-containing cap. In general terms, the inventive method, which is illustrated, for example, in FIGS. 4A-4E, includes providing a dielectric material having a dielectric constant of about 3.0 or less and at least one conductive material embedded therein. The at least one conductive material has an upper surface that is coplanar with an upper surface of the dielectric material. Next, a noble metal-containing cap is formed directly on the upper surface of the at least one conductive material. The noble metal-containing cap may be a discontinuous cap or a non-uniform cap that has a rough surface.

[0035] Specifically, FIG. 4A illustrates an initial structure 50 that can be employed in the present invention in fabricating the inventive interconnect structure. The initial structure 50 includes a dielectric material 52 having a pad stack 54 located on an upper surface thereof.

[0036] It is noted that the initial structure 50 is typically located upon a substrate (not shown in the drawings of the present application). The substrate may comprise a semiconducting material, an insulating material, a conductive material or any combination including multilayers thereof. When the substrate is comprised of a semiconducting material, any semiconductor such as Si, SiGe, SiGeC, SiC, Ge alloys, GaAs, InAs, InP and other III/V or II/VI compound semiconductors may be used. In addition to these listed types of semiconducting materials, the present invention also contemplates cases in which the semiconductor substrate is a layered semiconductor such as, for example, Si/SiGe, Si/SiC, silicon-on-insulators (SOIs) or silicon germanium-on-insulators (SGOIs).

[0037] When the substrate is an insulating material, the insulating material can be an organic insulator, an inorganic insulator or a combination thereof including multilayers. When the substrate is a conducting material, the substrate may include, for example, polySi, an elemental metal, alloys of elemental metals, a metal silicide, a metal nitride or combinations thereof including multilayers. When the substrate comprises a semiconducting material, one or more semiconductor devices such as, for example, complementary metal oxide semiconductor (CMOS) devices can be fabricated thereon.

[0038] When the substrate comprises a combination of an insulating material and a conductive material, the substrate may represent a first interconnect level of a multilayered interconnect structure.

[0039] The dielectric material 52 of the initial structure 50 comprises any interlevel or intralevel dielectric including inorganic dielectrics or organic dielectrics. The dielectric material 52 may be porous, non-porous or contain regions and/or surfaces that are porous and other regions and/or surfaces that may be non-porous. Some examples of suitable dielectrics that can be used as the dielectric material 52 include, but are not limited to silsesquioxanes, C doped oxides (i.e., organosilicates) that include atoms of Si, C, O and H, thermosetting polyarylene ethers, or multilayers thereof. The term "polyarylene" is used in this application to denote aryl moieties or inertly substituted aryl moieties which are linked together by bonds, fused rings, or inert linking groups such as, for example, oxygen, sulfur, sulfone, sulfoxide, carbonyl and the like.

[0040] The dielectric material 52 typically has a dielectric constant that is about 3.0 or less, with a dielectric constant of about 2.8 or less being even more typical. All dielectric constants mentioned herein are relative to a vacuum, unless otherwise noted. These dielectrics generally have a lower parasitic cross talk as compared with dielectric materials that have a higher dielectric constant than 4.0. The thickness of the dielectric material 52 may vary depending upon the dielectric material used as well as the exact number of dielectric layers within the dielectric material 52. Typically, and for normal interconnect structures, the dielectric material 52 has a thickness from 50 nm to 1000 nm.

[0041] The dielectric material 52 is formed utilizing any conventional deposition process including, but not limited to chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), evaporation, chemical solution deposition and spin-on coating.

[0042] After forming the dielectric material 52, pad stack 54 is formed on an exposed upper surface of dielectric material 52. The pad stack 54 comprises an oxide, nitride, oxynitride or

multilayers thereof (e.g., a pad stack comprising a pad oxide and a pad nitride). The pad stack 54 typically comprises a semiconductor oxide, semiconductor nitride and/or a semiconductor oxynitride. Preferably, the pad stack 54 comprises an oxide of silicon and/or a nitride of silicon.

[0043] In some embodiments, the pad stack 54 may be formed utilizing any conventional deposition process including, for example, CVD, PECVD, evaporation, chemical solution deposition, physical vapor deposition (PVD) and atomic layer deposition (ALD). In other embodiments, the pad stack 54 is formed by a thermal process such as, for example, a thermal oxidation, a thermal nitridation and/or a thermal oxynitridation process. In yet other embodiments, the pad stack 54 is formed utilizing a combination of deposition and thermal processes.

[0044] The thickness of the pad stack 54 may vary depending on the number of materials within the pad stack itself as well as the technique that was used in forming the same. Typically, the pad stack 54 has a thickness from 10 nm to 80 nm.

[0045] After forming the initial structure 50 shown in FIG. 4A, at least one opening 56 is formed into the dielectric material 52 utilizing the pad stack 54 as a pattern mask. The resultant structure including the at least one opening 56 is shown, for example, in FIG. 4B. The at least one opening 56 may include a via opening, a line opening, a combined via and line opening, or any combination thereof. In the drawings, a line opening is shown by way of a non-limiting example.

[0046] The at least one opening 56 is formed utilizing conventional lithography and etching. The lithographic step includes forming a photoresist (organic, inorganic or hybrid) atop the pad stack 54 utilizing a conventional deposition process such as, for example, CVD, PECVD and spin-on coating. Following formation of the photoresist, the photoresist is exposed to a desired pattern of radiation. Next, the exposed photoresist is developed utilizing a conventional resist development process.

[0047] After the development step, an etching step is performed to transfer the pattern from the patterned photoresist into first the pad stack 54 and then the dielectric material 52. The patterned photoresist is typically removed from the surface of the structure after transferring the pattern into the pad stack 54 utilizing a conventional resist stripping process such as, for example, ashing. The etching step used in forming the at least one opening 56 comprises a dry etching process (including reactive ion etching, ion beam etching, plasma etching or laser ablation), a wet chemical etching process or any combination thereof. Typically, reactive ion etching is used to form the at least one opening 56.

[0048] Next, and as shown in FIG. 4C, a diffusion barrier 58 and a conductive material 60 are formed into each of the at least one openings 56. The diffusion barrier 58 comprises Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, IrTa, IrTaN, W, WN or any other material that can serve as a barrier to prevent conductive material from diffusing there through. The thickness of the diffusion barrier 58 may vary depending on the deposition process used as well as the material employed. Typically, the diffusion barrier 58 has a thickness from 4 nm to 40 nm, with a thickness from 7 nm to 20 nm being more typical.

[0049] The diffusion barrier 58, which is located between the conductive material 60 and the dielectric material 52 is formed by any conventional deposition process including, for example, CVD, PECVD, PVD, sputtering and plating.

[0050] The conductive material 60 used in forming the conductive region of the interconnect structure includes, for example, polySi, a conductive metal, an alloy comprising at least one conductive metal, a conductive metal silicide or combinations thereof. Preferably, the conductive material 60 that is used in forming the conductive region is a conductive metal such as Cu, W or Al, with Cu or a Cu alloy (such as AlCu) being highly preferred in the present invention.

[0051] The conductive material 60 is formed into each of the openings 56 that are lined with the diffusion barrier 58 utilizing any conventional deposition process including, for example, CVD,

PECVD, PVD, sputtering, plating, chemical solution deposition and electroless plating. After deposition of the conductive material 60, the structure is subjected to a planarization process such as, for example, chemical mechanical polishing (CMP) and/or grinding. The planarization process provides a planar structure such as is shown in FIG. 4C in which the upper surfaces of the dielectric material 52, the diffusion barrier 58 (which is now U-shaped) and the conductive material 60 are substantially coplanar with each other. It is noted that during the planarization process, the remaining pad stack 54 is removed from the structure.

[0052] Next, and as is shown in FIG. 4D, a discontinuous noble metal-containing cap 62 is selectively formed essentially atop the conductive material 60. The term "noble metal-containing" when referring to the discontinuous noble metal cap 62 located essentially atop the at least one conductive region (i.e., conductive material 60) includes any metal that is resistant to corrosion or oxidation. The term "essentially" when referring to the discontinuous noble metal-containing cap 62 is used herein to denote that no portion of the cap extends onto the surface of the dielectric material. Preferably, no portion of the cap 62 extends onto the diffusion barrier.

[0053] The preferred noble metals that can be used in the present invention as the discontinuous noble metal-containing cap 62 are selected from the group consisting of Ru, Ir, Rh, Pt, Co, W and alloys thereof. The term "alloy" is used to denote a mixture of noble metals as well as elements such as W, B and P. More preferably, the noble metal employed as the discontinuous noble metal-containing cap 62 comprises Ru or a Ru alloy. In some embodiments, the discontinuous noble metal-containing cap 62 includes a multilayered noble metal or noble metal alloy stack.

[0054] The thickness of the discontinuous noble metal-containing cap 62 may vary depending on the type of noble metal present in the cap, the deposition technique and conditions used as well as the number of noble metals within the cap. Typically, the discontinuous noble metal-containing cap 62 has a thickness from 1 Å to 100 Å, with a thickness from 5 Å to 50 Å being more highly preferred.

[0055] In some embodiments of the present invention, the discontinuous metal-containing cap 62 is formed by a chemical deposition process including, for example, CVD, PECVD and ALD. When a chemical deposition process is used in forming the discontinuous noble metal-containing cap 62, the discontinuity within the cap is achieved by controlling at least one of the deposition time, the deposition pressure and the deposition temperature.

[0056] Specifically, the applicants have determined that a discontinuous noble metal-containing cap, as described above, can be obtained by performing the chemical deposition using at least one of the following deposition parameters: A deposition time of less than 3 minutes, preferably from 0.1 minutes to 2 minutes, and more preferably from 0.5 minutes to 1 minute. A deposition pressure of 50 mTorr or less, preferably 20 mTorr or less, and more preferably from 5 mTorr to 20 mTorr. A deposition temperature of 300°C or less, preferably 200°C or less, and more preferably from 150°C to 200°C. In a highly preferred embodiment of the invention, a discontinuous noble metal-containing cap 62 can be obtained by chemical deposition at a temperature from 150°C to 200°C and a pressure from 5 mTorr to 20 mTorr for a duration of less than 1 minute.

[0057] In addition to chemical deposition, a discontinuous noble metal-containing cap 62 can be formed by utilizing electroless plating or by electroplating. Electroplating is a process of using electrical current to reduce cations of a desired material, e.g., a noble metal, from a solution and coat a conductive object, e.g., the at least one conductive material, with a thin layer of the material, e.g., the noble metal. In electroless plating, a redox reaction involving the oxidation of one or more soluble reducing agents such as, for example, hypophosphite, and the reduction of one or metallic ions, e.g., noble metal ions, occurs on the surface of a substrate, e.g., the at least one conductive material.

[0058] When plating techniques are used in forming a discontinuous cap, the discontinuity within the cap is achieved by performing the plating process for a duration of time of less than 3 minutes, preferably from 0.1 minutes to 2 minutes, and more preferably from 0. 5 minutes to 1

minute. The plating temperature and pressure are not relative for this embodiment for controlling the discontinuity of the cap 62.

[0059] In addition to the above techniques that have been described, the discontinuous noble metal-containing cap 62 can be formed by first forming a continuous noble metal-containing cap across the entire surface of the at least one conductive material; some of the noble metal cap may extend onto an upper surface of the diffusion barrier, but not onto the dielectric material. Such deposition is achieved utilizing a low temperature chemical deposition process including, for example, CVD, PECVD, low pressure CVD and ALD. By "low temperature", it is meant a deposition temperature of about 200°C or less, with a deposition temperature of less than about 150°C being even more preferred. The deposition conditions are selected to provide a deposition rate of the continuous noble metal-containing cap onto the conductive material 60 that is from 0.2 to 1.2 Å/sec.

[0060] After forming the continuous noble metal-containing cap, portions of the continuous noble metal-containing cap are selectively removed so as to form a discontinuous noble metal-containing cap, as described above. The selective removal may be performed by first forming a patterned mask or block mask over portions of the structure, including portions of the continuous noble metal-containing cap. Next, a selective etching process including, for example, a dry etch or a wet chemical etch can be used. When dry etching is used, one of reactive ion etching, ion beam etching, plasma etching and laser ablation can be used. When a wet chemical etch is employed, a mixture of HCl, H_2SO_4, HF and HNO_3 can be used as a chemical etchant. In yet another embodiment, the selective removal can be achieved using a touch-up chemical mechanical polishing (CMP) process. By "touch-up CMP" it is meant a short, less than 1 minute, and non-uniform CMP process.

[0061] After selectively forming the discontinuous noble metal-containing cap 62 predominately onto conductive material 60, a dielectric capping layer 64 is formed across the entire structure shown in FIG. 4D. The resultant structure including the dielectric capping layer 64 is shown, for example, in FIG. 4E. The dielectric capping layer 64 comprises any suitable dielectric capping

material such as, for example, SiC, Si_4NH_3, SiO_2, a carbon doped oxide, a nitrogen and hydrogen doped silicon carbide SiC(N,H) or multilayers thereof.

[0062] The thickness of the dielectric capping layer 64 may vary depending on the technique used to form the same as well as the material make-up of the layer. Typically, the dielectric capping layer 64 has a thickness from 15 nm to 100 nm, with a thickness from 25 nm to 45 nm being more typical.

[0063] The dielectric capping layer 64 is formed utilizing any conventional deposition process including, for example, CVD, PECVD, evaporation, spin-on coating and chemical solution deposition.

[0064] FIG. 4E illustrates an interconnect structure in accordance with an embodiment of the present invention. Specifically, this inventive interconnect structure includes a dielectric material 52 having a dielectric constant of about 3.0 or less. The dielectric material 52 has at least one conductive region (represented by conductive material 60) embedded within the dielectric material 52, said at least one conductive region having an upper surface. A discontinuous noble metal cap 62 is located directly on the upper surface of the at least one conductive region (i.e., conductive material 60).

[0065] FIG. 5 illustrates an alternative interconnect structure that can be employed in the present invention. The alternative interconnect structure of FIG. 5 is essentially the same as the interconnect structure shown in FIG. 4E, except that the discontinuous noble metal–containing cap 62 is replaced with a noble metal cap that has a rough surface that is characterized as having a variable thickness across the entire surface of the at least one conductive material. In the alternative interconnect structure, reference numeral 62' is used to denote the 'non-uniform' noble metal-containing cap. The non-uniform noble metal-containing cap 62' is formed utilizing basically the same chemical deposition techniques and materials as described above. One difference between the above described chemical depositions techniques that ensures a non-uniform noble metal-containing cap 62' is that longer processing times are used. For example, a

non-uniform noble metal-containing cap 62' can be formed using a desposition time of less than 5 minutes, preferably from 0.5 to 3 minutes, and more preferably from 1 minute to 2 minutes.

[0066] Notwithstanding whether a discontinuous or non-uniform noble metal-containing cap is formed, the applicants have determined that the presence of either the discontinuous noble metal-containing cap or the non-uniform noble metal-containing cap atop a conductive material embedded within an interconnect dielectric improves the EM resistance of the interconnect structure. In prior art interconnect structures, a continuous noble metal-containing cap is used and was thought to be the desired cap design for EM improvement. In addition to improved EM, the applicants have determined that the presence of either the discontinuous noble metal-containing cap or the non-uniform noble metal-containing cap atop a conductive material embedded within an interconnect dielectric also improves the time dependent dielectric breakdown (TDDB) reliability of the interconnect structure. Such an improved in TDDB reliability is not observed when a continuous noble metal-containing cap is employed.

[0067] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

CLAIMS:

1. An interconnect structure comprising:

a dielectric material having a dielectric constant of about 3.0 or less and at least one conductive material embedded therein, the at least one conductive material having an upper surface that is coplanar with an upper surface of the dielectric material; and

a discontinuous noble metal-containing cap present at least on some portion of the upper surface of the at least one conductive material, while other portions of the upper surface of the at least one conductive material that are located between adjacent portions of the discontinuous noble-metal containing cap are bare, wherein said discontinuous noble metal-containing cap is selected from the group consisting of Ir, Rh, Pt, Co and alloys thereof.

2. An interconnect structure comprising:

a dielectric material having a dielectric constant of about 3.0 or less and at least one conductive material embedded therein, the at least one conductive material having an upper surface that is coplanar with an upper surface of the dielectric material; and

a discontinuous noble metal-containing cap present at least on some portion of the upper surface of the at least one conductive material, while other portions of the upper surface of the at least one conductive material that are located between adjacent portions of the discontinuous noble-metal containing cap are bare, wherein said discontinuous noble metal-containing cap comprises Ru or a Ru alloy.

3. The interconnect structure of Claim 1, further comprising a dielectric capping layer located atop said dielectric material, said discontinuous noble metal-containing cap and said other portions of the upper surface of the at least one conductive material that are located between adjacent portions of the discontinuous noble-metal containing cap that are bare.

4. The interconnect structure of Claim 3, wherein said dielectric capping layer comprises SiC, Si_4NH_3, SiO_2, a carbon doped oxide, a nitrogen and hydrogen doped silicon carbide SiC(N,H) or multilayers thereof.

5. The interconnect structure of Claim 1, wherein said at least one conductive material comprises polySi, a conductive metal, a conductive metal alloy, a conductive metal silicide or combinations and multilayers thereof.

6. The interconnect structure of Claim 5, wherein said at least one conductive material is a conductive metal selected from one of Cu, W and Al.

7. The interconnect structure of Claim 1, wherein said dielectric material comprises a silsesquioxane, a C doped oxide that includes at least atoms of Si, C, O and H, a thermosetting polyarylene ether, or multilayers thereof.

8. An interconnect structure comprising:

a dielectric material having a dielectric constant of about 3.0 or less and at least one conductive material embedded therein, the at least one conductive material having an upper surface that is coplanar with an upper surface of the dielectric material; and

a noble metal-containing cap present on an entirety of the upper surface of the at least one conductive material, said noble metal-containing cap having a non-uniform thickness and does not extend beyond outer edges of the at least one conductor material onto said upper surface of said dielectric material and an upper surface of a diffusion barrier that is positioned between said conductive material and said dielectric material.

9. The interconnect structure of Claim 8, wherein said noble metal-containing cap is selected from the group consisting of Ru, Ir, Rh, Pt, Co, W and alloys thereof.

10. The interconnect structure of Claim 9, wherein said noble metal-containing cap comprises Ru or a Ru alloy.

11. The interconnect structure of Claim 8, further comprising a dielectric capping layer located atop said dielectric material and said noble metal-containing cap.

12. The interconnect structure of Claim 11, wherein said dielectric capping layer comprises SiC, Si_4NH_3, SiO_2, a carbon doped oxide, a nitrogen and hydrogen doped silicon carbide SiC(N,H) or multilayers thereof.

13. The interconnect structure of Claim 8, wherein said at least one conductive material comprises polySi, a conductive metal, a conductive metal alloy, a conductive metal silicide or combinations and multilayers thereof.

14. The interconnect structure of Claim 13, wherein said at least one conductive material is a conductive metal selected from one of Cu, W and Al.

15. The interconnect structure of Claim 8, wherein said dielectric material comprises a silsesquioxane, a C doped oxide that includes at least atoms of Si, C, O and H, a thermosetting polyarylene ether, or multilayers thereof.