

ABSTRACT

COMPUTATION OF STICKY-BIT IN PARALLEL WITH PARTIAL PRODUCTS IN A FLOATING POINT MULTIPLIER UNIT

A floating point unit multiply logic in which a sticky bit is computed in parallel with partial product generation and reduction for three different rounding precisions and two different operand ranges. Two sticky bits need to be calculated during the parallel operation because the result can be anywhere between 0 and 4 and it will not be known which is correct until after the result of the multiplication has been calculated. If the result is between 0 and 2, then a first sticky bit is generated. When the result is between 2 and 4, a second sticky bit is generated. It is not known which sticky bit is the correct one to use until the final addition is performed. Once the results of the final addition is known, the correct sticky bit is selected using a carry out from the adder, the overflow bit. If the overflow bit is a 1, then the first sticky bit is selected. If the overflow bit is a 0, then the second sticky bit is selected.

(Figure 3)