

THIS SHEET HAS BEEN
REPLACED

A B S T R A C T

A sequential process-pipeline (12) has a first processing stage (30) coupled to a CODEC (24) through a plurality of buffers, including an image data input buffer (28), an image data output buffer (26), and an address buffer (34). The address buffer stores addresses, each of which identifies an initial address of a block of addresses within an image memory (22). Each block of addresses in the image memory stores a block of decompressed image data. A local controller (18) is responsive to the writing of an address into the address buffer to initiate the operation of the CODEC to execute a Discrete Cosine Transformation Process and a Discrete Cosine Transformation Quantization Process.

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